

IRFPS40N60KPbF

HEXFET® Power MOSFET

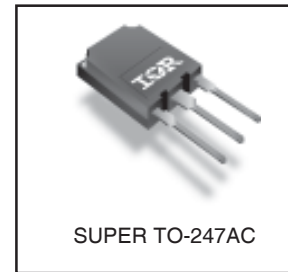
V_{DSS}	$R_{DS(on)}$ typ.	I_D
600V	0.110 Ω	40A

Applications

- Hard Switching Primary or PFC Switch
- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Motor Drive
- Lead-Free

Benefits

- Low Gate Charge Q_g results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Enhanced Body Diode dv/dt Capability



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	40	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	24	
I_{DM}	Pulsed Drain Current ①	160	
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	570	W
	Linear Derating Factor	4.5	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ②	5.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	$^\circ\text{C}$
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	600	mJ
I_{AR}	Avalanche Current ①	—	40	A
E_{AR}	Repetitive Avalanche Energy ①	—	57	mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.22	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

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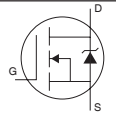
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	600	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.63	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ ⓐ
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.110	0.130	Ω	$V_{GS} = 10V, I_D = 24A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	50	μA	$V_{DS} = 600V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 480V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	21	—	—	S	$V_{DS} = 50V, I_D = 24A$
Q_g	Total Gate Charge	—	—	330	nC	$I_D = 38A$
Q_{gs}	Gate-to-Source Charge	—	—	84		$V_{DS} = 480V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	150		$V_{GS} = 10V$, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	47	—	ns	$V_{DD} = 300V$
t_r	Rise Time	—	110	—		$I_D = 38A$
$t_{d(off)}$	Turn-Off Delay Time	—	97	—		$R_G = 4.3\Omega$
t_f	Fall Time	—	60	—		$V_{GS} = 10V$, See Fig. 10 ④
C_{iss}	Input Capacitance	—	7970	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	750	—		$V_{DS} = 25V$
C_{riss}	Reverse Transfer Capacitance	—	75	—		$f = 1.0\text{MHz}$, See Fig. 5
C_{oss}	Output Capacitance	—	9440	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	200	—		$V_{GS} = 0V, V_{DS} = 480V, f = 1.0\text{MHz}$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	260	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 480V$ ⑤

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	40	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	160		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}, I_S = 38A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	630	950	ns	$T_J = 25^\circ\text{C}$
		—	730	1090		$T_J = 125^\circ\text{C}$
Q_{rr}	Reverse Recovery Charge	—	14	20	μC	$T_J = 25^\circ\text{C}$
		—	17	25		$T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	39	58	A	$T_J = 25^\circ\text{C}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.84\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 38A$, $dv/dt = 5.5V/ns$ (See Figure 12a)
- ③ $I_{SD} \leq 38A$, $di/dt \leq 150A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ $C_{oss \text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

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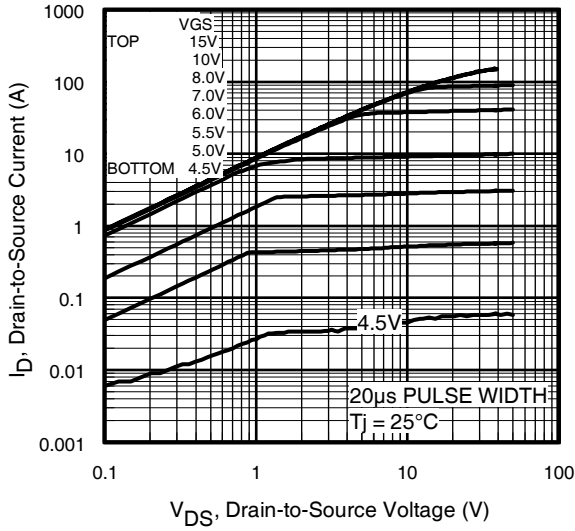


Fig 1. Typical Output Characteristics

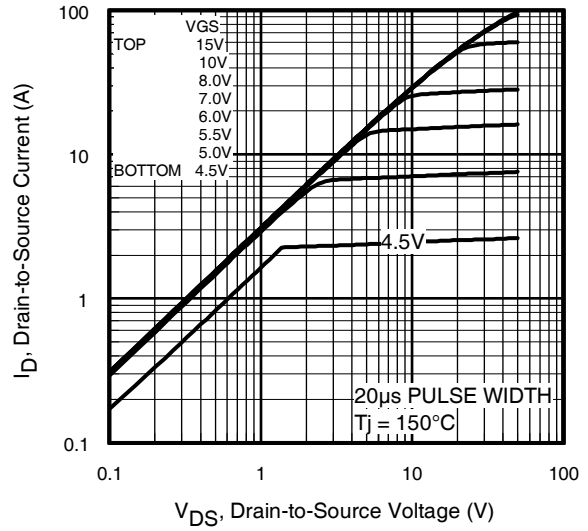


Fig 2. Typical Output Characteristics

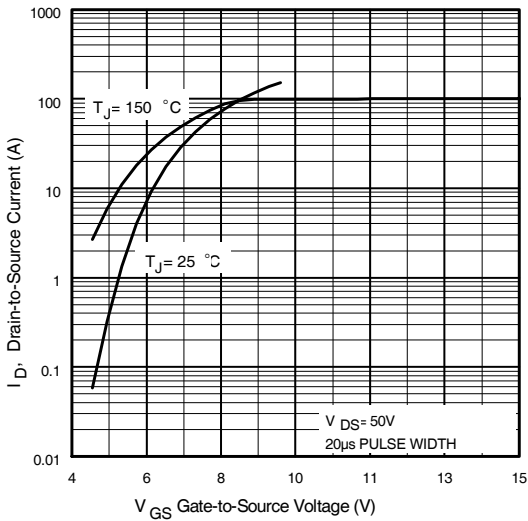


Fig 3. Typical Transfer Characteristics

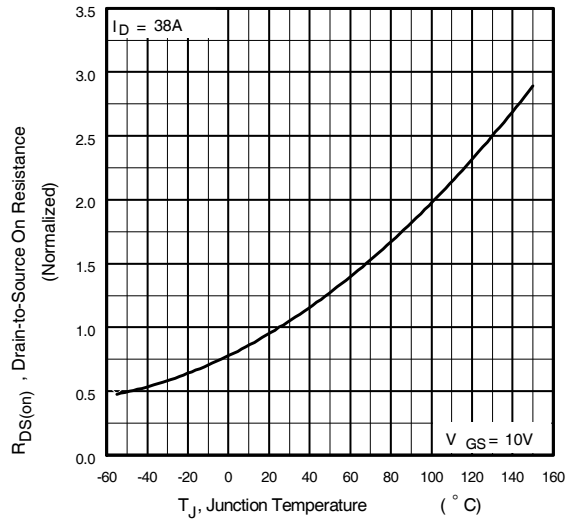


Fig 4. Normalized On-Resistance Vs. Temperature

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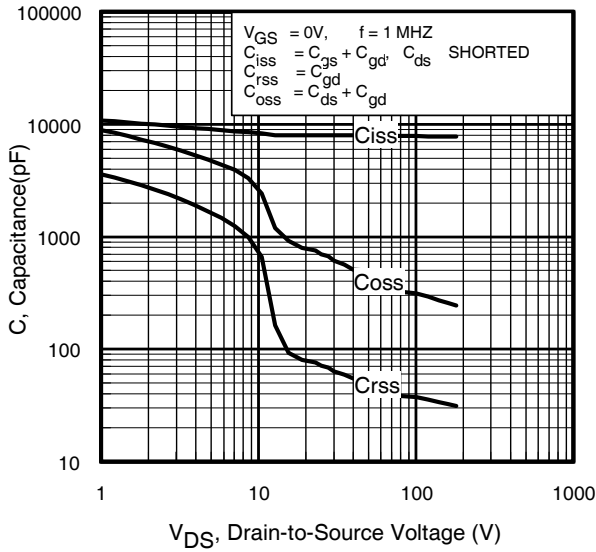


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

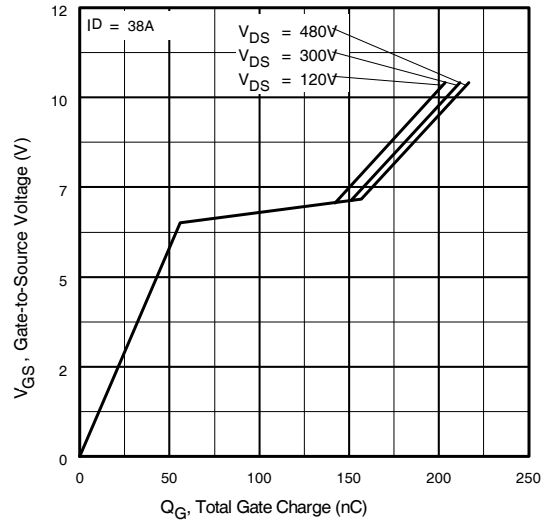


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

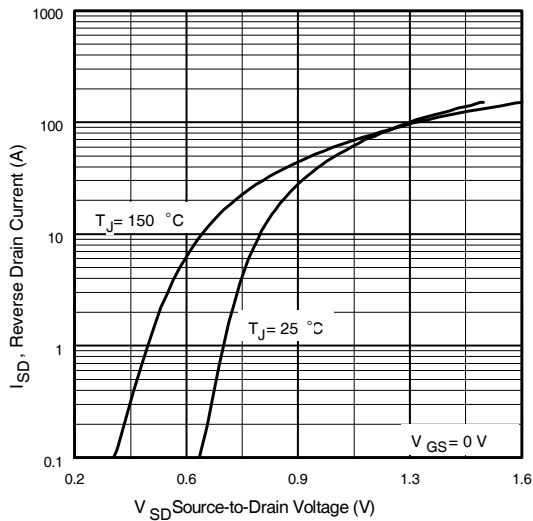


Fig 7. Typical Source-Drain Diode Forward Voltage

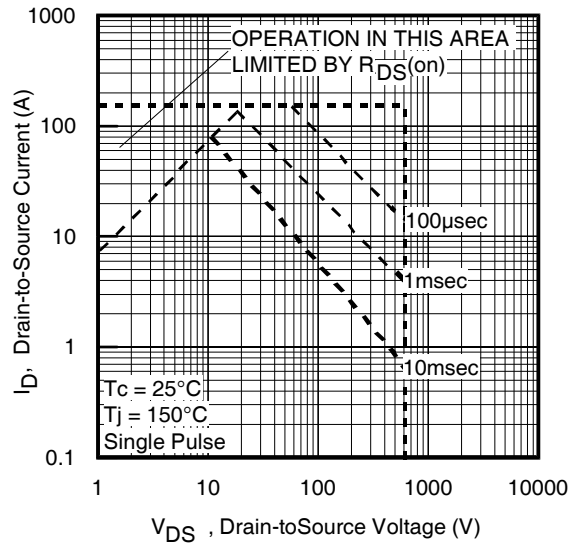


Fig 8. Maximum Safe Operating Area

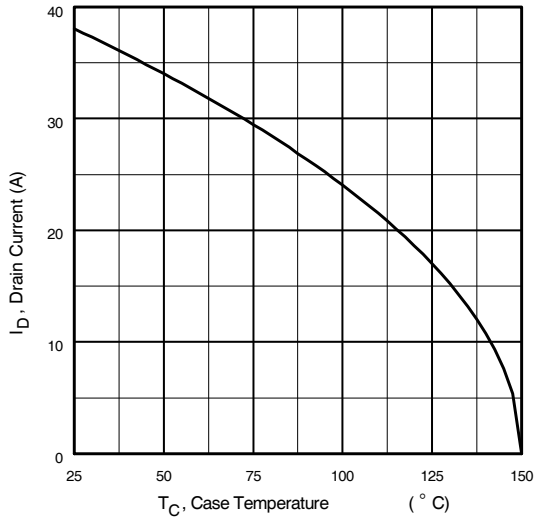


Fig 9. Maximum Drain Current Vs. Case Temperature

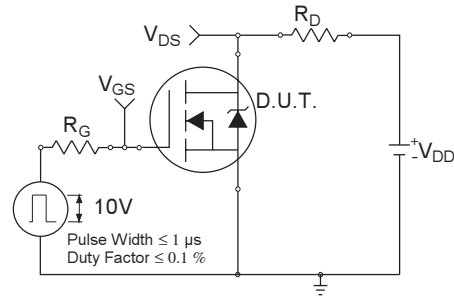


Fig 10a. Switching Time Test Circuit

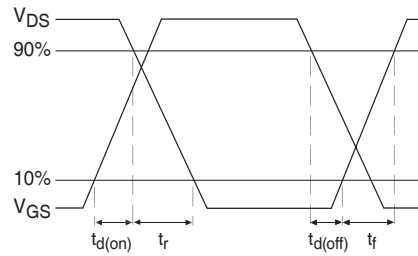


Fig 10b. Switching Time Waveforms

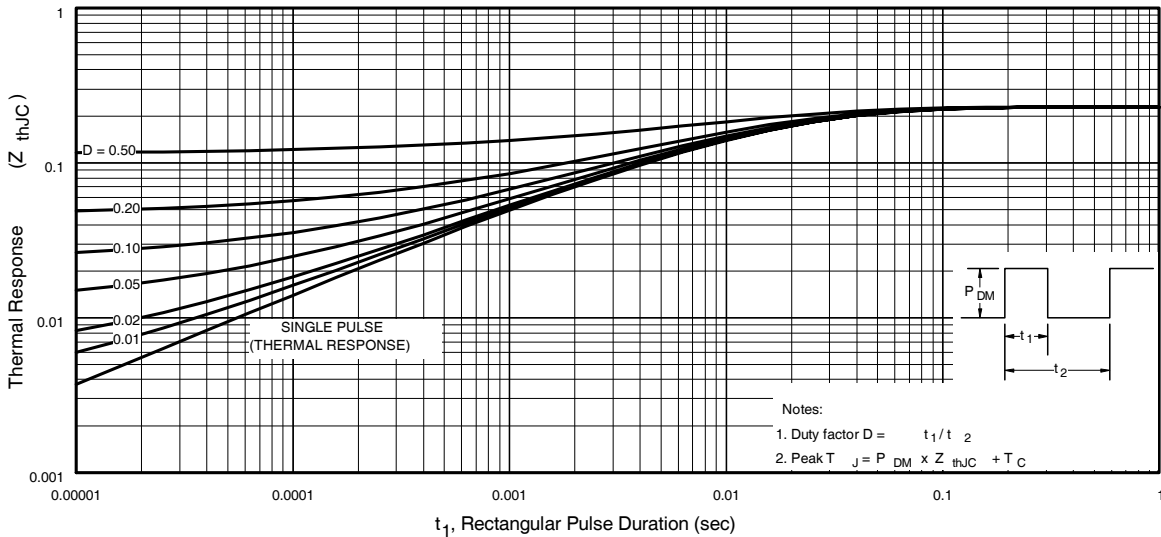


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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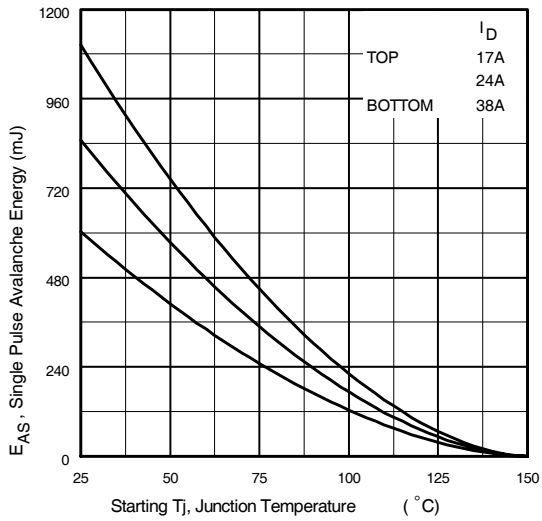


Fig 12a. Maximum Avalanche Energy Vs. Drain Current

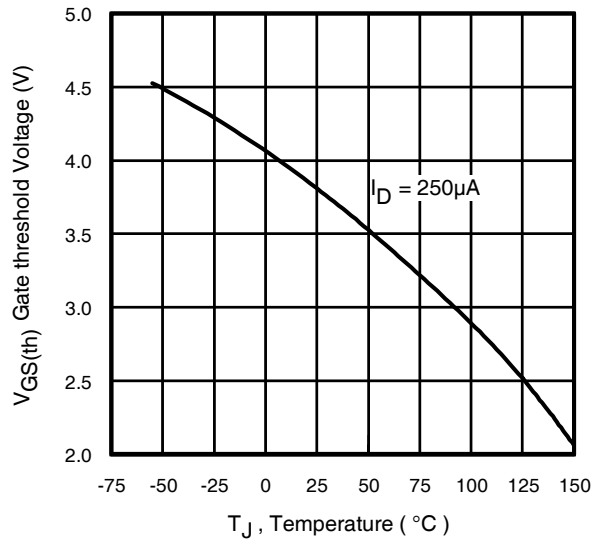


Fig 14. Threshold Voltage Vs. Temperature

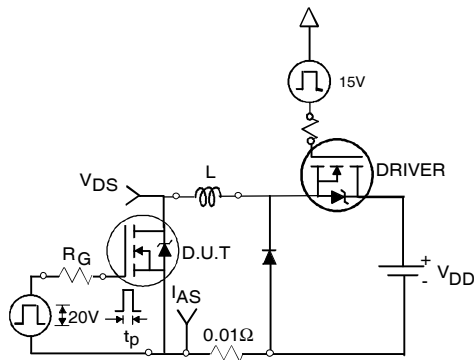


Fig 12c. Unclamped Inductive Test Circuit

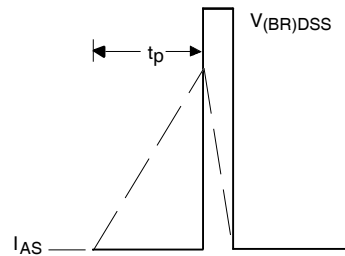


Fig 12d. Unclamped Inductive Waveforms

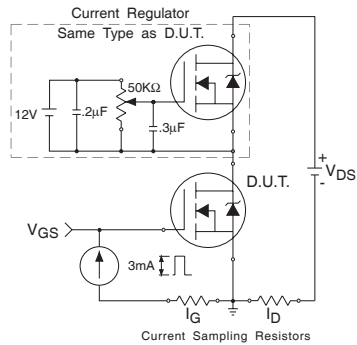


Fig 13a. Gate Charge Test Circuit

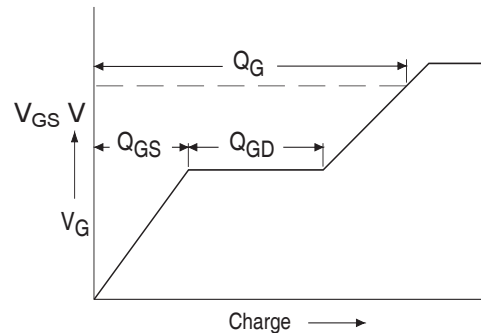
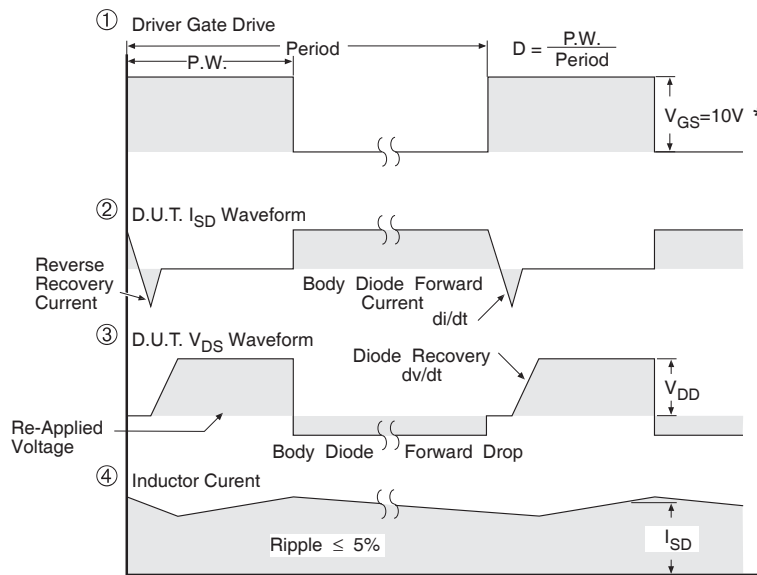
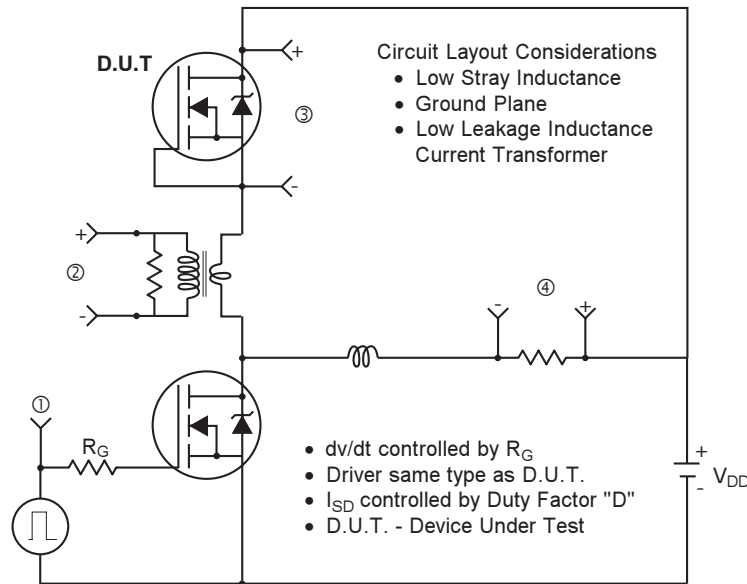


Fig 13b. Basic Gate Charge Waveform

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Peak Diode Recovery dv/dt Test Circuit



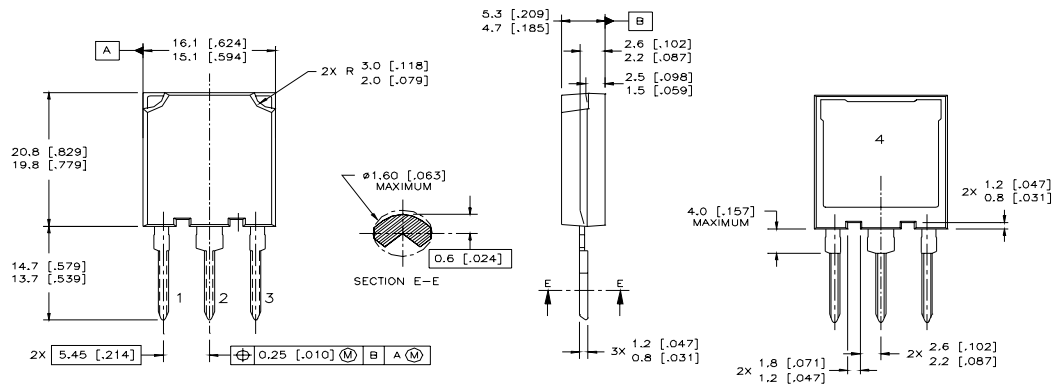
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

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Case Outline and Dimensions — Super-247



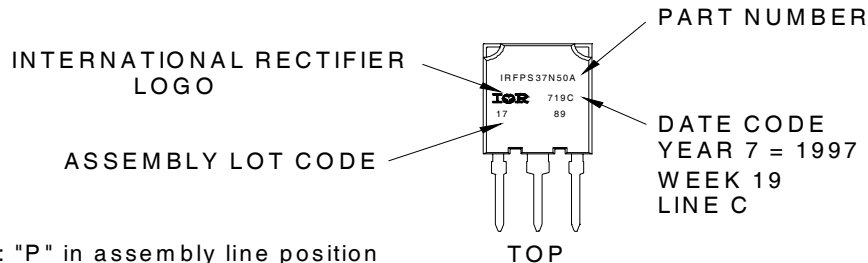
- NOTES:
 1. DIMENSIONS & TOLERANCING PER ASME Y14.5M-1994
 2. CONTROLLING DIMENSION: MILLIMETER
 3. DIMENSIONS ARE SHOWN IN MILLIMETRES [INCHES]

LEAD ASSIGNMENTS

MOSFET	IGBT
1 - GATE	1 - GATE
2 - DRAIN	2 - COLLECTOR
3 - SOURCE	3 - EMITTER
4 - DRAIN	4 - COLLECTOR

Super-247 (TO-274AA) Part Marking Information

EXAMPLE: THIS IS AN IRFPS37N50A WITH
 ASSEMBLY LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"



Note: "P" in assembly line position indicates "Lead-Free"

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Industrial market.
 Qualification Standards can be found on IR's Web site.

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