

IRF7317PbF

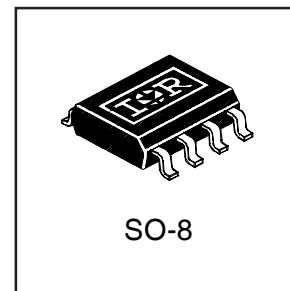
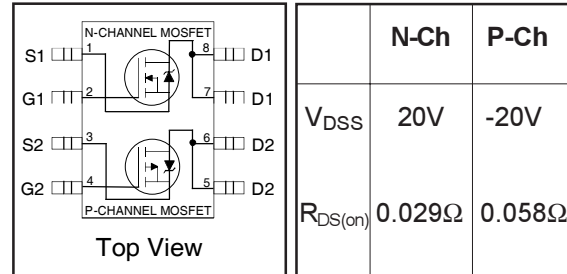
HEXFET® Power MOSFET

- Generation V Technology
- Ultra Low On-Resistance
- Dual N and P Channel MOSFET
- Surface Mount
- Fully Avalanche Rated
- Lead-Free

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques.



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

	Symbol	Maximum		Units
		N-Channel	P-Channel	
Drain-Source Voltage	V_{DS}	20	-20	
Gate-Source Voltage	V_{GS}	± 12		
Continuous Drain Current ^①	$T_A = 25^\circ\text{C}$ $T_A = 70^\circ\text{C}$	6.6	-5.3	A
		5.3	-4.3	
Pulsed Drain Current	I_{DM}	26	-21	
Continuous Source Current (Diode Conduction)	I_S	2.5	-2.5	
Maximum Power Dissipation ^②	$T_A = 25^\circ\text{C}$ $T_A = 70^\circ\text{C}$	2.0		W
		1.3		
Single Pulse Avalanche Energy	E_{AS}	100	150	mJ
Avalanche Current	I_{AR}	4.1	-2.9	A
Repetitive Avalanche Energy	E_{AR}	0.20		mJ
Peak Diode Recovery dv/dt ^③	dv/dt	5.0	-5.0	V/ ns
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to + 150 °C		

Thermal Resistance Ratings

Parameter	Symbol	Limit	Units
Maximum Junction-to-Ambient ^④	$R_{\theta JA}$	62.5	°C/W

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Parameter	Min.	Typ.	Max.	Units	Conditions	
						Parameter
V _{(BR)DSS}	N-Ch	20	—	—	V	V _{GS} = 0V, I _D = 250μA
	P-Ch	-20	—	—		V _{GS} = 0V, I _D = -250μA
ΔV _{(BR)DSS} /ΔT _J	N-Ch	—	0.027	—	V/°C	Reference to 25°C, I _D = 1mA
	P-Ch	—	0.031	—		Reference to 25°C, I _D = -1mA
R _{DS(ON)}	N-Ch	—	0.023	0.029	Ω	V _{GS} = 4.5V, I _D = 6.0A ④
		—	0.030	0.046		V _{GS} = 2.7V, I _D = 5.2A ④
	P-Ch	—	0.049	0.058		V _{GS} = -4.5V, I _D = -2.9A ④
		—	0.082	0.098		V _{GS} = -2.7V, I _D = -1.5A ④
V _{GS(th)}	N-Ch	0.7	—	—	V	V _{DS} = V _{GS} , I _D = 250μA
	P-Ch	-0.7	—	—		V _{DS} = V _{GS} , I _D = -250μA
g _{fs}	N-Ch	—	20	—	S	V _{DS} = 10V, I _D = 6.0A ④
	P-Ch	—	5.9	—		V _{DS} = -10V, I _D = -1.5A ④
I _{DSS}	N-Ch	—	—	1.0	μA	V _{DS} = 16V, V _{GS} = 0V
	P-Ch	—	—	-1.0		V _{DS} = -16V, V _{GS} = 0V
	N-Ch	—	—	5.0		V _{DS} = 16V, V _{GS} = 0V, T _J = 55°C
	P-Ch	—	—	-25		V _{DS} = -16V, V _{GS} = 0V, T _J = 55°C
I _{GSS}	N-P	—	—	±100	nA	V _{GS} = ±12V
Q _g	N-Ch	—	18	27	nC	N-Channel I _D = 6.0A, V _{DS} = 10V, V _{GS} = 4.5V ④
	P-Ch	—	19	29		
Q _{gs}	N-Ch	—	2.2	3.3	nC	P-Channel I _D = -2.9A, V _{DS} = -16V, V _{GS} = -4.5V
	P-Ch	—	4.0	6.1		
Q _{gd}	N-Ch	—	6.2	9.3	nC	N-Channel V _{DD} = 10V, I _D = 1.0A, R _G = 6.0Ω, R _D = 10Ω ④
	P-Ch	—	7.7	12		
t _{d(on)}	N-Ch	—	8.1	12	ns	P-Channel V _{DD} = -10V, I _D = -2.9A, R _G = 6.0Ω, R _D = 3.4Ω ④
	P-Ch	—	15	22		
t _r	N-Ch	—	17	25	ns	N-Channel V _{GS} = 0V, V _{DS} = 15V, f = 1.0MHz
	P-Ch	—	40	60		
t _{d(off)}	N-Ch	—	38	57	ns	P-Channel V _{GS} = 0V, V _{DS} = -15V, f = 1.0MHz
	P-Ch	—	42	63		
t _f	N-Ch	—	31	47	ns	N-Channel V _{GS} = 0V, V _{DS} = -15V, f = 1.0MHz
	P-Ch	—	49	73		
C _{iss}	N-Ch	—	900	—	pF	P-Channel V _{GS} = 0V, V _{DS} = -15V, f = 1.0MHz
P-Ch	—	780	—			
C _{oss}	N-Ch	—	430	—	pF	N-Channel V _{GS} = 0V, V _{DS} = 15V, f = 1.0MHz
	P-Ch	—	470	—		
C _{rss}	N-Ch	—	200	—	pF	P-Channel V _{GS} = 0V, V _{DS} = -15V, f = 1.0MHz
	P-Ch	—	240	—		

Source-Drain Ratings and Characteristics

Parameter	Min.	Typ.	Max.	Units	Conditions	
						Parameter
I _S	N-Ch	—	—	2.5	A	
	P-Ch	—	—	-2.5		
I _{SM}	N-Ch	—	—	26	A	
	P-Ch	—	—	-21		
V _{SD}	N-Ch	—	0.72	1.0	V	T _J = 25°C, I _S = 1.7A, V _{GS} = 0V ③
	P-Ch	—	-0.78	-1.0		T _J = 25°C, I _S = -2.9A, V _{GS} = 0V ③
t _{rr}	N-Ch	—	52	77	ns	N-Channel T _J = 25°C, I _F = 1.7A, di/dt = 100A/μs ④
	P-Ch	—	47	71		
Q _{rr}	N-Ch	—	58	86	nC	P-Channel T _J = 25°C, I _F = -2.9A, di/dt = 100A/μs ④
	P-Ch	—	49	73		

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 22)
- ② N-Channel I_{SD} ≤ 4.1A, di/dt ≤ 92A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 150°C
P-Channel I_{SD} ≤ -2.9A, di/dt ≤ -77A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 150°C
- ③ N-Channel Starting T_J = 25°C, L = 12mH R_G = 25Ω, I_{AS} = 4.1A. (See Figure 12)
P-Channel Starting T_J = 25°C, L = 35mH R_G = 25Ω, I_{AS} = -2.9A.
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ⑤ Surface mounted on FR-4 board, t ≤ 10sec.

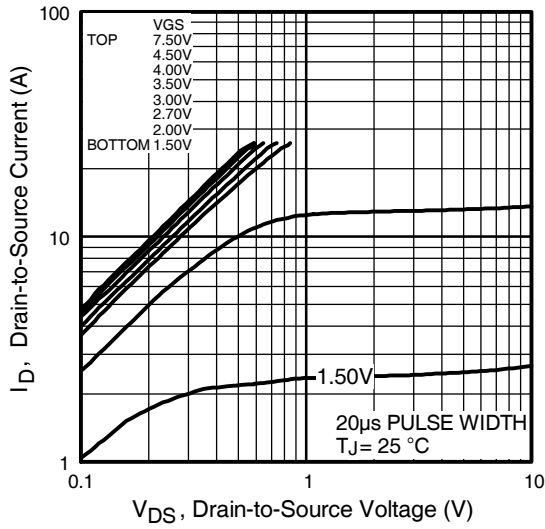


Fig 1. Typical Output Characteristics

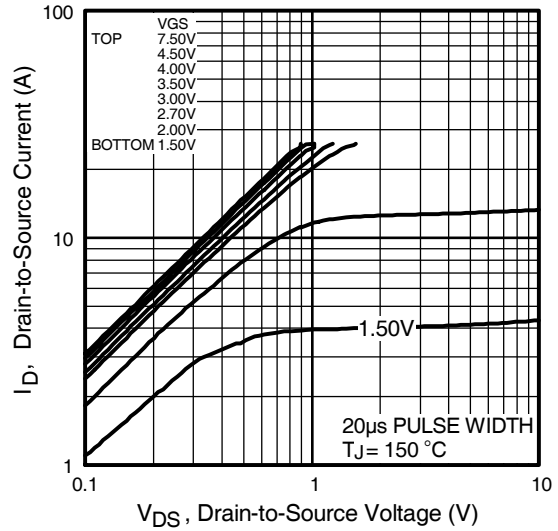


Fig 2. Typical Output Characteristics

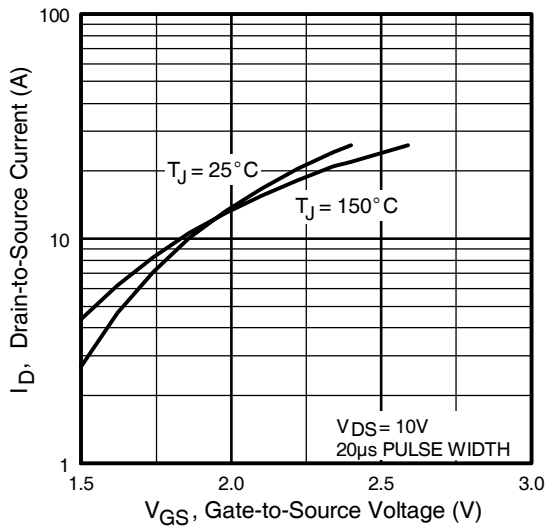


Fig 3. Typical Transfer Characteristics

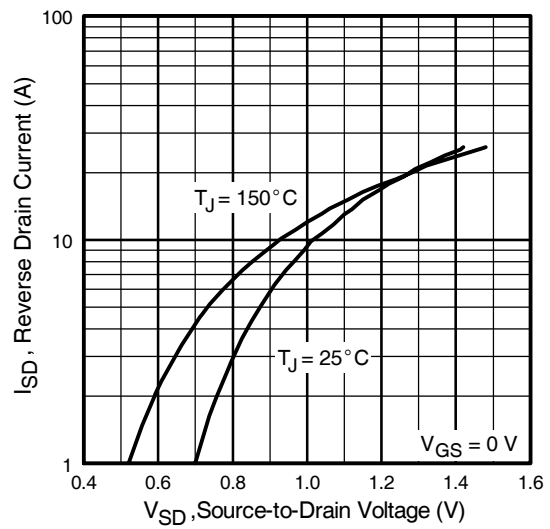


Fig 4. Typical Source-Drain Diode Forward Voltage

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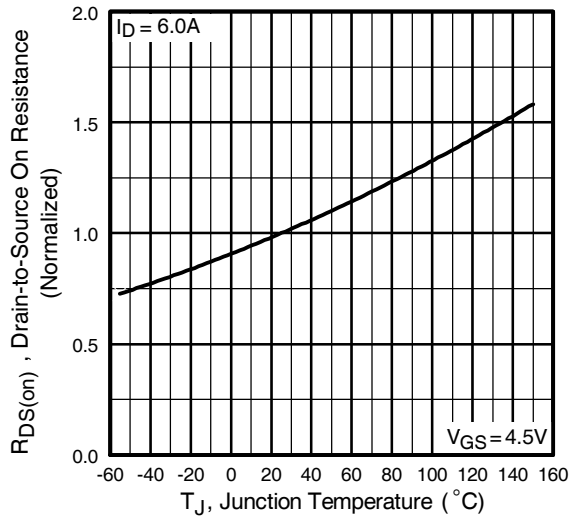


Fig 5. Normalized On-Resistance Vs. Temperature

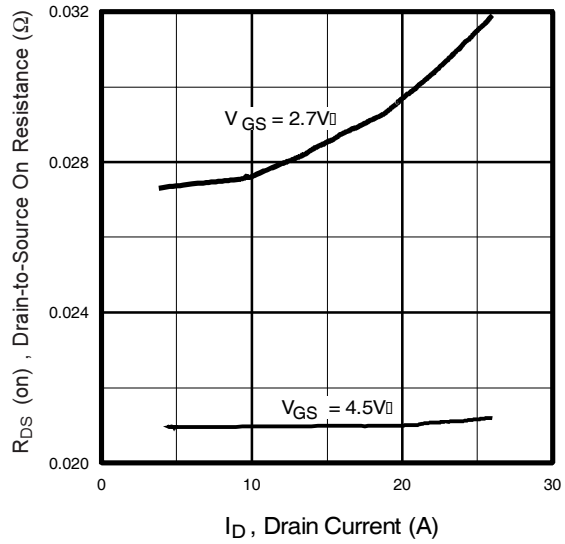


Fig 6. Typical On-Resistance Vs. Drain Current

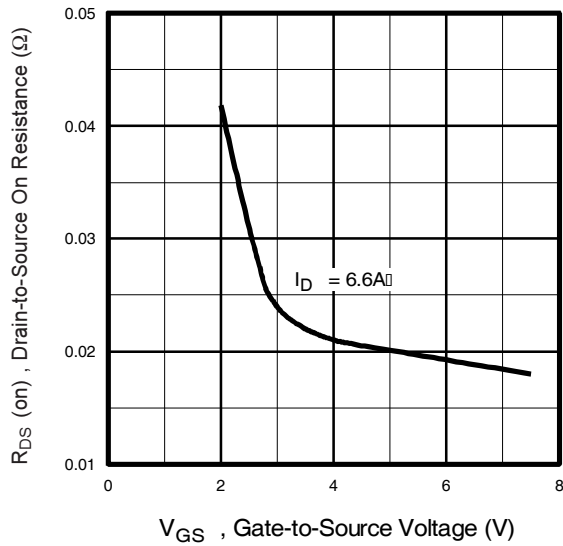


Fig 7. Typical On-Resistance Vs. Gate Voltage

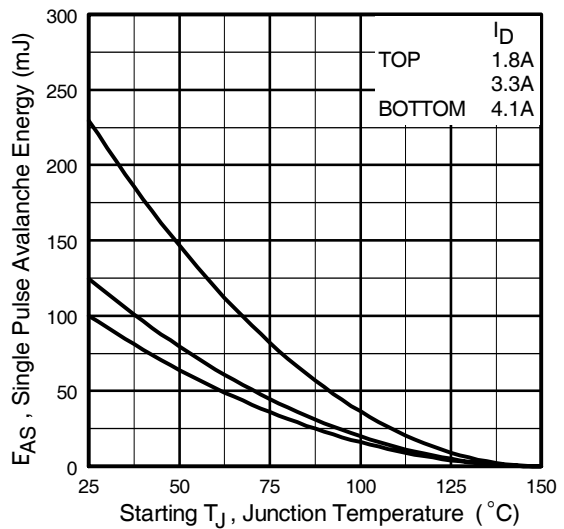


Fig 8. Maximum Avalanche Energy Vs. Drain Current

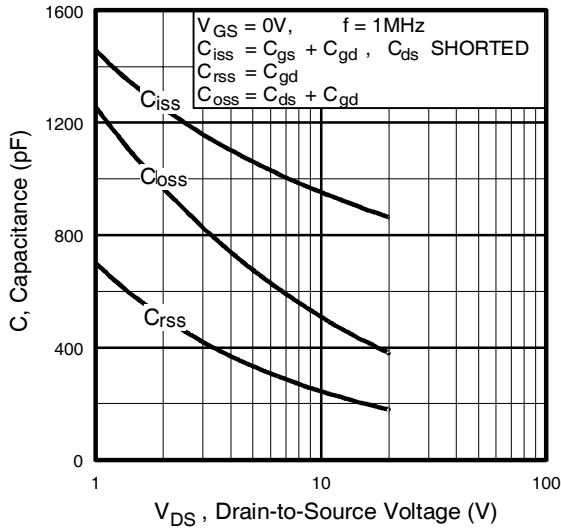


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

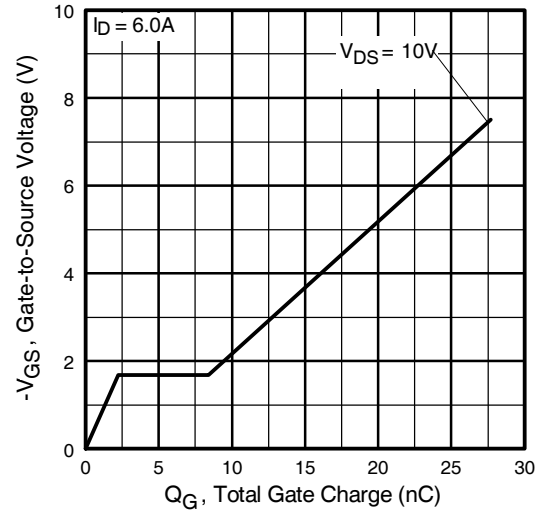


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

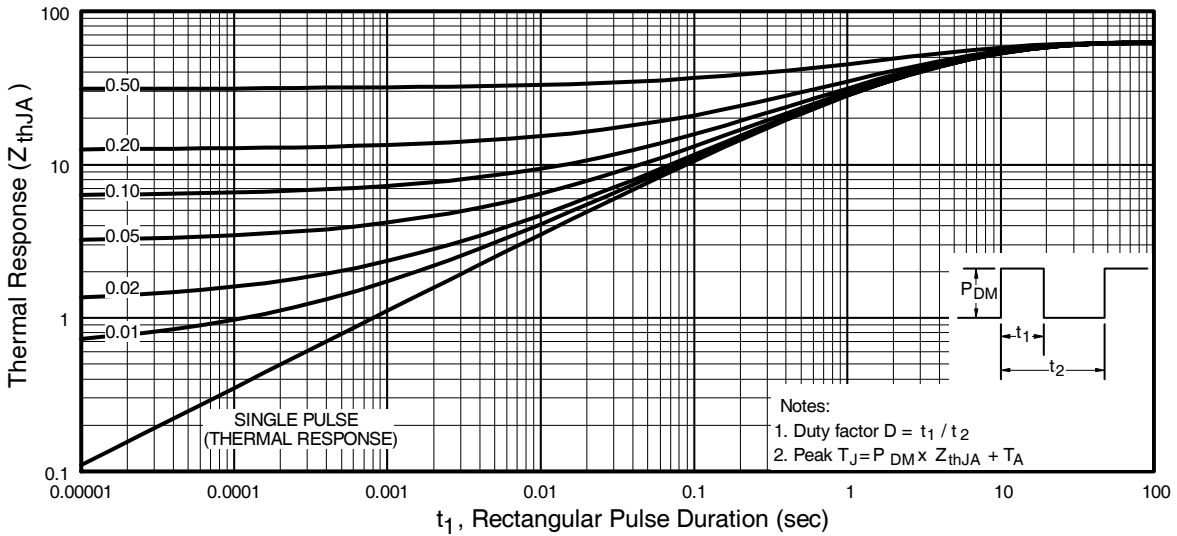


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

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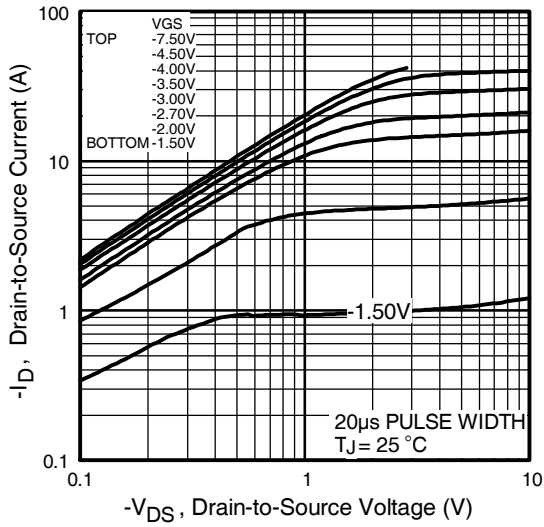


Fig 12. Typical Output Characteristics

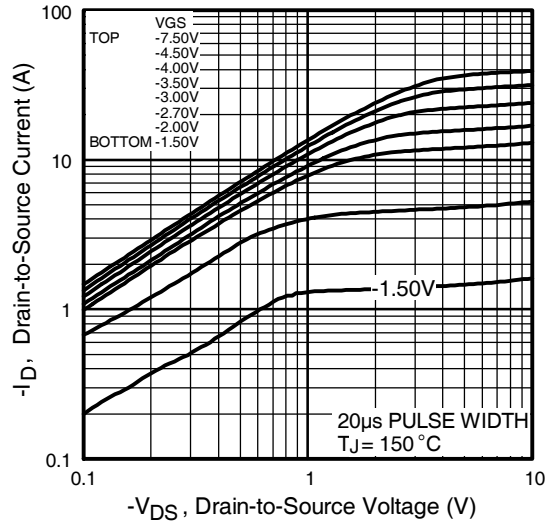


Fig 13. Typical Output Characteristics

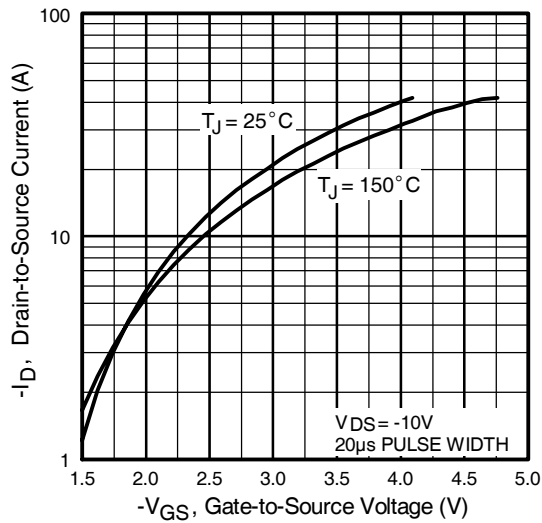


Fig 14. Typical Transfer Characteristics

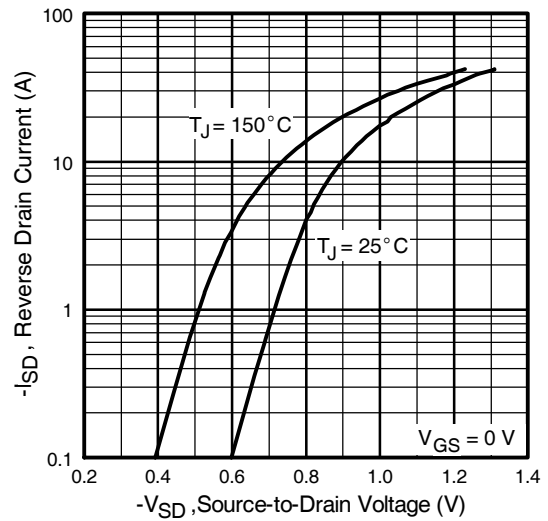


Fig 15. Typical Source-Drain Diode Forward Voltage

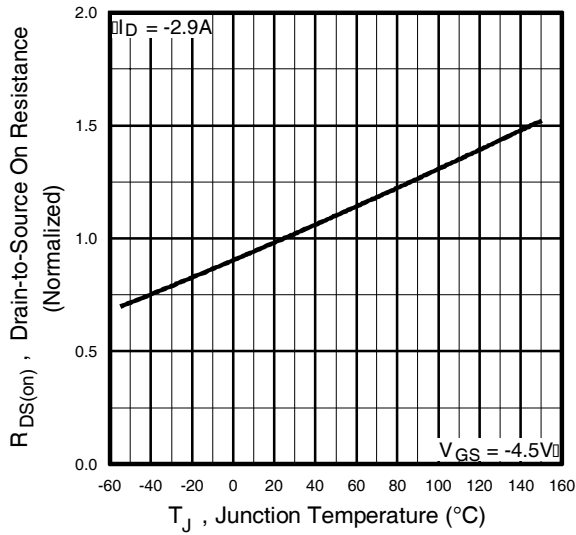


Fig 16. Normalized On-Resistance Vs. Temperature

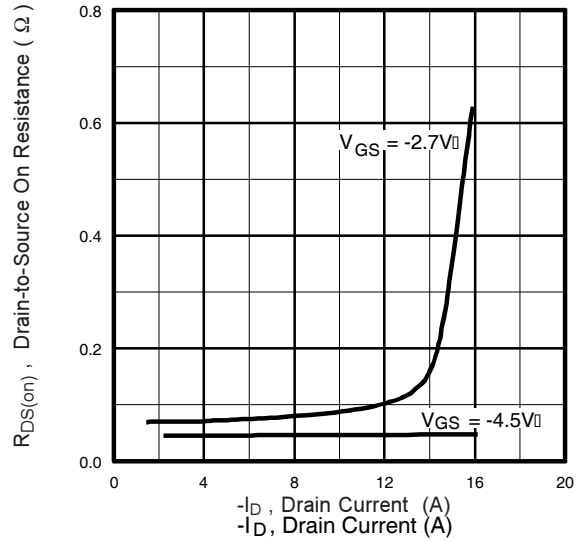


Fig 17. Typical On-Resistance Vs. Drain Current

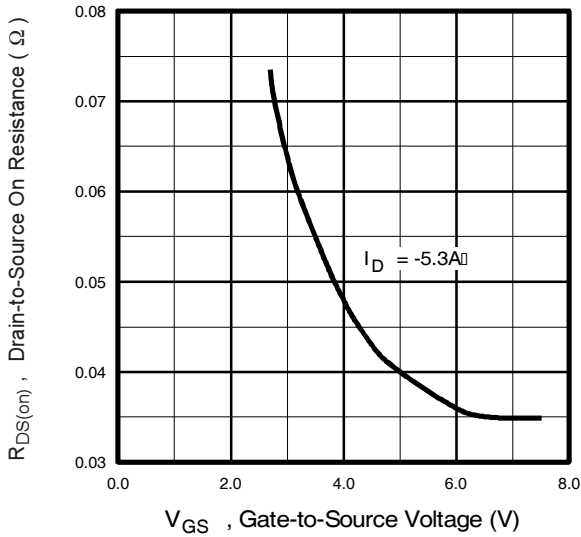


Fig 18. Typical On-Resistance Vs. Gate Voltage

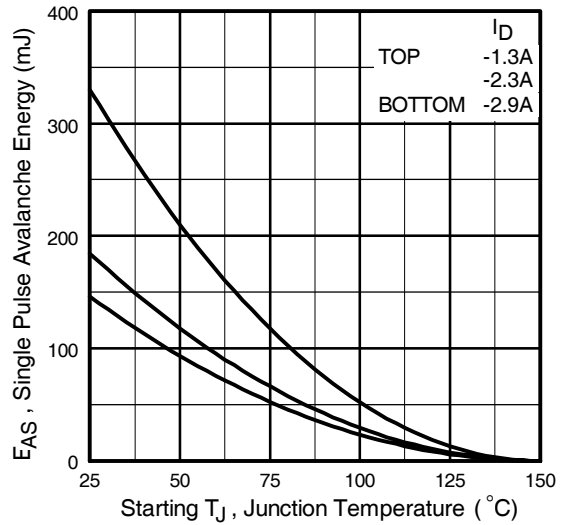


Fig 19. Maximum Avalanche Energy Vs. Drain Current

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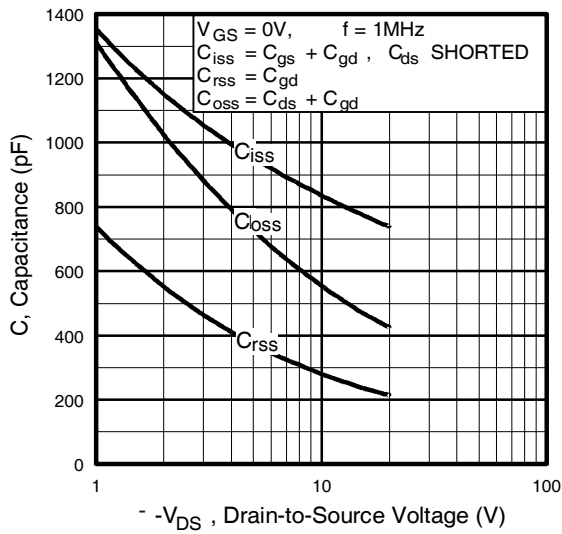


Fig 20. Typical Capacitance Vs. Drain-to-Source Voltage

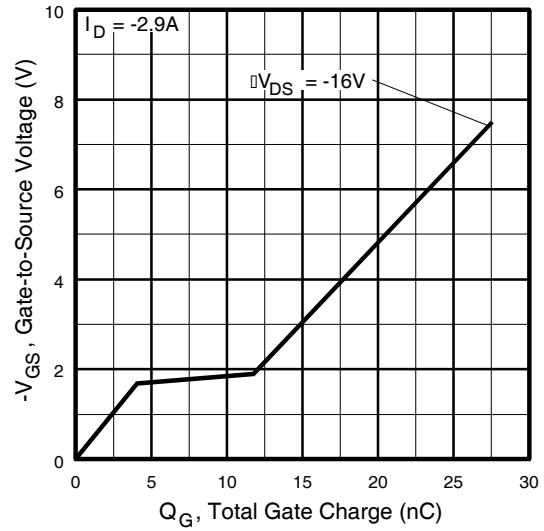


Fig 21. Typical Gate Charge Vs. Gate-to-Source Voltage

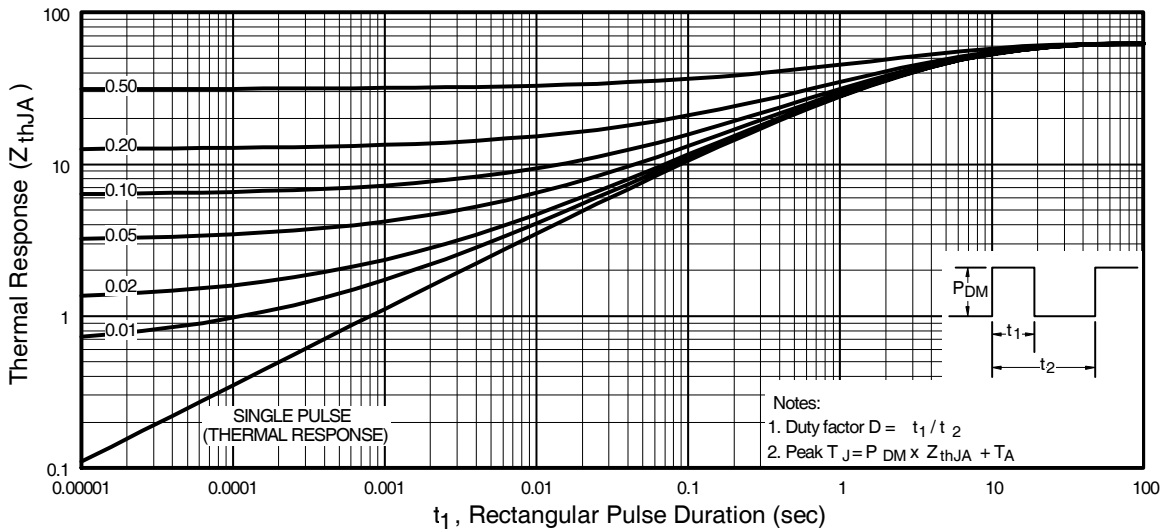
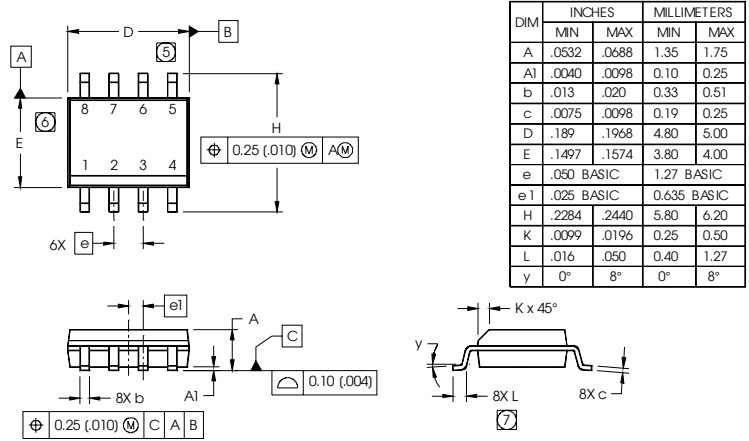


Fig 22. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

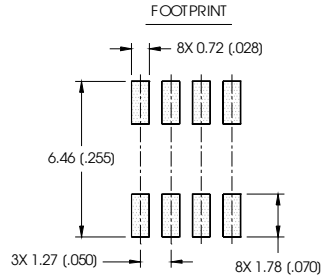
SO-8 Package Outline

Dimensions are shown in millimeters (inches)



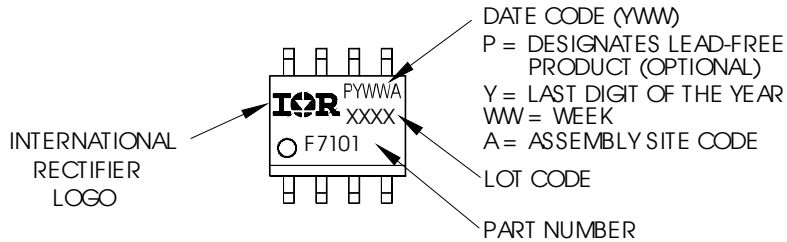
NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
- ⑤ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 (.006).
- ⑥ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.010).
- ⑦ DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.



SO-8 Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF7101 (MOSFET)

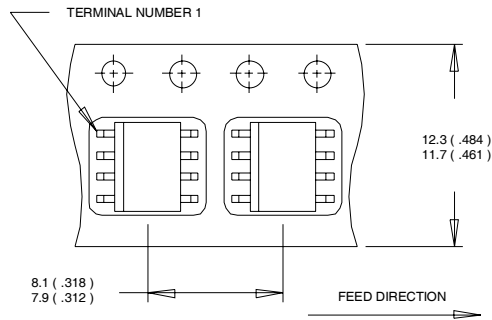


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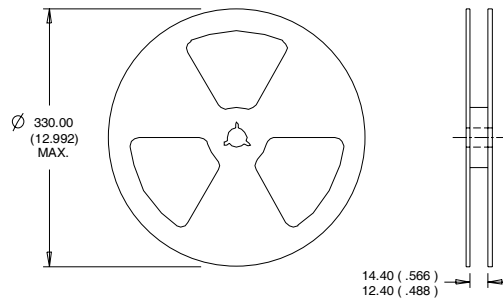
SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

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TAC Fax: (310) 252-7903

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