

IRF3315PbF

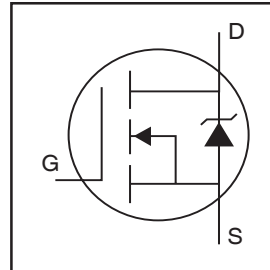
HEXFET® Power MOSFET

- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Lead-Free

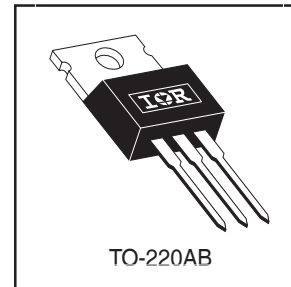
Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



$V_{DS} = 150V$
$R_{DS(on)} = 0.070\Omega$
$I_D = 23A$



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	23	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	16	
I_{DM}	Pulsed Drain Current ①	84	
$P_D @ T_C = 25^\circ C$	Power Dissipation	94	W
	Linear Derating Factor	0.63	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	350	mJ
I_{AR}	Avalanche Current③	12	A
E_{AR}	Repetitive Avalanche Energy④	9.4	mJ
dv/dt	Peak Diode Recovery dv/dt ⑤	2.5	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

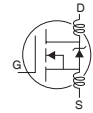
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.6	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.187	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.070	Ω	$V_{GS} = 10V, I_D = 12A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	17	—	—	S	$V_{DS} = 50V, I_D = 12A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 150V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 120V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	—	95	nC	$I_D = 12A$
Q_{gs}	Gate-to-Source Charge	—	—	11		$V_{DS} = 120V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	47		$V_{GS} = 10V$, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	9.6	—	ns	$V_{DD} = 75V$
t_r	Rise Time	—	32	—		$I_D = 12A$
$t_{d(off)}$	Turn-Off Delay Time	—	49	—		$R_G = 5.1\Omega$
t_f	Fall Time	—	38	—		$R_D = 5.9\Omega$, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1300	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	300	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	160	—		$f = 1.0\text{MHz}$, See Fig. 5



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	23	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	84		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 12A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	174	260	ns	$T_J = 25^\circ\text{C}, I_F = 12A$
Q_{rr}	Reverse Recovery Charge	—	1.2	1.7	μC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting $T_J = 25^\circ\text{C}$, $L = 4.9\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 12A$. (See Figure 12)

③ $I_{SD} \leq 12A$, $di/dt \leq 140A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$

④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

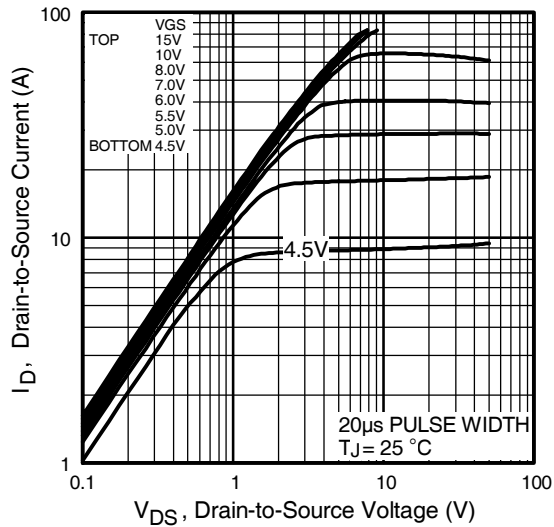


Fig 1. Typical Output Characteristics

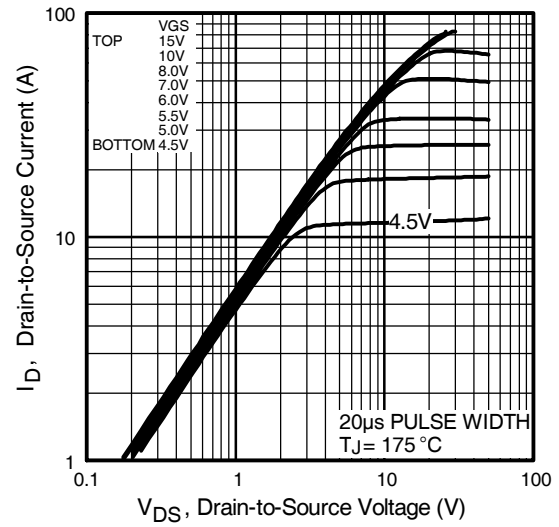


Fig 2. Typical Output Characteristics

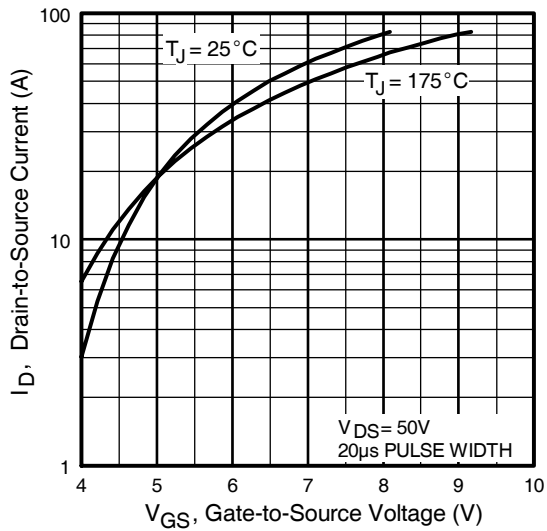


Fig 3. Typical Transfer Characteristics

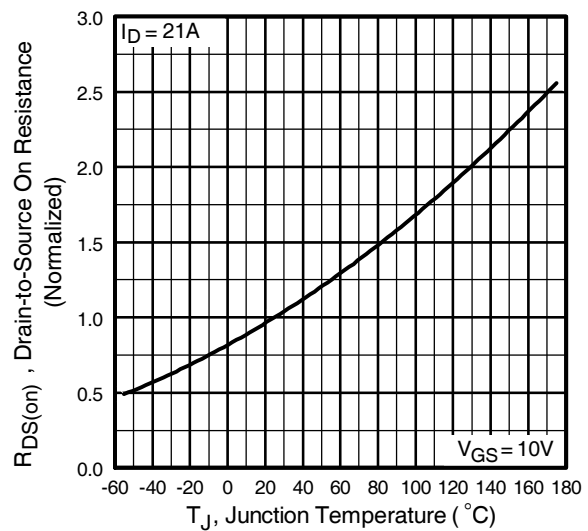


Fig 4. Normalized On-Resistance Vs. Temperature

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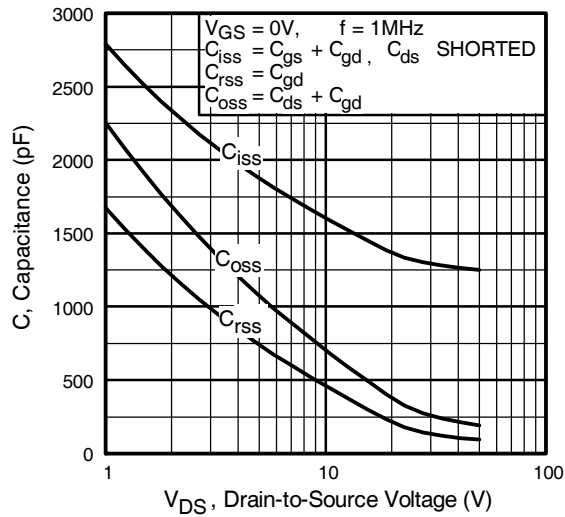


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

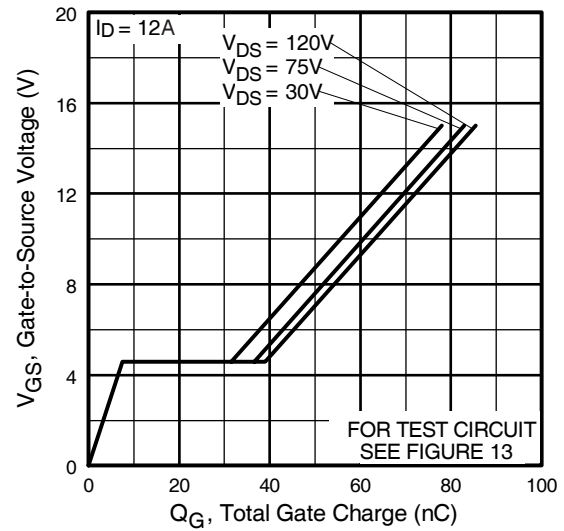


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

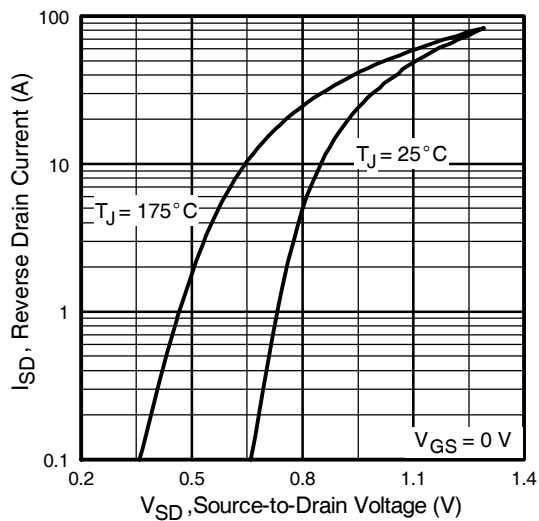


Fig 7. Typical Source-Drain Diode Forward Voltage

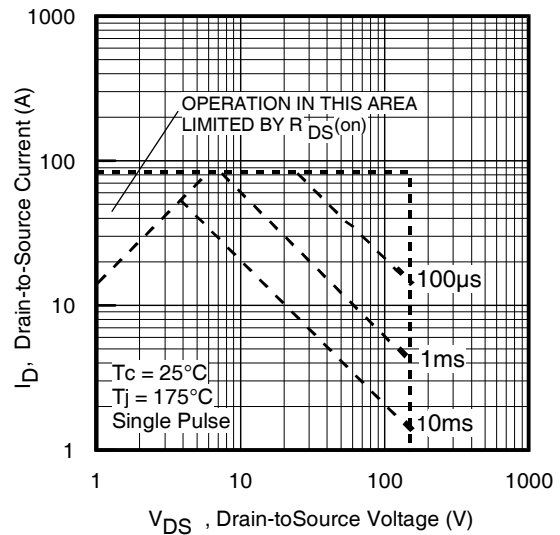


Fig 8. Maximum Safe Operating Area

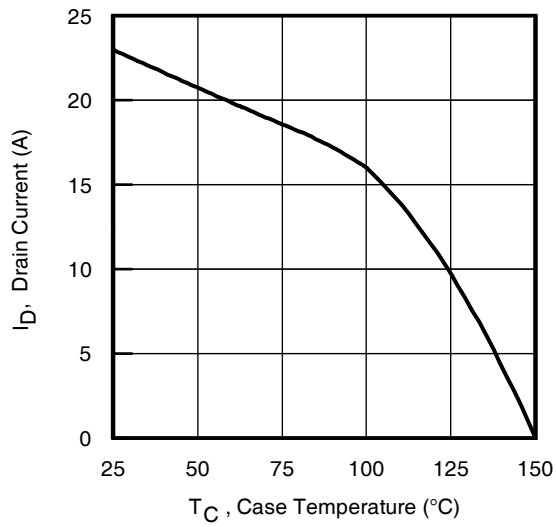


Fig 9. Maximum Drain Current Vs. Case Temperature

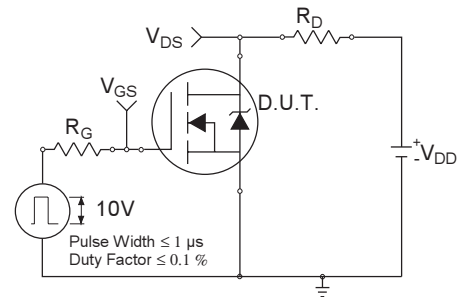


Fig 10a. Switching Time Test Circuit

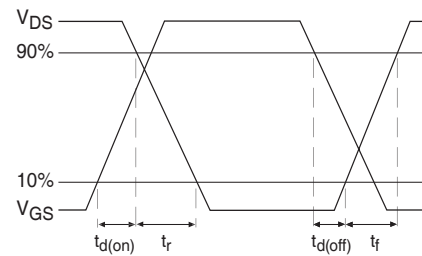


Fig 10b. Switching Time Waveforms

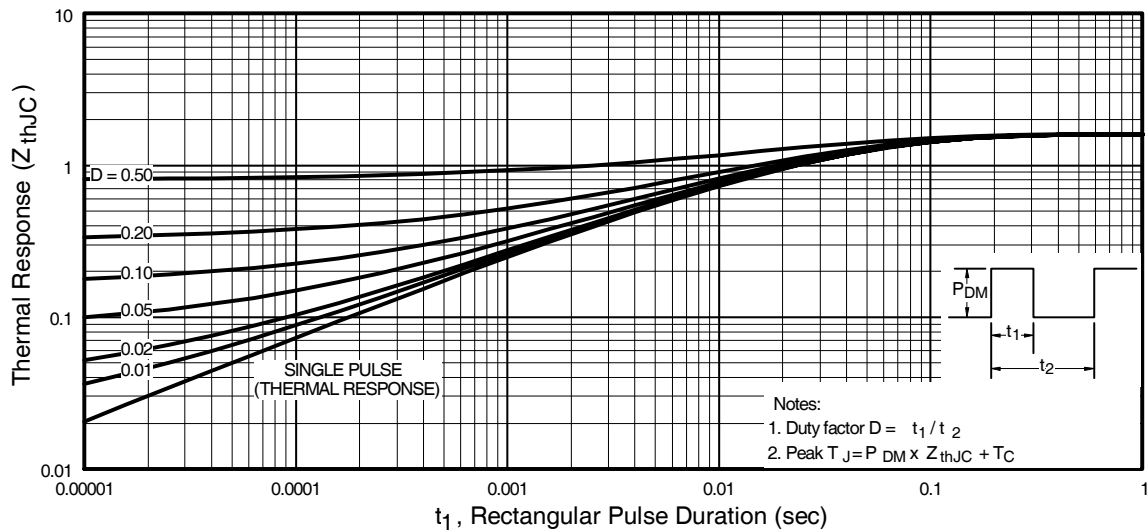


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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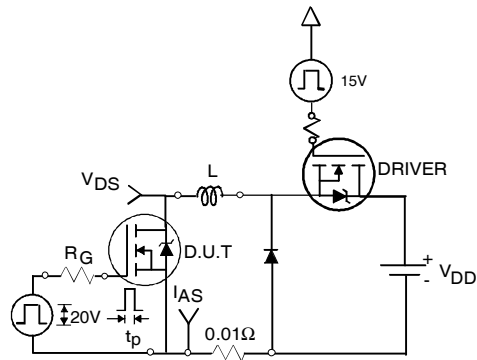


Fig 12a. Unclamped Inductive Test Circuit

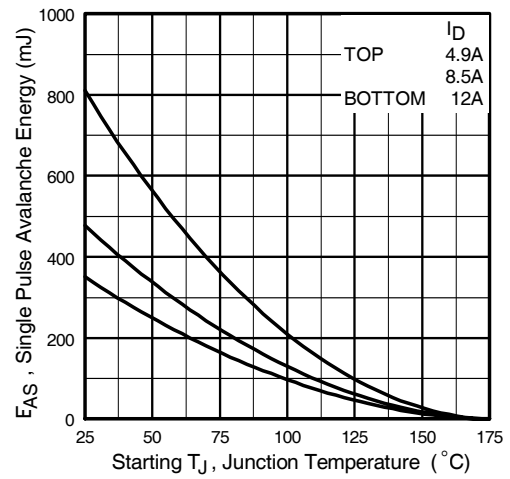


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

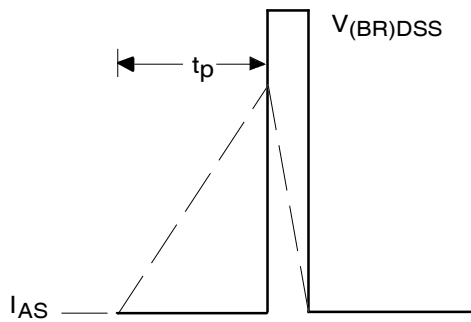


Fig 12b. Unclamped Inductive Waveforms

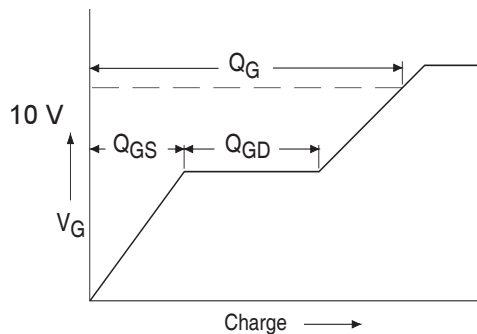


Fig 13a. Basic Gate Charge Waveform

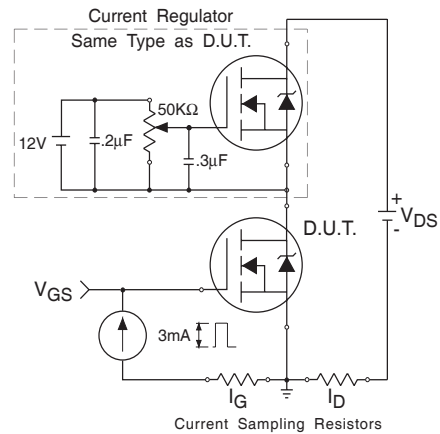
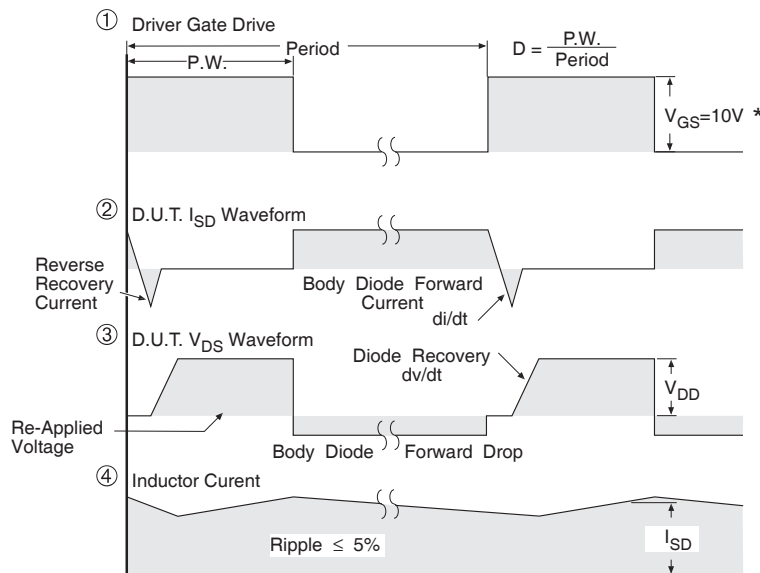
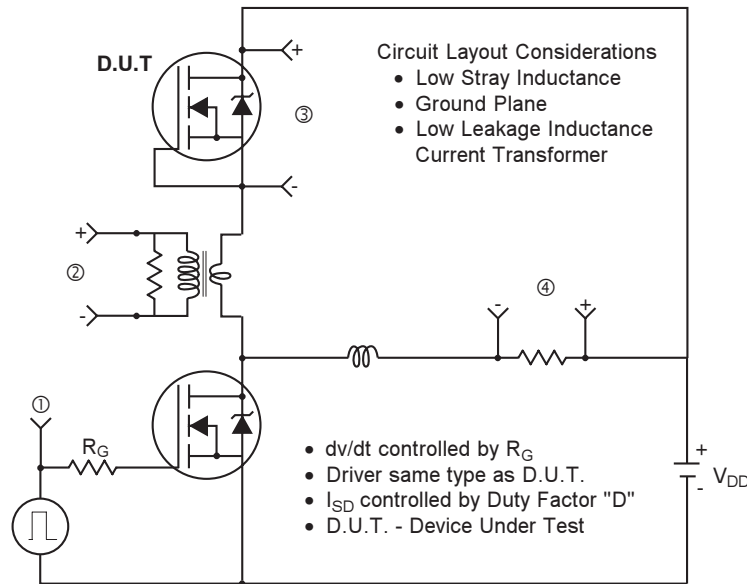


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

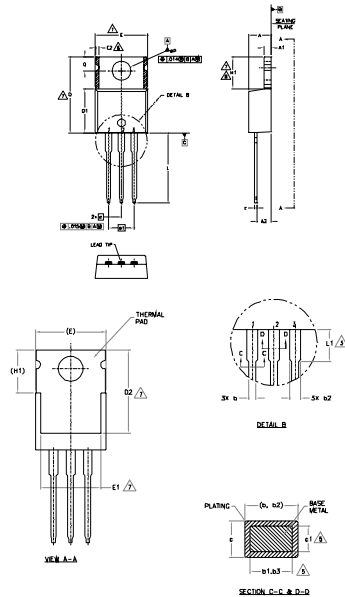
Fig 14. For N-Channel HEXFETS

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TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M-1994.
 - 2- DIMENSIONS ARE SHOWN IN INCHES (MILLIMETERS).
 - 3- LEAD DIMENSION AND PITCH UNCONTROLLED IN U.S.
 - 4- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
 - 5- CONTROLLING DIMENSION: INCHES.
 - 6- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E1, D2 & E1.
 - 7- DIMENSION E2 IS IN SETTING A ZONE. WHEN STAMPING AND SOLDERING IRREGULARITIES ARE ALLOWED.
 - 8- OUTLINE CONFORMS TO JEDEC TO-220 EXCEPT A2 (max.) AND D2 (min.).
 - 9- DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	5
b1	0.38	0.97	.015	.038	
b2	1.54	1.78	.045	.070	5
b3	1.54	1.73	.045	.068	
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.35	6.88	.250	.300	7
E2		0.76		.030	8
e	2.54		.100 BSC		
ef	5.08		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	5.56	4.06	.140	.160	3
MP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

LEAD ASSIGNMENTS

- 1- GATE
2- DRAIN
3- SOURCE

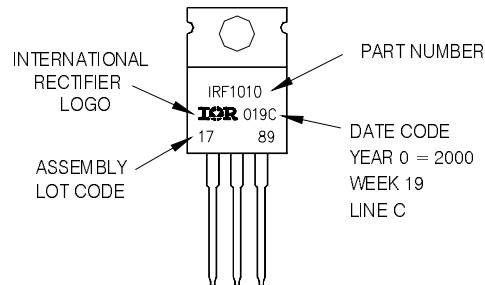
ORIENT. CHIPS

- 1- GATE
2- DRAIN
3- SOURCE

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 2000
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position
indicates "Lead - Free"



TO-220AB package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.

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