

IRF1312PbF
IRF1312SPbF
IRF1312LPbF
HEXFET® Power MOSFET

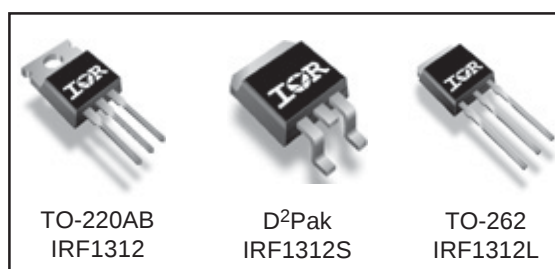
Applications

- High frequency DC-DC converters
- Motor Control
- Uninterruptible Power Supplies
- Lead-Free

V_{DSS}	$R_{DS(on)}$ max	I_D
80V	10m Ω	95A ^⑥

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	95 ^⑥	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	67 ^⑥	
I_{DM}	Pulsed Drain Current ^①	380	
P_D @ $T_A = 25^\circ\text{C}$	Power Dissipation ^③	3.8	W
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	210	
	Linear Derating Factor	1.4	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt ^③	5.1	V/ns
T_J	Operating Junction and	-55 to + 175	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	$^\circ\text{C/W}$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface ^⑦	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient ^②	—	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB mount) ^⑧	—	40	

Notes ^① through ^⑧ are on page 11

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	80	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.078	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	6.6	10	m Ω	$V_{GS} = 10V, I_D = 57A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.5	—	5.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 76V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 64V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	92	—	—	S	$V_{DS} = 25V, I_D = 57A$
Q_g	Total Gate Charge	—	93	140	nC	$I_D = 57A$
Q_{gs}	Gate-to-Source Charge	—	36	—		$V_{DS} = 40V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	34	—		$V_{GS} = 10V$, ④
$t_{d(on)}$	Turn-On Delay Time	—	25	—	ns	$V_{DD} = 40V$
t_r	Rise Time	—	130	—		$I_D = 57A$
$t_{d(off)}$	Turn-Off Delay Time	—	47	—		$R_G = 4.5\Omega$
t_f	Fall Time	—	51	—		$V_{GS} = 10V$ ④
C_{iss}	Input Capacitance	—	5450	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	550	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	340	—		$f = 1.0MHz$
C_{oss}	Output Capacitance	—	1910	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
C_{oss}	Output Capacitance	—	380	—		$V_{GS} = 0V, V_{DS} = 64V, f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	620	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 64V$ ⑤

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②⑥	—	250	mJ
I_{AR}	Avalanche Current①	—	57	A
E_{AR}	Repetitive Avalanche Energy①	—	21	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	95⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①⑥	—	—	380		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 57A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	64	96	ns	$T_J = 25^\circ\text{C}, I_F = 57A$
Q_{rr}	Reverse Recovery Charge	—	150	230	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

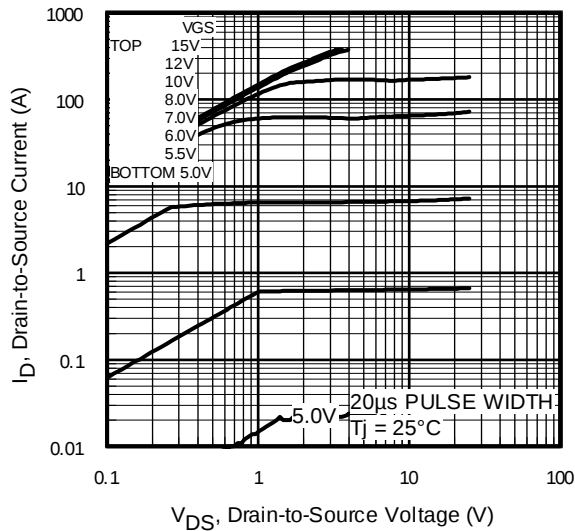


Fig 1. Typical Output Characteristics

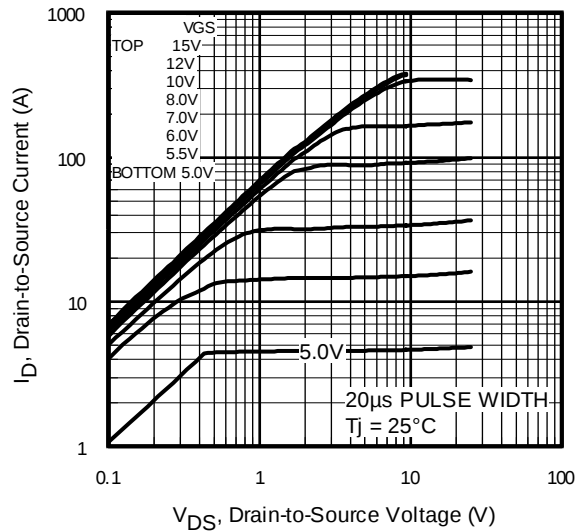


Fig 2. Typical Output Characteristics

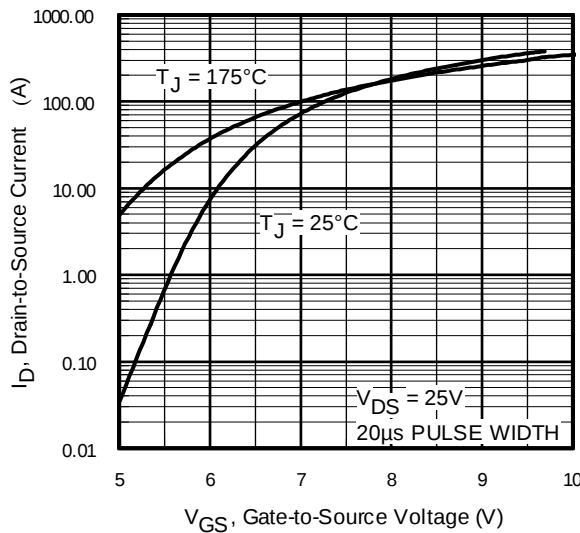


Fig 3. Typical Transfer Characteristics

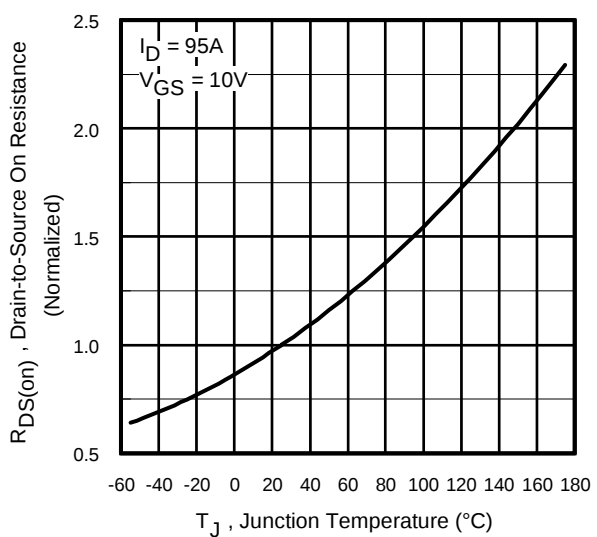
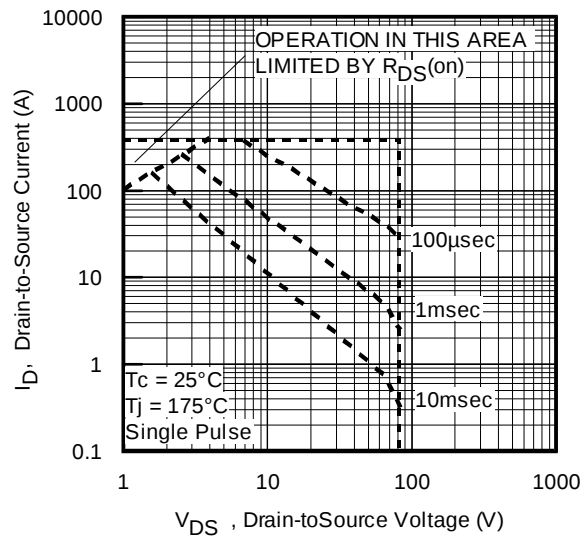
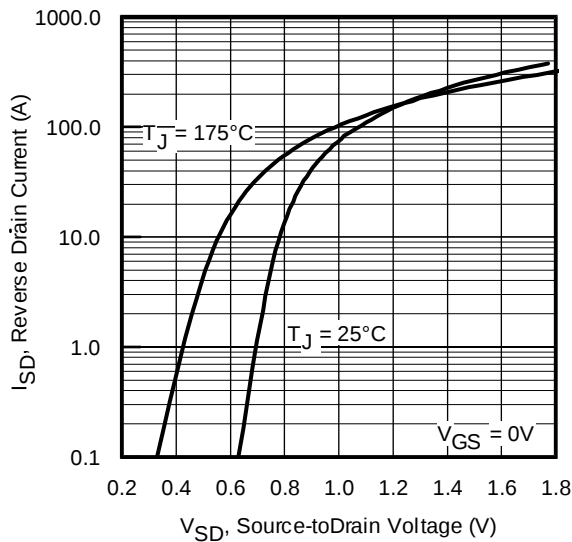
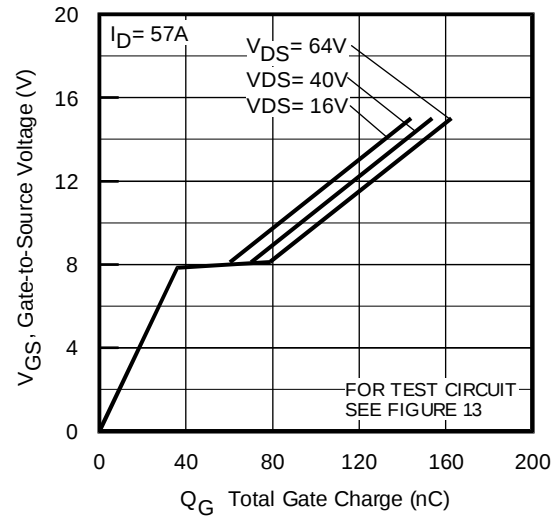
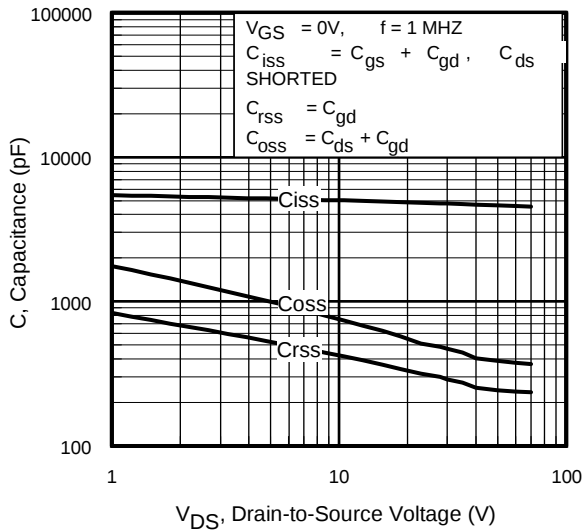


Fig 4. Normalized On-Resistance Vs. Temperature

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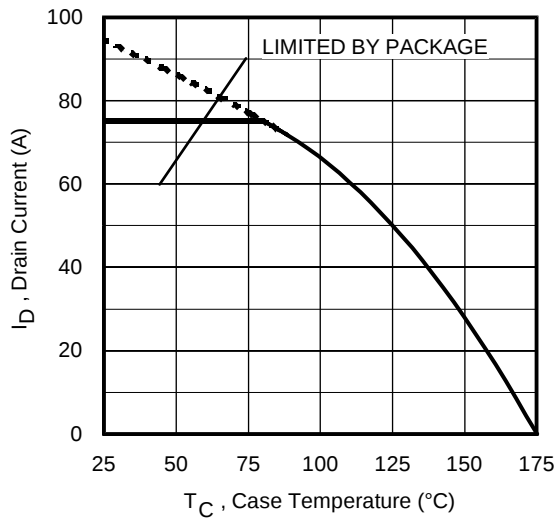


Fig 9. Maximum Drain Current Vs. Case Temperature

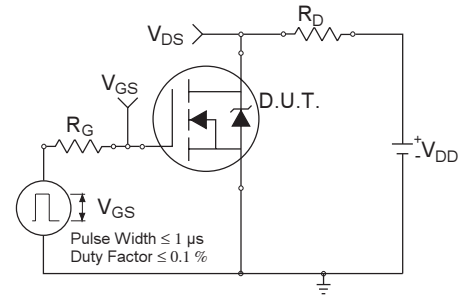


Fig 10a. Switching Time Test Circuit

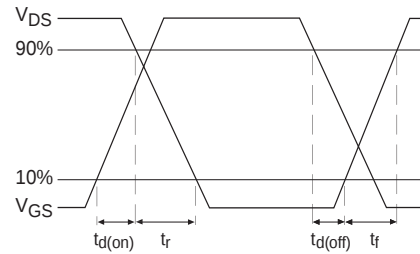


Fig 10b. Switching Time Waveforms

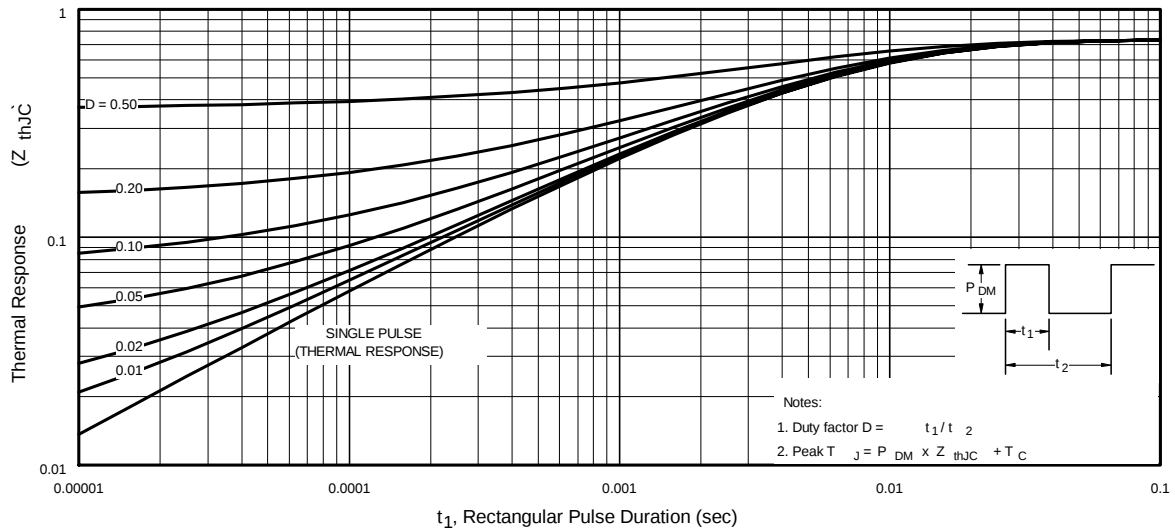


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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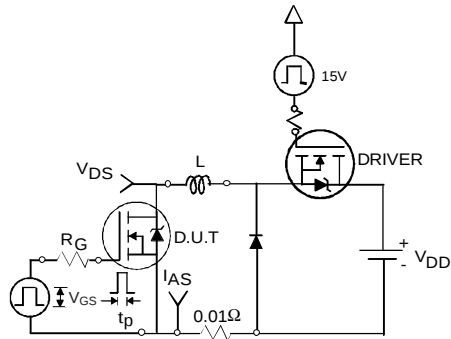


Fig 12a. Unclamped Inductive Test Circuit

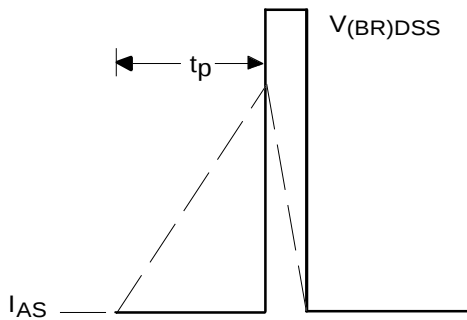


Fig 12b. Unclamped Inductive Waveforms

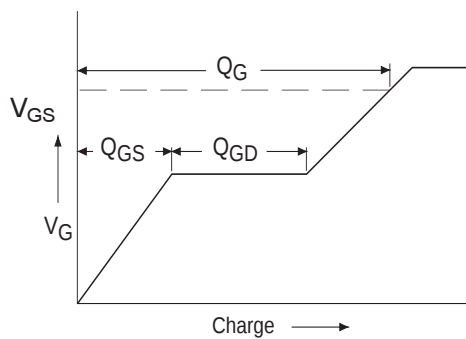


Fig 13a. Basic Gate Charge Waveform

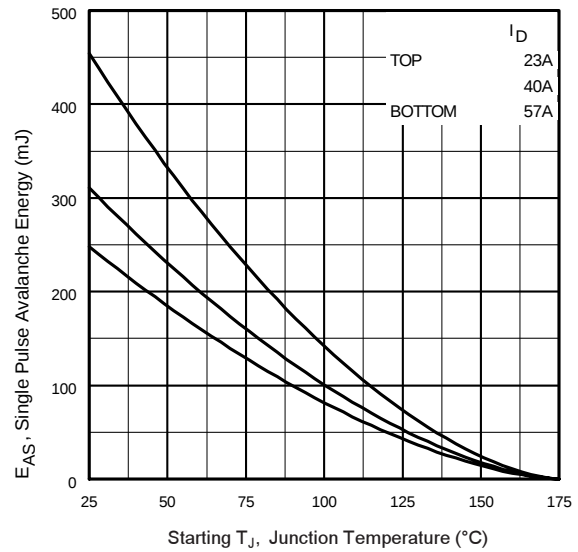


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

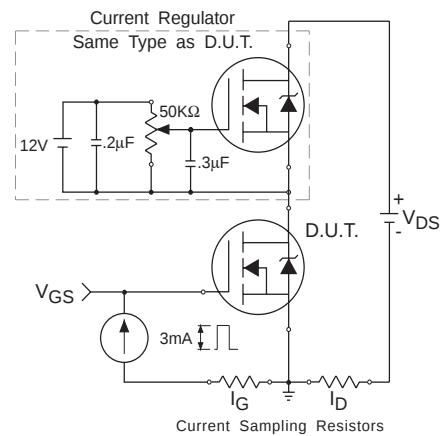


Fig 13b. Gate Charge Test Circuit

Circuit Diagram: The diagram shows a Class D MOSFET amplifier. The input stage consists of a MOSFET with its gate connected to a gate voltage source V_{GS} through a resistor R_G (callout 1). The gate is also connected to a transformer-coupled gate driver (callout 2). The output stage is a MOSFET (callout 3) whose drain is connected to a load (callout 4) and a supply voltage V_{DD} . The load is connected to ground through a resistor. The output of the load is connected to a load inductor (callout 4) and a load capacitor (callout 4). The output of the load is connected to a load inductor (callout 4) and a load capacitor (callout 4). The output of the load is connected to a load inductor (callout 4) and a load capacitor (callout 4).

Circuit Layout Considerations:

- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance

Annotations:

- dv/dt controlled by R_G
- I_{SD} controlled by Duty Factor "D"
- D.U.T. - Device Under Test

① Driver Gate Drive

P.W. Period

$D = \frac{\text{P.W.}}{\text{Period}}$

$[V_{GS}=10V]$ ***

② D.U.T. I_{SD} Waveform

Reverse Recovery Current

Body Diode Forward Current

di/dt

③ D.U.T. V_{DS} Waveform

Diode Recovery dv/dt

Re-Applied Voltage

Body Diode Forward Drop

$[V_{DD}]$

④ Inductor Current

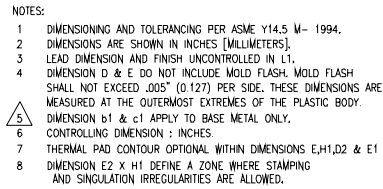
Ripple $\leq 5\%$

$[I_{SD}]$

Fig 14. For N-channel HEXFET® power MOSFETs

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Dimensions are shown in millimeters (inches)

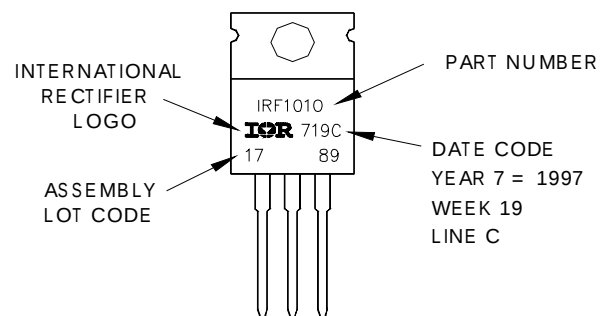


SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.82	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.04	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.96	.015	.038	5
b2	1.15	1.77	.045	.070	
b3	1.15	1.73	.045	.068	
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	12.19	12.88	.480	.507	7
E	9.66	10.66	.380	.420	4,7
E1	8.38	8.89	.330	.350	7
e	2.54 BSC		.100 BSC		
e1	5.08		.200 BSC		
H1	5.85	6.55	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	-	6.35	-	.250	3
ØP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	
ø	90°-95°		90°-95°		

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

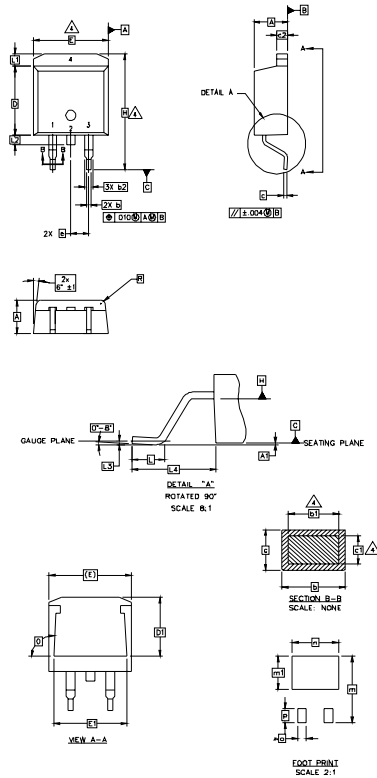
EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"



D²Pak Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	4
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	
D	8.51	9.65	.335	.380	3
D1	6.86		.270		3
E	9.65	10.67	.380	.420	
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	IGBTs, CoPACK
L	1.78	2.79	.070	.110	
L1		1.65		.065	
L2	1.27	1.78	.050	.070	
L3	0.25 BSC		.010 BSC		DIODES
L4	4.78	5.28	.188	.208	
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		1.- ANODE *
o	2.08		.082		
p	3.81		.150		
R	0.51	0.71	.020	.028	
θ	90°	93°	90°	93°	* PART DEPENDENT.

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2, 4.- DRAIN
- 3.- SOURCE

IGBTs, CoPACK

- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER

DIODES

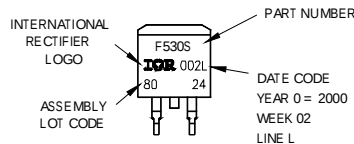
- 1.- ANODE *
- 2, 4.- CATHODE
- 3.- ANODE

* PART DEPENDENT.

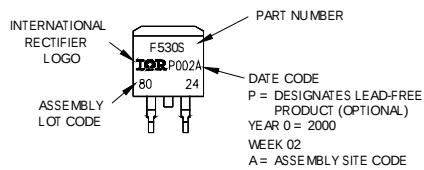
D²Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line
position indicates "Lead-Free"



OR

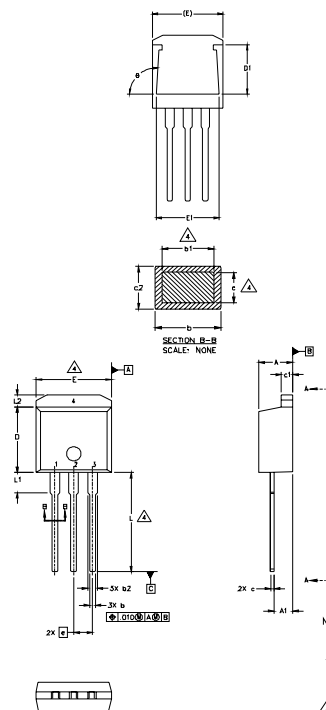


IRF1312/S/LPbF

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IR Rectifier

TO-262 Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.38	0.63	.015	.025	
c1	1.14	1.40	.045	.055	
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

LEAD ASSIGNMENTS

HEXFET

- 1. - GATE
- 2. - DRAIN
- 3. - SOURCE
- 4. - DRAIN

IGBT

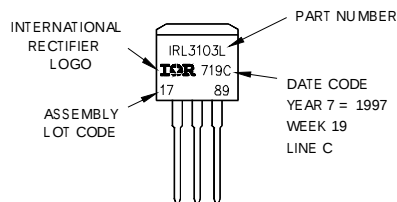
- 1 - GATE
- 2 - COLLECTOR
- 3 - EMITTER

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
 4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
 5. CONTROLLING DIMENSION: INCH.

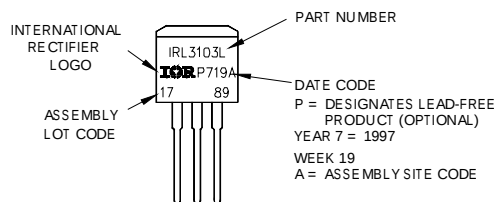
TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON VW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"

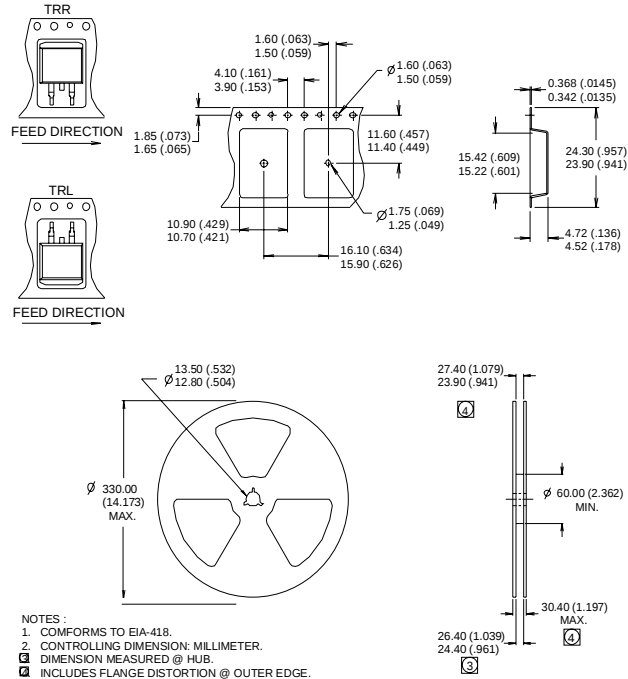


OR



D²Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.15\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 57\text{A}$. (See Figure 12)
- ③ $I_{SD} \leq 57\text{A}$, $di/dt \leq 410\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.
- ⑦ This is only applied to TO-220AB package
- ⑧ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

TO-220AB package is not recommended for Surface Mount Application

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information.12/04

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>