HMC976LP3E

400mA LOW NOISE, HIGH PSRR LINEAR VOLTAGE REGULATOR

Typical Applications

The HMC976LP3E is ideal for:

- Test Instrumentation
- Military Radios, Radar and ECM
- Basestation Infrastructure
- Ultra Low Noise Frequency Generation
- Fractional-N Synthesizer Supply
- Microwave VCO Supply
- Mixed-Signal Circuit Supply
- Low Noise Baseband Circuit Supply

Features

High Output Current: 400mA

Low Dropout: 300mV at 400mA Output and VR>3V

Ultra Low Noise: 3nV/√Hz at 10 kHz, 6nV/√Hz at 1 kHz

High Power Supply Rejection Ratio (PSRR):

<-60 dB at 1 kHz, <-30 dB at 1 MHz

Adjustable Voltage Output: VR 1.8 to 5V at 400mA

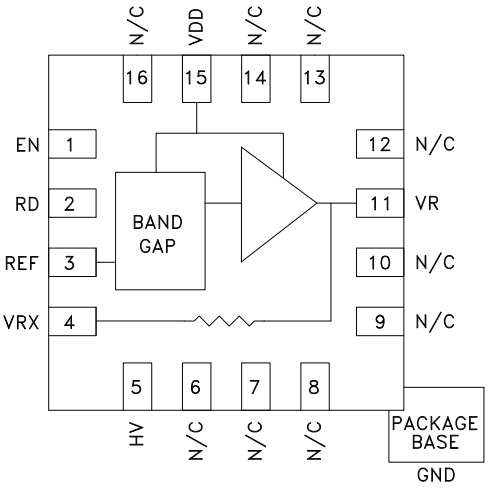
Designed to work with low ESR ceramic capacitors

Low Power-Down Current: <1 µA

Thermal Protection

16 Lead 3x3 mm SMT Package: 9mm²

Functional Diagram



General Description

The HMC976LP3E is a BiCMOS ultra low noise linear voltage regulator. The high Power Supply Rejection Ratio (PSRR) in the 0.1 MHz to 10 MHz range provides excellent rejection of any preceding switching regulator or other power supply noise. The voltage output is ideal for frequency generation subsystems including Hittite's broad line of PLLs with integrated VCOs.

The output voltage can be adjusted lower than the default value by using one external resistor. The output can be set to 5V by grounding the HV pin. The regulator can be powered down by the TTL-compatible Enable input. The HMC976LP3E is housed in a 3x3mm QFN SMT package.

Table 1. Electrical Specifications, T_A = +25 °C

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage VR (Default)	Vdd = 5.5V; Maximum load current	4.7	4.8	4.9	V
Output Voltage VR (5V setting)	Vdd = 5.5V; Maximum load current	4.9	5	5.1	V
Output Voltage Tolerance	Vdd = 5.5V; Maximum load current; Default and 5V setting			2	%
Input Voltage Range (Default)	Default output voltage configuration	5.1		5.5	V
Input Voltage Range	VR>3V[1] VDD>VR+0.3V	3.3		5.5	V
Input Voltage Range	VR<3V[1]	3.3		5.5	V

[1] See Absolute Maximum Ratings Table "Absolute Maximum Ratings"

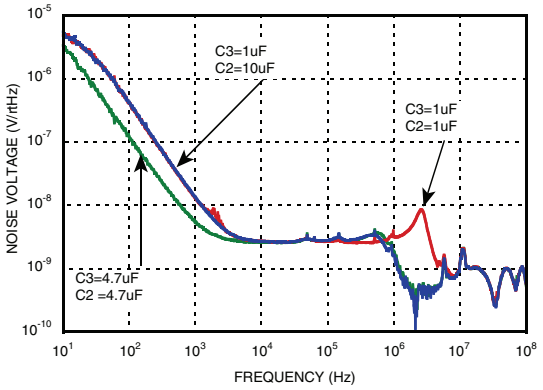
Table 1. Electrical Specifications (Continued)

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage Range VR	Set by external resistors.	1.8		5.1	V
Reference Voltage VREF	Vdd = 5.5V; REF cannot source/sink external current		1.17		V
Output Current VR [1]	T_A = -40°C to +85°C			400	mA
Output Noise Spectral Density 10 Hz 100 Hz 1 kHz 10 kHz 100 kHz	Vdd = 5.5V; VR = 5.0V Measured on Application Schematic [3] Maximum Load Current		4000 120 6 3 3		nV/rtHz
Integrated Output Noise 100 Hz to 100 kHz	Vdd = 5.5V; VR = 5.0V [3]		1.5		µVrms
Load Regulation, VR	Vdd = 5.5V; VR=5.0V			0.01	% / mA
PSRR 1 kHz 10 kHz 100 kHz 1 MHz 10 MHz 50 MHz	Vdd = 5.5V; VR=5.0V Maximum load current		-70 -65 -45 -35 -30 -20		dB
Output Voltage Variation vs. Package Base Temperature 25°C to 85°C -40°C to 25°C	Vdd = 5.5V; VR=5.0V Maximum load current		 0.005 0.005	 0.01 0.01	 % / °C % / °C
Current Consumption (I_{GND})	Ven = Vdd = 5.5V; Maximum Load Current		1.1	1.5	mA
Power Down Current	Vdd = 5.5V; EN = Low; Output is floating (high - impedance) in Power-Down mode			1	µA
Start-Up Transient Time	0 to 90% of final voltage Vdd = 5.5V[3]			200	ms
Enable Input EN High Level	Vdd>=VEN	2		Vdd	V
Enable Input EN Low Level	Vdd>=VEN	0		0.8	V
Output Load Capacitance [2]	To guarantee stability, noise and PSRR performance [3]	4.7			µF
Thermal Protection Threshold Junction Temperature		115			°C
Thermal Protection Hysteresis			10		°C

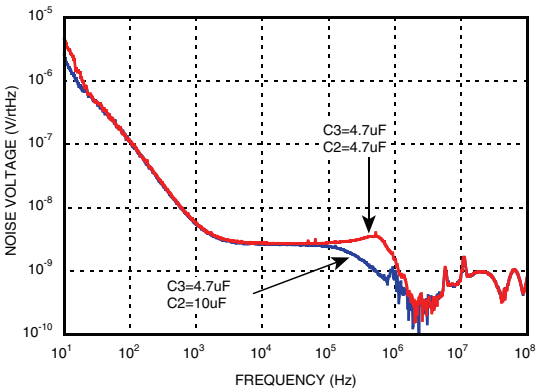
[1] The regulator does not include short-circuit protection circuitry. The outputs will withstand short-circuit conditions for a duration <10s.
[2] HMC976LP3E was designed to work with low ESR ceramic capacitors connected to pin 4 VRX.
[3] See HMC976LP3E 5.0V User Application Schematic herein

400mA LOW NOISE, HIGH PSRR LINEAR VOLTAGE REGULATOR

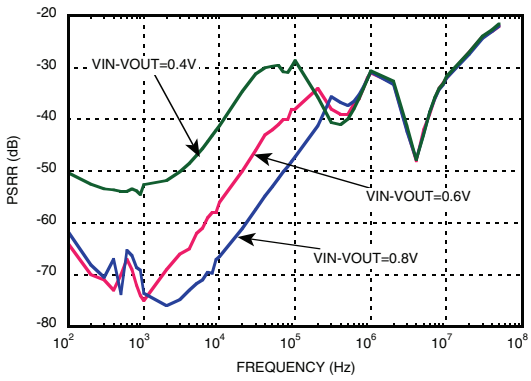
Vout=5V Output Noise Spectral Density [1]



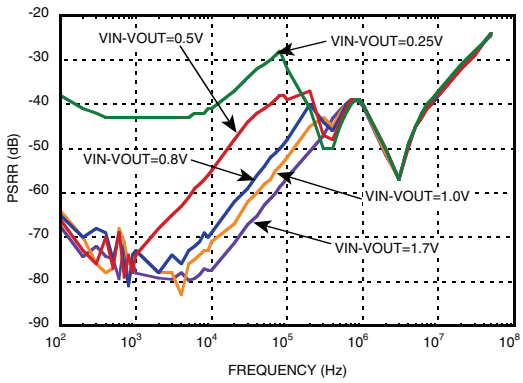
Vout=3.3V Output Noise Spectral Density [2]



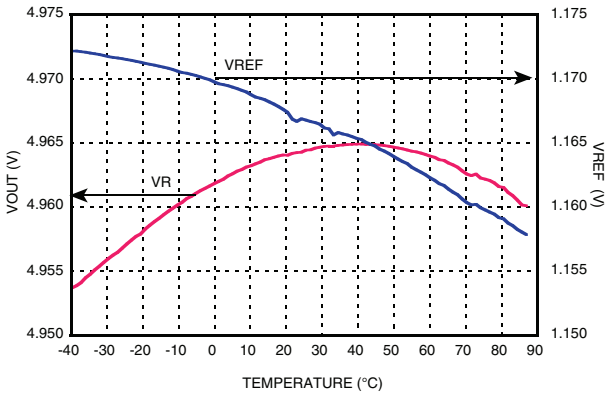
Vout 4.8V PSRR vs. Vin-Vout [3]



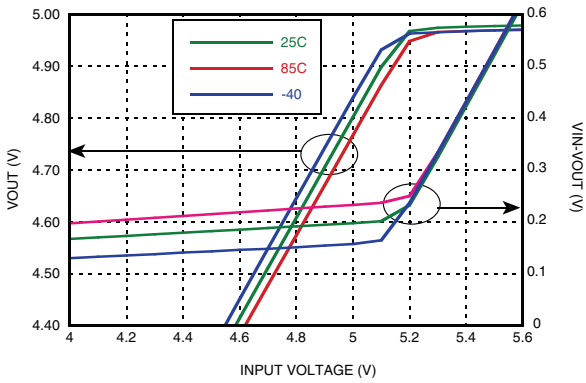
Vout=3.3V PSRR vs. Vin-Vout [2]



Vout and Vref vs. Temperature [1]

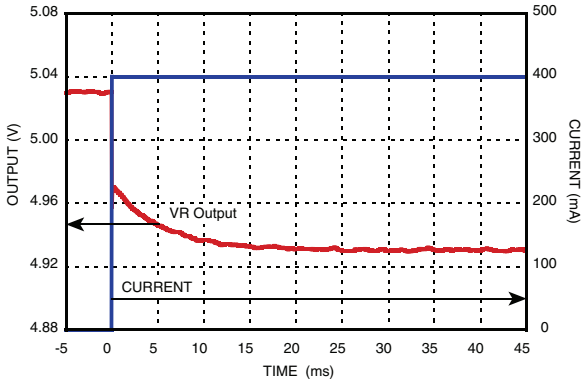


Vout vs. Vin vs. Temperature [1]

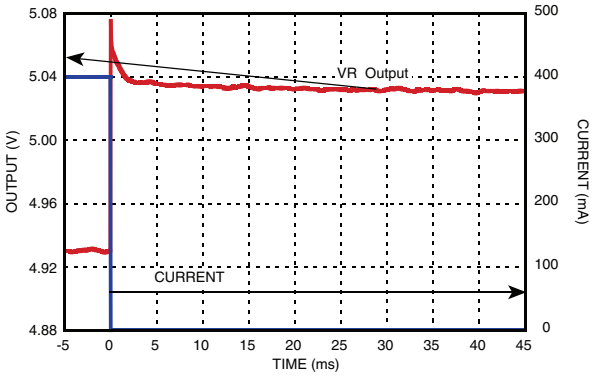


[1] VDD=5.5V,400mA Load see "HMC976LP3E 5V User Application Schematic".
[2] VDD=5.0V,400mA Load see "HMC976LP3E 3.3V User Application Schematic".
[3] VDD=5.5V,400mA Load see "HMC976LP3E 4.8V User Application Schematic".

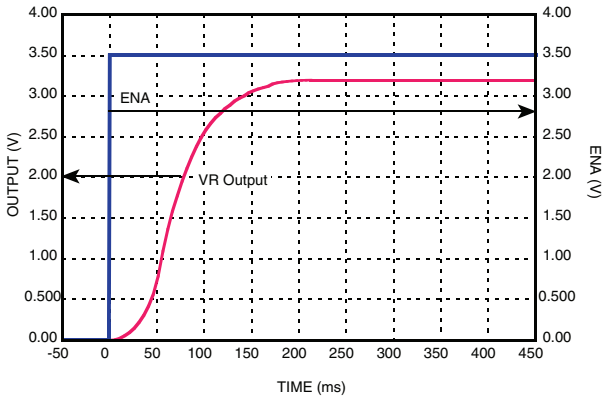
Output Load Switched OFF to ON [1]



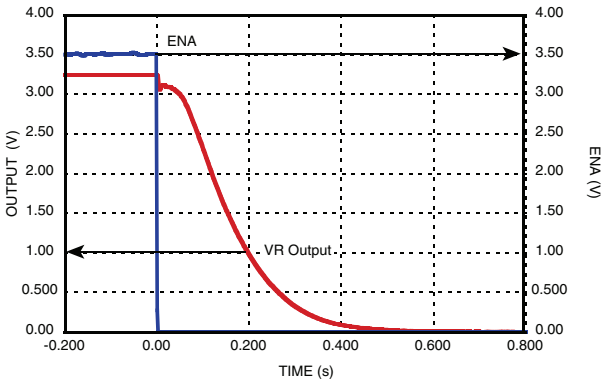
Output Load Switched ON to OFF [1]



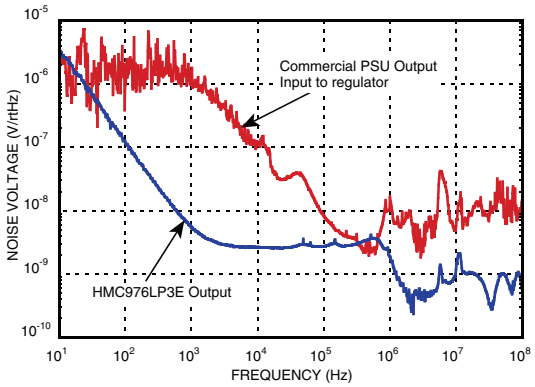
Supply Turn-On Transient [2]



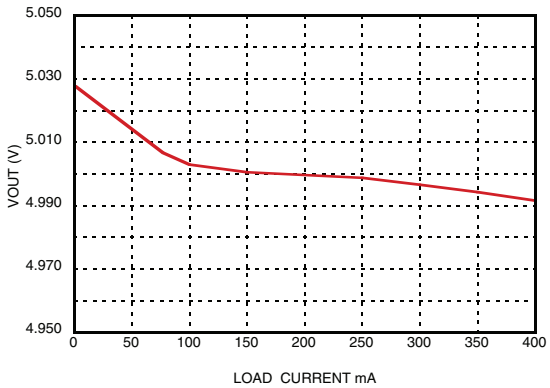
Supply Turn-Off Transient [2]



HMC976LP3E Output Noise Spectral Density vs. Commercial PSU [1]



Vout vs. Load current[1]



[1] VDD=5.5V, 400mA Load "HMC976LP3E 5V User Application Schematic".

[2] VDD=5.0V, 400mA Load "HMC976LP3E 3.3V User Application Schematic"

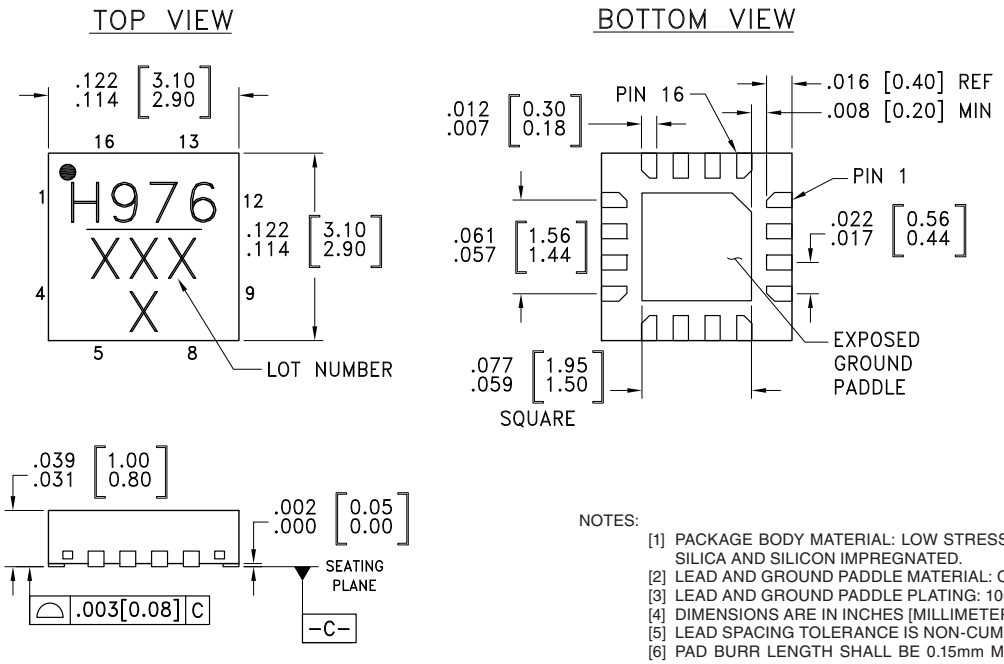
Table 2. Absolute Maximum Ratings

Vdd to GND Voltage	+5.8V / -0.3V
EN to GND Voltage	+5.8V /-0.3V
RDx / HVx to GND Voltage	+5.8V / -0.3V
Maximum Dissipation	780mW
Thermal Resistance (Junction to Ambient)	51.5 °C/W
Maximum Junction Temperature	+125 °C
Max Output Current	420 mA
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The absolute maximum ratings apply individually only, not in combination.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

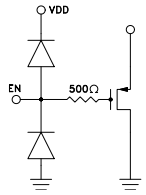
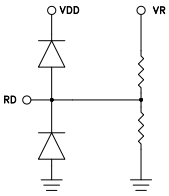
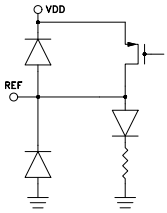
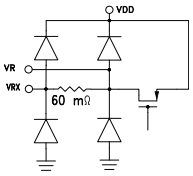
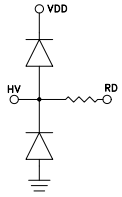
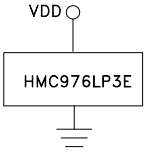
[1] PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
[2] LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
[3] LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
[4] DIMENSIONS ARE IN INCHES [MILLIMETERS].
[5] LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
[6] PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25m MAX.
[7] PACKAGE WARP SHALL NOT EXCEED 0.05mm
[8] ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB GROUND.
[9] REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Table 3. Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC976LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	976 XXX X

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

Table 4. Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	EN	Enable Input, TTL Logic Level. The VR and VRX outputs are floating (high impedance) when EN = Low.	
2	RD	Resistive feedback for VR, see “Output Voltage Adjust” section.	
3	REF	Reference voltage (bandgap) output. Cannot be used to source/sink current to/from external circuits	
4	VRX	For Decoupling Capacitor Cannot be used to source current to external circuits	
11	VR	Regulator Output VR 400mA	
5	HV	Sets VR to 5V output when grounded	
6 - 10, 12 - 14,16	N/C	These pins can be left unconnected or connected to GND with no change in performance	
15	VDD	Unregulated power supply input 5.5V max	
Package Base	GND	Must contact PCB ground	

Evaluation PCB

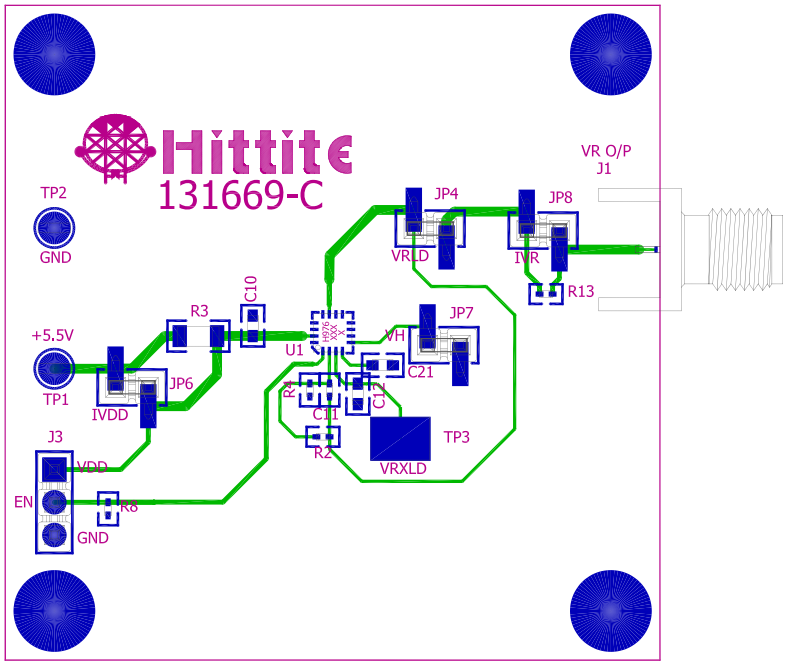


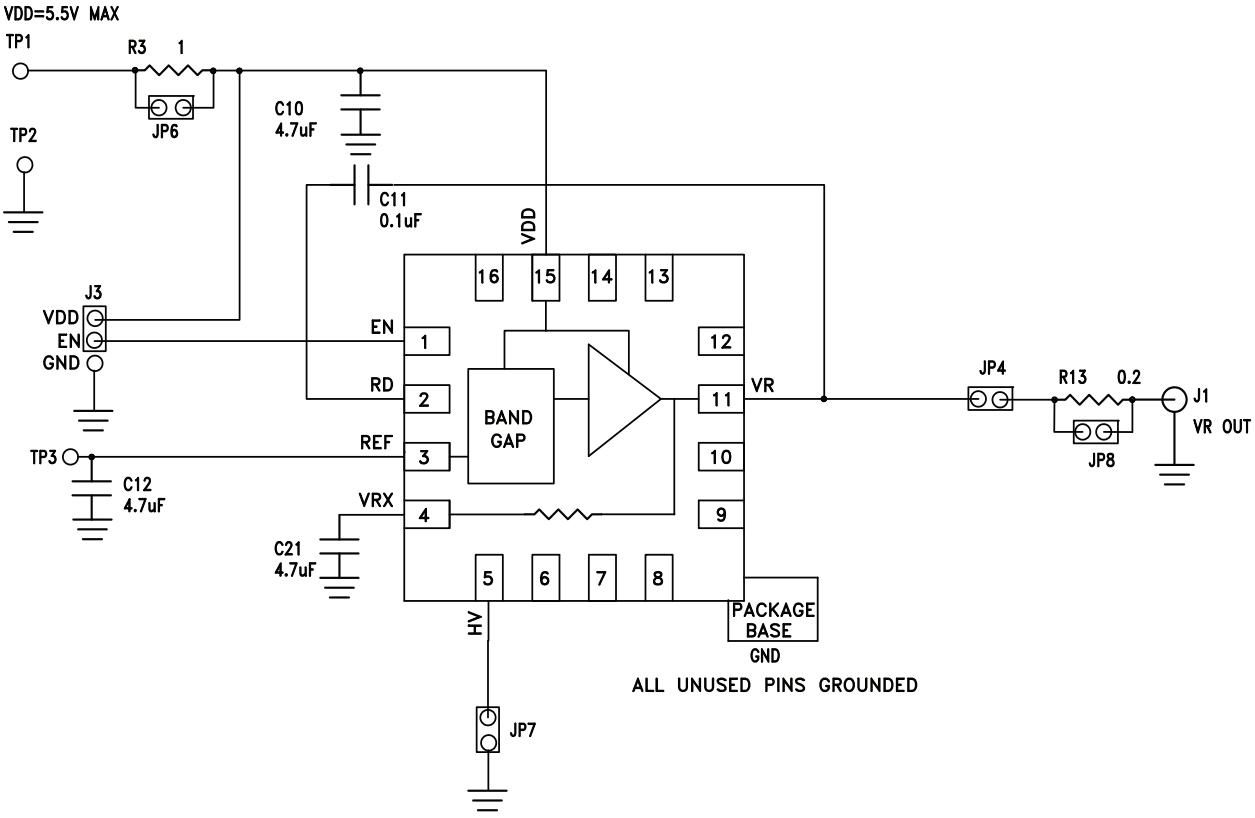
Table 5. Ordering Information

Item	Contents	Part Number
Evaluation PCB	HM976LP3E Evaluation PCB	131671-HMC976LP3E

Table 6. List of Materials for Evaluation PCB 131671

Item	Contents
J1	PCB Mount SMA connector
J3	3 Pin Header
JP4, JP6, JP7, JP8,	2 Pin Header and Jumper
C10, C12, C21	4.7µF Capacitor 0603 Pkg.
C11	0.1µF Capacitor 0402 Pkg.
R13	0.2 Ohm Resistor 0402 Pkg.
R3	1 Ohm Resistor 0402 Pkg.
R8	100 kOhm Resistor 0402 Pkg.
TP1, TP3	Test Point PC Compact Red
TP2	Test Point PC Compact Black
U1	HMC976LP3E 400mA Low Noise, High PSRR Linear Voltage Regulator
PCB	131669 Eval Board

Evaluation PCB Schematic



Operational Features

The recommended configuration is "HMC976LP3E 4.8V User Application Schematic". This is for the default output voltage of 4.8V nominal. The values shown are those recommended for optimum Noise Spectral density. For users requiring extremely low noise in the 1 MHz to 10 MHz range the largest capacitor possible should be used: a 68uF takes the noise between 100 kHz and 1 MHz to below 2.5nV/√Hz.

Load Capacitor Characteristics

The HMC976LP3E was designed to work with a low ESR ceramic load capacitor on the VRX pin (C21 in the schematic above). Low ESR ceramic capacitors are very small and best for eliminating high frequency noise. Ceramic capacitors can vary as much as 50% versus temperature and 60% versus voltage, dependant on the ceramic type e.g. Z5U, Y5V, X7R or X5R. There are no restrictions on ceramic type or minimum ESR, only that the user must guarantee that the minimum capacitance over operating conditions is 4.7µF, smaller values can result in noise peaking or lower stability.

Output Voltage Adjustment

The default output voltage is 4.8V this configuration "HMC976LP3E 4.8V User Application Schematic".

The output voltage can be set to 5V by a ground on HV pin 5 "HMC976LP3E 5V User Application Schematic".

The output voltage can be set from 1.8V to <4.8V by a resistor from pin 2 to the output pin 11 shown in "HMC976LP3E 3.3V User Application Schematic". The value of the resistor is given by the equation below.

$$R1 = \frac{\left(\left(\frac{Vout}{1.17}\right)-1\right)*18.9}{1-0.32*\left(\left(\frac{Vout}{1.17}\right)-1\right)}$$

If the temperature stability performance similar to that shown in the plot "Vout and Vref vs. Temperature [1]" is required, then any external resistor temperature coefficient is a critical parameter and should be better than 50ppm and 1% tolerance. Please note that the temperature coefficient of the internal resistor feedback divider is 270ppm/°C.

Layout of PCB

The layout of the PCB should follow these guide lines, the PADDLE should be grounded to the supply -VE terminal or ground with at least 5 vias directly under the paddle to the bottom side ground plane. To ensure the noise and PSRR specifications are met, the capacitors connecting to Pins 15, 11, 3 (see user application schematics), should be placed as close as possible to the relevant pin and the ground connection should be as short as possible. Trace widths and via sizes should be scaled to match the current drawn. The use of a large ground plane is recommended with a large number of ground vias near the device to carry the ground.

Thermal Protection

Under the HMC976LP3E default output voltage condition (Vout = 4.8V and maximum output current) the thermal protection circuitry limits the output current to approximately 500µA. When the ambient temperature rises to approximately +115°C. The output will be kept disabled, allowing to the regulator to cool down, until the ambient temperature decreases by approximately 10°C. The thermal protection may cycle the output on and off, protecting the regulator from damage, dependant on the power dissipation and ambient temperature. The thermal protection circuitry will act indirectly when a short circuit occurs at the output. After the overload or the fault condition is removed/changed, the regulator output will return to the nominal operation.

For reliable operation the "Absolute Maximum Ratings" must be complied with especially the maximum junction temperature must not be exceeded. The board copper ground area and thermal dissipation should be taken into account during board layout. The junction temperature for a given dissipation can be calculated from the equation below

$$T_j = T_a + \left(P_d \times \theta_{ja}\right)$$

Where Tj=Junction Temperature (°C), Ta=Ambient Temperature (°C), Pd=Dissipated Power (W), θja=Thermal Resistivity Junction to Ambient (°C/W).

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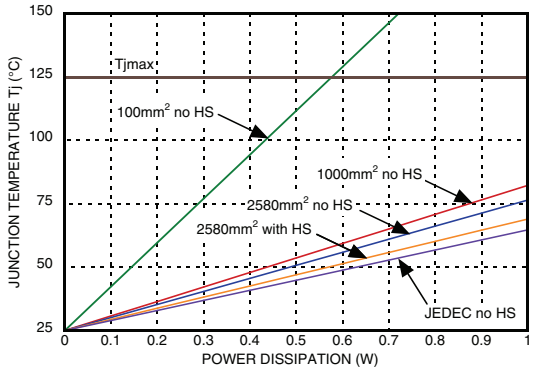
Application Support: apps@hittite.com

Thermal dissipation should be taken into account at all times especially with large VDD-VR values i.e. if 1.8V is required from 5.5V VIN then the output current must be restricted to <210mA , or VDD restricted to <3.75V for a 400mA load.

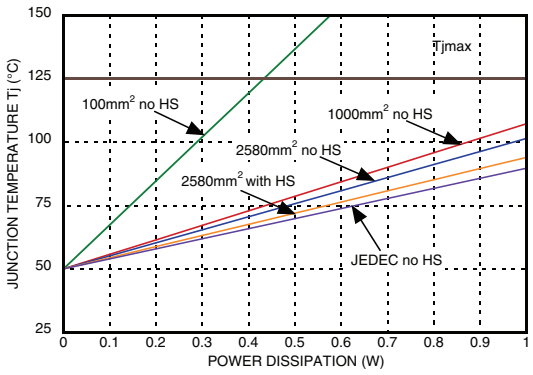
The following plots show the board ground copper area influence, on junction temperature for ambient temperatures of 25°C, 50°C, 85°C vs. Total power dissipated in the device. The conditions for the plots are :

1. 100mm² Copper Area
2. 1000mm² Copper Area
3. 2580mm² Copper Area HMC976LP3E Evaluation PCB No Heat Sink
4. 2580mm² Copper Area HMC976LP3E Evaluation PCB with Heat Sink
5. JEDEC Board as per JESD51-3

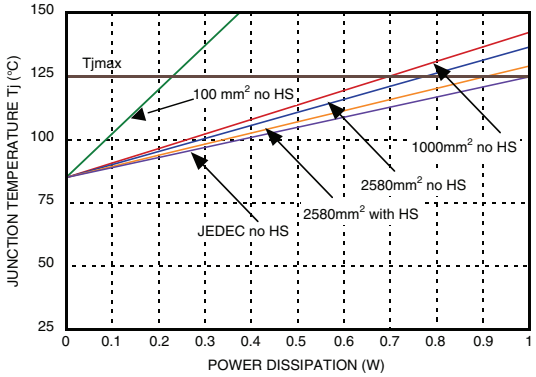
HMC976LP3E JUNCTION TEMPERATURE °C vs. TOTAL POWER DISSIPATION 25°C AMBIENT



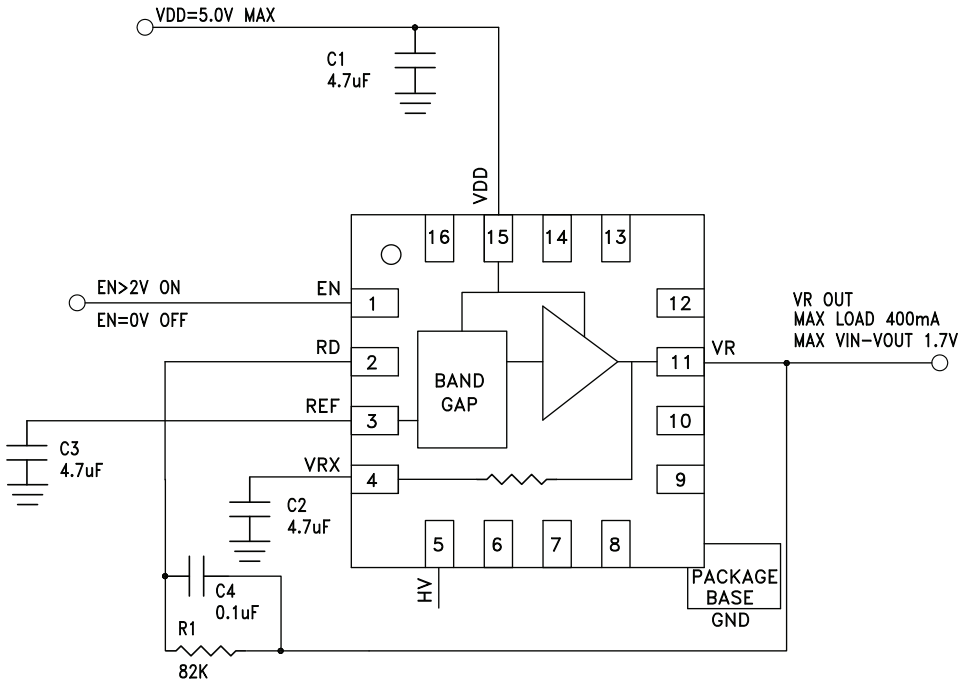
HMC976LP3E JUNCTION TEMPERATURE °C vs. TOTAL POWER DISSIPATION 50°C AMBIENT



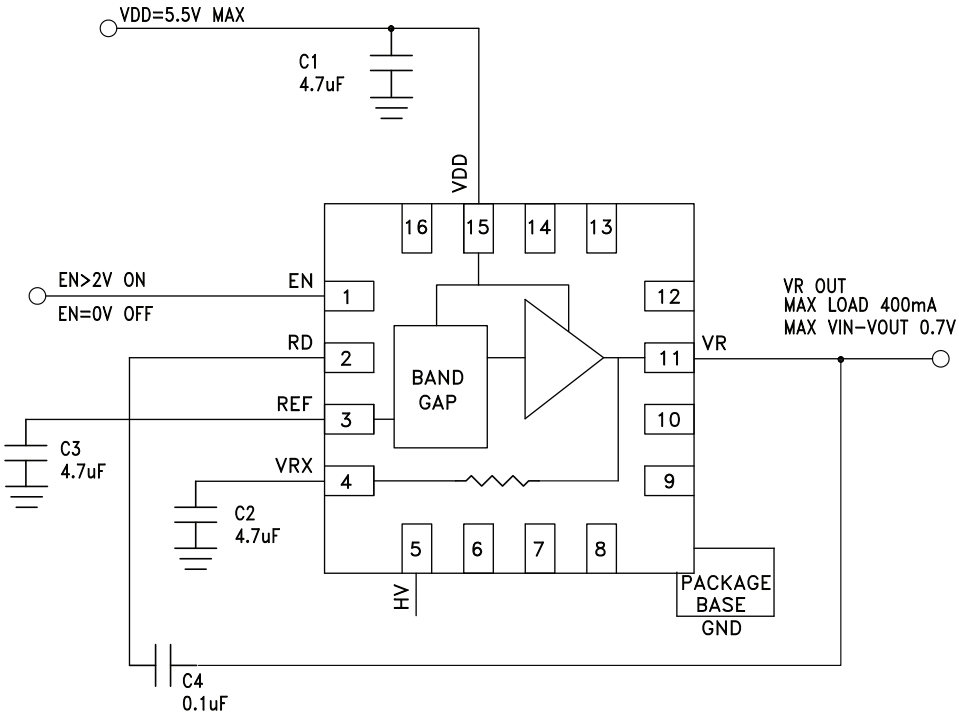
HMC976LP3E JUNCTION TEMPERATURE °C vs. TOTAL POWER DISSIPATION 85°C AMBIENT



HMC976LP3E 3.3V User Application Schematic



HMC976LP3E 4.8V User Application Schematic



HMC976LP3E 5V User Application Schematic