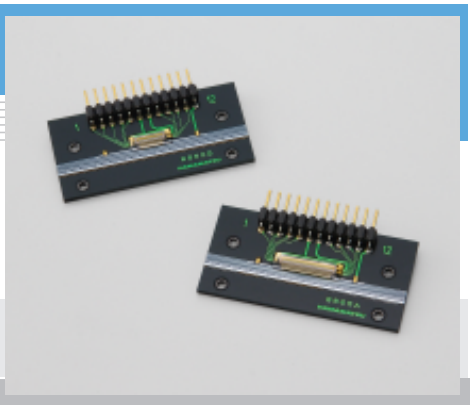
Photodiode array with amplifier
S8865 series

Photodiode array combined with signal processing circuit chip



S8865 series is a Si photodiode array combined with a signal processing circuit chip. The signal processing circuit chip is formed by CMOS process and incorporates a timing generator, shift register, charge amplifier array, clamp circuit and hold circuit, making the external circuit configuration simple. A long, narrow image sensor can also be configured by arranging multiple arrays in a row. For X-ray detection applications, types with fluorescent paper affixed on the active area are also available.

Features

- Large element pitch: 2 types available
  S8865-64: 0.8 mm pitch × 64 ch
  S8865-128: 0.4 mm pitch × 128 ch
- 5 V power supply operation
- Simultaneous integration by using a charge amplifier array
- Sequential readout with a shift register
  (Data rate: 1 MHz Max.)
- Low dark current due to zero-bias photodiode operation
- Integrated clamp circuit allows low noise and wide dynamic range
- Integrated timing generator allows operation at two different pulse timings
- Types with phosphor screen affixed on the active area are available for X-ray detection: S8865-64G/S8865-128G

Applications

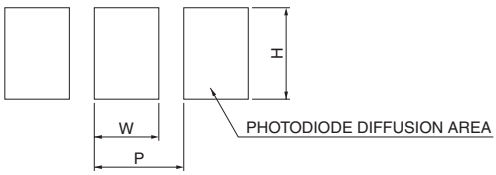
- Long line sensors
- Line sensors for X-ray detection

■ Mechanical specifications

Parameter	Symbol *1	S8865-64	S8865-128	Unit
Element pitch	P	0.8	0.4	mm
Element diffusion width	W	0.7	0.3	mm
Element height	H	0.8	0.6	mm
Number of elements	-	64	128	-
Active area length	-	51.2	51.2	mm

*1: Refer to following figure.

■ Enlarged view of active area



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■ Absolute maximum ratings

Parameter	Symbol	Rated value	Unit
Supply voltage	Vdd	-0.3 to +6	V
Reference voltage	Vref	-0.3 to +6	V
Photodiode voltage	Vpd	-0.3 to +6	V
Gain selection terminal voltage	Vgain	-0.3 to +6	V
Master/slave selection voltage	Vms	-0.3 to +6	V
Clock pulse voltage	V (CLK)	-0.3 to +6	V
Reset pulse voltage	V (RESET)	-0.3 to +6	V
External start pulse voltage	V (EXTST)	-0.3 to +6	V
Operating temperature *2	Topr	-5 to +60	°C
Storage temperature	Tstg	-10 to +70	°C

*2 : No condensation

■ Recommended terminal voltage

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		Vdd	4.75	5	5.25	V
Reference voltage		Vref	4	4.5	Vdd	V
Photodiode voltage		Vpd	-	Vref	-	V
Gain selection terminal voltage	High gain	Vgain	Vdd-0.25	Vdd	Vdd+0.25	V
	Low gain		0	-	0.4	V
Master/slave selection voltage	High level *3	Vms	Vdd-0.25	Vdd	Vdd+0.25	V
	Low level *4		0	-	0.4	V
Clock pulse voltage	High level	V (CLK)	Vdd-0.25	Vdd	Vdd+0.25	V
	Low level		0	-	0.4	V
Reset pulse voltage	High level	V (RESET)	Vdd-0.25	Vdd	Vdd+0.25	V
	Low level		0	-	0.4	V
External start pulse voltage	High level	V (EXESP)	Vdd-0.25	Vdd	Vdd+0.25	V
	Low level		0	-	0.4	V

*3 : Parallel
*4 : Serial at 2nd or later stages

■ Electrical characteristics [Ta=25 °C, Vdd=5 V, V (CLK)=V (RESET)=5 V]

Parameter		Symbol	S8865-64			S8865-128			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock pulse frequency *5		f (CLK)	40	-	4000	40	-	4000	kHz
Output impedance		Zo	-	3	-	-	3	-	kΩ
Power consumption		P	-	100	-	-	180	-	mW
Charge amp feedback capacitance	High gain	Cf	-	0.5	-	-	0.5	-	pF
	Low gain		-	1	-	-	1	-	

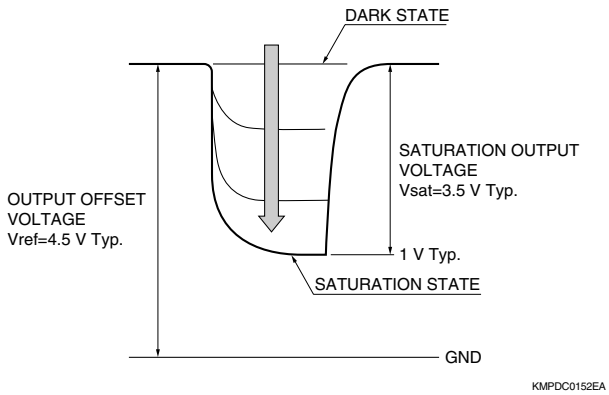
* 5: Video data rate is 1/4 of clock pulse frequency f (CLK).

■ Electrical/optical characteristics [Ta=25 °C, Vdd=5 V, V (CLK)=V (RESET)=5 V, Vgain=5 V (High gain), 0 V (Low gain)]

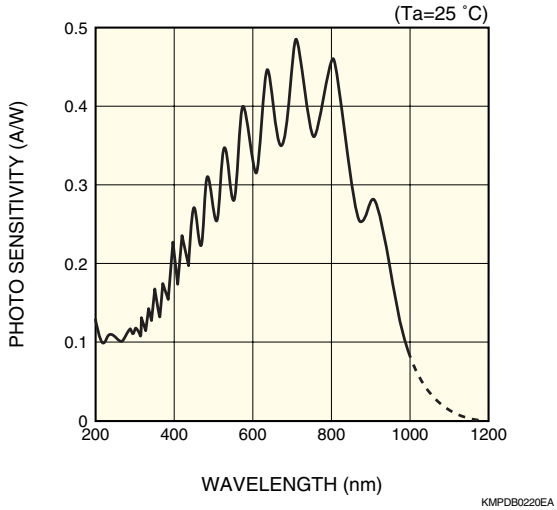
Parameter		Symbol	S8865-64			S8865-128			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Spectral response range		λ	200 to 1000						nm
Peak sensitivity wavelength		λp	-	720	-	-	720	-	nm
Dark output voltage *6	High gain	Vd	-	0.02	0.2	-	0.01	0.1	mV
	Low gain		-	0.01	0.1	-	0.005	0.05	
Saturation output voltage		Vsat	-	3.5	-	-	3.5	-	V
Saturation exposure *7	High gain	Esat	-	0.8	-	-	2.4	-	mlx · s
	Low gain		-	1.6	-	-	4.8	-	
Photo sensitivity	High gain	S	-	4400	-	-	1500	-	V/lx · s
	Low gain		-	2200	-	-	750	-	
Photo response non-uniformity *8		PRNU	-	-	±10	-	-	±10	%
Noise *9	High gain	N	-	1	-	-	1	-	mVrms
	Low gain		-	0.6	-	-	0.6	-	
Output offset voltage *10		Vos	-	Vref	-	-	Vref	-	V

*6: Integration time ts=1 ms
*7: Measured with a 2856 K tungsten lamp.
*8: When the photodiode array is exposed to uniform light which is 50 % of the saturation exposure, the Photo Response Non-Uniformity (PRNU) is defined as follows:
PRNU = ΔX/X × 100 (%)
where X is the average output of all elements and ΔX is the difference between the maximum and minimum outputs.
*9: Measured with a video data rate of 50 kHz and Ts=1 ms in dark state.
*10: Video output is negative-going output with respect to the output offset voltage.

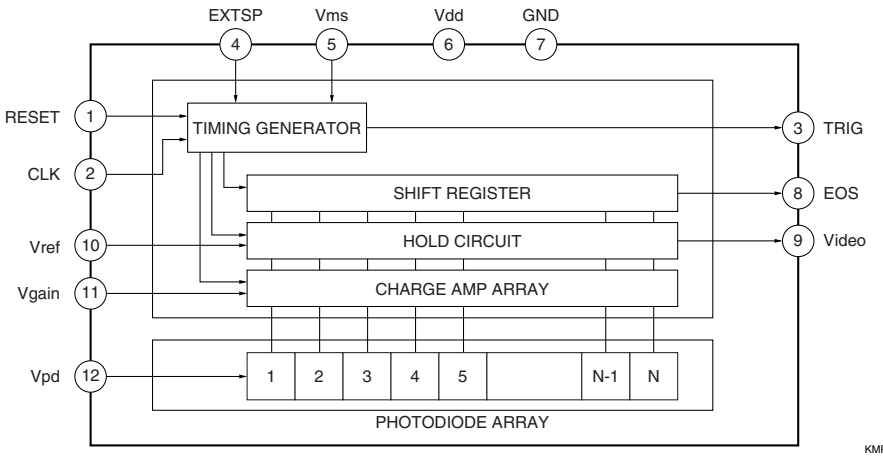
■ Output waveform of one element



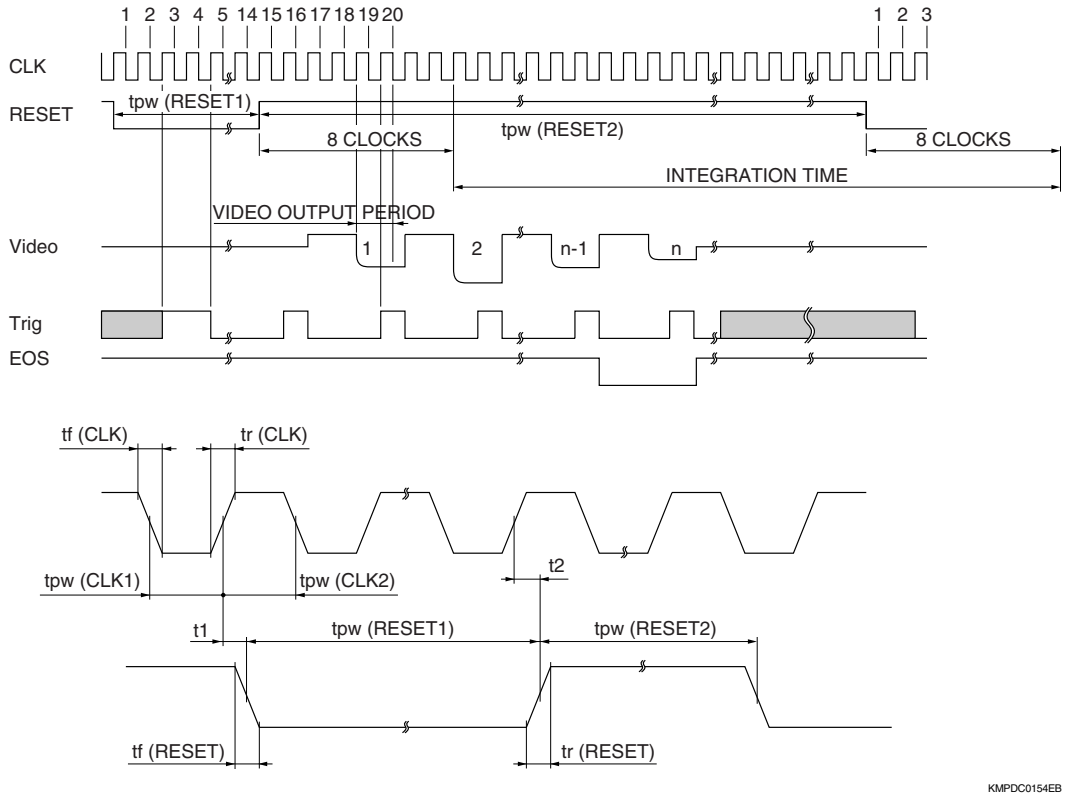
■ Spectral response (measurement example)



■ Block diagram



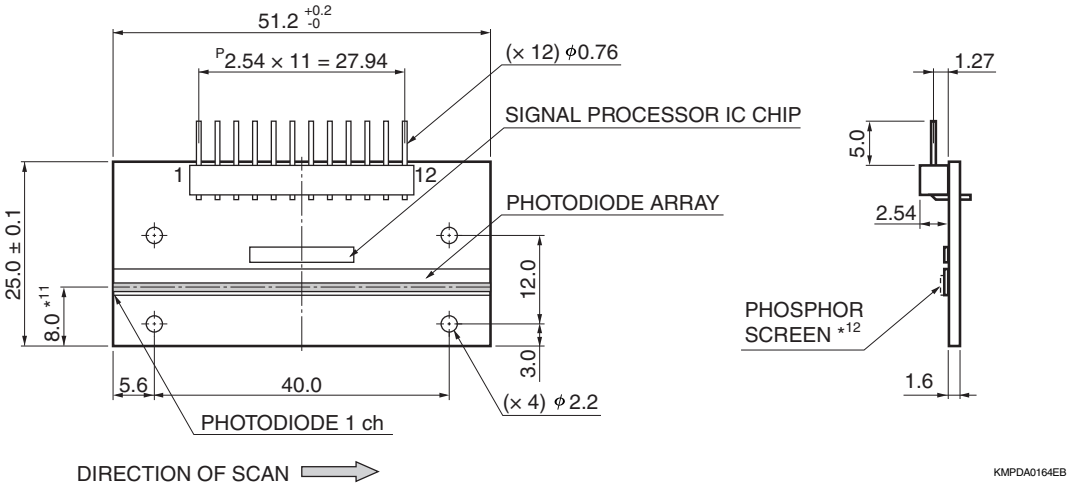
■ Timing chart



Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse width	tpw (CLK1), tpw (CLK2)	125	-	12500	ns
Clock pulse rise/fall times	tr (CLK), tf (CLK)	0	20	30	ns
Reset pulse width 1	tpw (RESET1)	10	-	-	µs
Reset pulse width 2	tpw (RESET2)	20	-	-	µs
Reset pulse rise/fall times	tr (RESET), tf (RESET)	0	20	30	ns
Clock pulse-reset pulse timing 1	t1	-20	0	20	ns
Clock pulse-reset pulse timing 2	t2	-20	0	20	ns

1. The internal timing circuit starts operation at a fall of CLK immediately after a RESET pulse sets to Low.
2. When a fall of CLK is counted as "1 clock", the video signal at the 1st channel appears between "18.5 clocks and 20 clocks". Then a video signal appears every 4 clocks.
3. Signal charge integration time equals the High period of a RESET pulse. However, the charge integration does not start at the rise of a RESET pulse but starts at the 8th clock after the rise of the RESET pulse and ends at the 8th clock after the fall of the RESET pulse. Signals integrated within this period are sequentially read out as time-series signals by the shift register operation when the RESET pulse next changes from High to Low. The rise and fall of a RESET pulse must be synchronized with the fall of a CLK pulse, but the rise of a RESET pulse must be set outside the video output period. One cycle of RESET pulses cannot be set shorter than the time equal to "(video signal readout period 16.5 + 4) × N (number of pixels)" clocks.

■ Dimensional outline (unit: mm)



*11: Distance from the bottom of the board to the center of active area
Board: G10 glass epoxy
Connector: PRECI-DIP DURTAL 800-10-012-20-001

*12: Photodiode array with phosphor screen: S8865-64G/-128G only
· Material Gd_2O_2S: Tb
· Phosphor thickness 300 µm Typ.
· Detectable energy range 30k to 100 keV

■ Pin connection

Pin No.	Symbol	Name	Note
1	RESET	Reset pulse	Pulse input
2	CLK	Clock pulse	Pulse input
3	Trig	Trigger pulse	Positive-going pulse output
4	EXTSP	External start pulse	Pulse input
5	Vms	Master/slave selection supply voltage	Voltage input
6	Vdd	Supply voltage	Voltage input
7	GND	Ground	
8	EOS	End of scan	Negative-going pulse output
9	Video	Video output	Negative-going output with respect to Vref
10	Vref	Reference voltage	Voltage input
11	Vgain	Gain selection terminal voltage	Voltage input
12	Vpd	Photodiode voltage	Voltage input

■ Gain selection terminal voltage setting
Vdd: High gain (Cf: 0.5 pF) GND: Low gain (Cf: 1 pF)

■ Master/slave selection voltage Vms and external start pulse EXTSP settings
Set to A in the table below in most cases.
To sequentially read out signals from two or more sensors linearly connected, set the 1st sensor to A and the 2nd or later sensors to B. The CLK and RESET pulses should be shared with each sensor and the video output terminal of each sensor connected together.

		Vms	EXTSP
A	Parallel readout, serial readout at 1st sensor	Vdd	Vdd
B	Serial readout at 2nd and later sensors	GND	Preceding sensor EOS should be input

■ Readout circuit
Check that pulse signals meet the required pulse conditions before supplying them to the input terminals.
Video output should be amplified by an operational amplifier that is connected close to the sensor.

■ Cautions during use

(1) The signal processing circuit chips of S8865 series are protected against static electricity. However, in order to prevent possible damage to the chip, implement electrostatic countermeasures such as grounding of the operator, work table and tools. Furthermore, the devices must be protected against surge voltages from external equipment.

(2) Since the photodiode array chip is not protected, handle it carefully so it will not become contaminated or scratched. Photodiode array performance may deteriorate if operated at high temperatures and humidity, so the housing should be designed to be airtight. The signal processing circuit chip and its wire bonding are covered with a resin coating for protection, but never touch these portions. In addition, take care when installing the board so that it does not warp.

(3) S8865-64G, -128G
Signal processing IC chip performance will drop if subjected to X-rays. Protect the IC chip from X-rays by installing a lead shield.

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Cat. No. KMPD1071E01
Jan. 2004 DN