FUJITSU MICROELECTRONICS
DATA SHEET

DS07-13713-6E

*16-bit Proprietary Microcontroller*

**CMOS**

# F²MC-16LX MB90495G Series

# MB90497G/F497G/F498G/V495G

## ■ DESCRIPTION

The MB90495G Series is a general-purpose, high-performance 16-bit microcontroller. It was designed for devices like consumer electronics, which require high-speed, real-time process control. This series features an on-chip full-CAN interface.

In addition to being backwards compatible with the F²MC* family architecture, the instruction set has been expanded to add support for high-level language instructions, expanded addressing mode, and enhanced multiply/divide and bit processing instructions. A 32-bit accumulator is also provided, making it possible to process long word (32-bit) data.

The MB90495G Series peripheral resources include on chip 8/10-bit A/D converter, UART (SCI) 0/1, 8/16-bit PPG timer, 16-bit I/O timer (16-bit free-run timer, input capture 0, 1, 2, 3 (ICU) ) , and CAN controller.

* : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

## ■ FEATURES

- **Models that support operating temperature ($T_A$) +125** °C
- **Clock**
  - •Built-in PLL clock multiplier circuit
  - •Choose 1/2 oscillation clock or ×1 to ×4 multiplied oscillation clock (for a 4-MHz oscillation clock, 4 to 16 MHz) machine (PLL) clock

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For the information for microcontroller supports, see the following web site.

http://edevice.fujitsu.com/micom/en-support/


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•Select subclock behavior (8.192 kHz)
•Minimum instruction execution time : 62.5 ns (operating with 4-MHz oscillation clock and × 4 PLL clock)

- **16-Mbyte CPU memory space**
  •24-bit internal addressing
  •External access possible through selection of 8/16-bit bus width (external bus mode)

- **Optimum instruction set for controller applications**
  •Wealth of data types (Bit, Byte, Word, Long Word)
  •Wealth of addressing modes (23 different modes)
  •Enhanced signed multiply-divide instructions and RETI instruction functions
  •Enhanced high-precision arithmetic employing 32-bit accumulator

- **Instruction set supports high-level programming language (C) and multitasking**
  •Employs system stack pointer
  •Enhanced indirect instructions with all pointer types
  •Barrel shift instructions

- **Improved execution speed**
  •4-byte instruction queue

- **Powerful interrupt feature**
  •Powerful 8-level, 34-condition interrupt feature

- **CPU-independent automated data forwarding**
  •Extended intelligent I/O service feature (EI$^2$OS) : maximum 16 channels

- **Low-power consumption (Standby) Mode**
  •Sleep mode (CPU operation clock stopped)
  •Time-base timer mode (oscillation clock and subclock, time-base timer and watch timer only operational)
  •Watch mode (subclock and watch timer only operational)
  •Stop mode (oscillation clock and subclock stopped)
  •CPU intermittent operation mode

- **Process**
  •CMOS technology

- **I/O Ports**
  •Generic I/O ports (CMOS output) : 49

- **Timer**
  •Time-base timer, watch timer, watchdog timer : 1 channel
  •8/16-bit PPG timer : four 8-bit channels, or two 16-bit channels
  •16-bit reload timer : 2 channels
  •16-bit I/O timer
    •16-bit free-run timer : 1 channel
    •16-bit input capture (ICU) : 4 channels
    Generates interrupt requests by latching onto the count value of the 16-bit free-run timer with pin input edge detection

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- **CAN Controller** : **1 channel**
  •CAN specifications conform to versions 2.0A and 2.0B
  •8 on-chip message buffers
  •Forwarding rate 10 kbps to 1 Mbps (with 16-MHz machine clock)

- **UART0 (SCI) /UART1 (SCI) : 2 channels**
  •All with full duplex double buffer
  •Use clock-asynchronous or clock-synchronous serial forwarding

- **DTP/external interrupt : 8 channels**
  •A module for launching extended intelligent I/O service ($EI^2OS$) and generating external interrupts through external output

- **Delayed interrupt generation module**
  •Generates interrupt requests for switching tasks

- **8/10-bit A/D converter : 8 channels**
  •Switch between 8-bit and 10-bit resolution
  •Launch through external trigger input
  •Conversion time : 6.13 μs (with 16-MHz machine clock, including sampling time)

- **Program batch function**
  •2-address pointer ROM correction

- **Clock output function**

## ■ PRODUCT LINEUP

| Parameter \ Part Number | | MB90F497G | MB90497G | MB90F498G | MB90V495G |
|---|---|---|---|---|---|
| Feature Classification | | Flash ROM | Mask ROM | Flash ROM | Product Evaluated |
| ROM Size | | 64 Kbytes | | 128 Kbytes | — |
| RAM Size | | 2 Kbytes | | | 6 Kbytes |
| Process | | CMOS | | | |
| Package | | LQFP64 (pin pitch 0.65 mm) , QFP64 (pin pitch 1.00 mm) | | | PGA256 |
| Operating Power | | 4.5 V to 5.5 V | | | |
| Emulator power supply* | | — | | | None |
| CPU Functions | | Number of instructions : 351<br>Instruction bit length : 8-bit, 16-bit<br>Instruction length : 1 to 7 bytes<br>Data bit length : 1 bit, 8-bit, 16-bit | | | |
| | | Minimum execution time : 62.5 ns (with 16-MHz machine clock) | | | |
| | | Interrupt processing time : minimum 1.5 µs (with 16-MHz machine clock) | | | |
| Low-power consumption (Standby) Mode | | Sleep mode/watch mode/time-base timer mode/stop mode / CPU intermittent mode | | | |
| I/O Ports | | General-purpose I/O ports (CMOS output) : 49 | | | |
| Time-base timer | | 18-bit free-run counter<br>Interrupt interval : 1.024 ms, 4.096 ms, 16.834 ms, 131.072 ms (with 4-MHz oscillation clock) | | | |
| Watchdog timer | | Reset generation intervals : 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (with 4-MHz oscillation clock) | | | |
| 16-bit I/O Timer | 16-bit free-run timer | Number of channels : 1<br>Interrupts from overflow generation | | | |
| | Input capture | Number of channels : 4<br>Maintenance of free-run timer value through pin input (rising, falling or both edges) | | | |
| 16-bit reload timer | | Number of channels : 2<br>16-bit reload timer operation<br>Count clock interval : 0.25 µs, 0.5 µs, 2.0 µs (with 16-MHz machine clock)<br>External event count enabled | | | |
| Watch timer | | 15-bit free-run counter<br>Interrupt intervals : 31.25 ms, 62.5 ms, 12 ms, 250 ms, 500 ms, 1.0 s, 2.0 s (with 8.192-kHz subclock) | | | |
| 8/16-bit PPG timer | | Number of channels : 2 (two 8-bit channels can be used)<br>Two 8-bit or one 16-bit channel PPG operation possible<br>Free interval, free duty pulse output possible<br>Count clock : 62.5 ns to 1 µs (with 16-MHz machine clock) | | | |

* : The S2 dipswitch setting when using the MB2145-507 emulation baud. For details, see the MB2145-507 hardware manual (2.7 Emulator Power Pin) .

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| Parameter \ Part Number | MB90F497G | MB90497G | MB90F498G | MB90V495G |
|---|---|---|---|---|
| Delayed interrupt generation module | Module for delayed interrupt generation switching tasks<br>Used in real-time OS | | | |
| DTP/external interrupt circuit | Number of inputs : 8<br>Starting by rising edge, falling edge, “H” level input, or “L” level input, external interrupts or extended intelligent I/O service (EI$^2$OS) can be used | | | |
| 8/10-bit A/D converter | Number of channels : 8<br>Resolution : set 10-bit or 8-bit<br>Conversion time : 6.13 µs (with 16-MHz machine clock, including sampling time)<br>Continuous conversion of multiple linked channels possible<br>(up to 8 channels can be set)<br>One-shot conversion mode : converts selected channel only once<br>Continuous conversion mode : converts selected channel continuously<br>Stop conversion mode : converts selected channel and suspends operation repeatedly | | | |
| UART0 (SCI) | Number of channels : 1<br>Clock-synchronous forwarding : 62.5 kbps to 2 Mbps<br>Clock-asynchronous forwarding : 1,202 bps to 62,500 bps<br>Transmission can be performed by two-way serial transmission or by master/slave connection | | | |
| UART1 (SCI) | Number of channels : 1<br>Clock-synchronous forwarding : 62.5 kbps to 2 Mbps<br>Clock-asynchronous forwarding : 9,615 bps to 500 kbps<br>Transmission can be performed by two-way serial transmission or by master/slave connection | | | |
| CAN | Compliant with CAN specification versions 2.0A and 2.0B<br>Send/receive message buffers : 8<br>Forwarding bit rate : 10 kbps to 1 Mbps (with 16-MHz machine clock) | | | |

## ■ PACKAGES AND CORRESPONDING PRODUCTS

| Package | MB90F497G | MB90497G | MB90F498G |
|---|---|---|---|
| FPT-64P-M06 | ○ | ○ | ○ |
| FPT-64P-M23 | ○ | ○ | ○ |

○ : available × : not available

Note : See “■ PACKAGE DIMENSIONS” for details.

## ■ PRODUCT COMPARISON

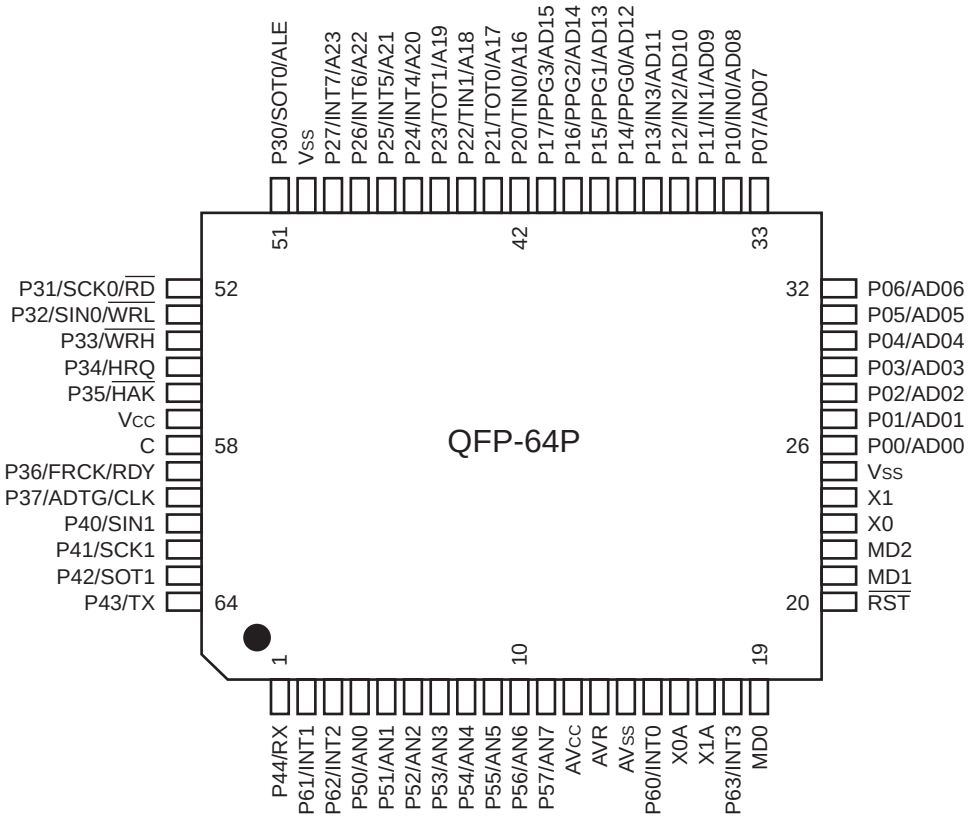
### Memory Size

When evaluating with evaluation chips and other means, take careful note of the different between the evaluation chip and the chip actually used. Take particular note of the following.

- While the MB90V495G does not feature an on-chip ROM, the dedicated development tool can be used to achieve operation equivalent to a product with built-in ROM. Therefore, the ROM size is configured by the development tool.
- On the MB90V495G, the FF4000$_H$ to FFFFFF$_H$ image is only visible in the 00 bank, and the FE0000$_H$ to FF3FFF$_H$ is only visible in the FE and FF banks (configurable on development tool) .
- On the MB90F497G/F498G/497G, the FF4000$_H$ to FFFFFF$_H$ image is visible in the 00 bank, and the FF0000$_H$ to FF3FFF$_H$ is visible only in the FF bank.

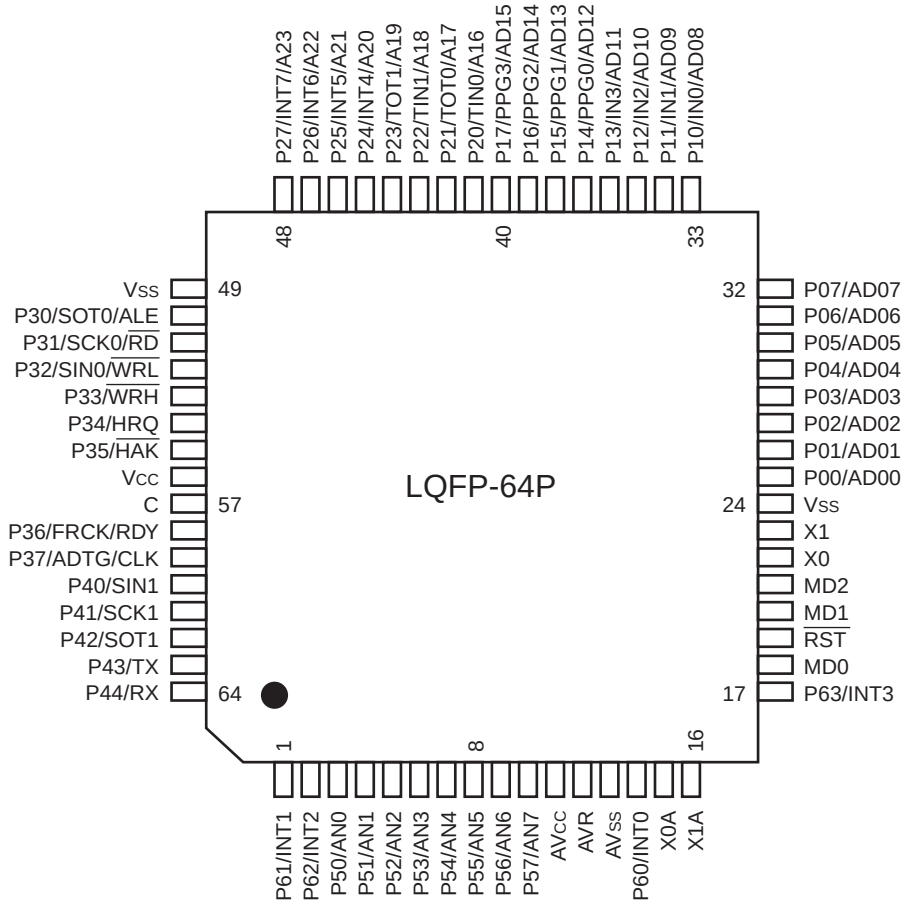
## ■ PIN ASSIGNMENTS

(TOP VIEW)




(FPT-64P-M06)

(TOP VIEW)




(FPT-64P-M23)

## ■ PIN DESCRIPTION

| Pin No. | | Pin Name | Circuit Type | Description |
|---|---|---|---|---|
| QFP-64P *1 | LQFP-64P *2 | | | |
| 2 | 1 | P61 | D | General-purpose I/O port |
| | | INT1 | | Functions as external interrupt input pin. Set this to input port. |
| 3 | 2 | P62 | D | General-purpose I/O port |
| | | INT2 | | Functions as external interrupt input pin. Set this to input port. |
| 4 to 11 | 3 to 10 | P50 to P57 | E | General-purpose I/O port |
| | | AN0 to AN7 | | Functions as analog input port of A/D converter. This is enabled if analog input configuration is permitted. |
| 12 | 11 | $AV_{CC}$ | — | $V_{CC}$ power input pin of A/D converter. |
| 13 | 12 | AVR | — | Reference voltage (+) input pin for the A/D converter.This voltage must not exceed $V_{CC}$ and $AV_{CC}$. Reference voltage (–) is fixed to $AV_{SS}$. |
| 14 | 13 | $AV_{SS}$ | — | $V_{SS}$ power input pin of A/D converter. |
| 15 | 14 | P60 | D | General-purpose I/O port |
| | | INT0 | | Functions as external interrupt input pin. Set this to input port. |
| 16 | 15 | X0A | A | Low-speed oscillation pin.<br>Perform pull-down processing if not connected to an oscillator. |
| 17 | 16 | X1A | A | Low-speed oscillation pin.<br>Set to open if not connected to an oscillator. |
| 18 | 17 | P63 | D | General-purpose I/O port |
| | | INT3 | | Functions as external interrupt input pin. Set this to input port. |
| 19 | 18 | MD0 | C | Input pin for specifying operation mode. |
| 20 | 19 | $\overline{RST}$ | B | External reset input pin. |
| 21 | 20 | MD1 | C | Input pin for specifying operation mode. |
| 22 | 21 | MD2 | F | Input pin for specifying operation mode. |
| 23 | 22 | X0 | A | High-speed oscillation pin. |
| 24 | 23 | X1 | A | High-speed oscillation pin. |
| 25 | 24 | $V_{SS}$ | — | Power supply (0 V) input pin. |
| 26 to 33 | 25 to 32 | P00 to P07 | D | General-purpose I/O port<br>Only enabled in single-chip mode. |
| | | AD00 to AD07 | | I/O pin for the lower 8-bit of the external address data bus.<br>Only enabled during external bus mode. |
| 34 to 37 | 33 to 36 | P10 to P13 | D | General-purpose I/O port. Only enabled in single-chip mode. |
| | | IN0 to IN3 | | Functions as trigger input pin for input capture channels ch.0 to ch.3. Set this to input port. |
| | | AD08 to AD11 | | I/O pin for upper 4-bit of external address data bus.<br>Only enabled during external bus mode. |

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| Pin No. | | Pin Name | Circuit Type | Description |
|---|---|---|---|---|
| QFP-64P *1 | LQFP-64P *2 | | | |
| 38 to 41 | 37 to 40 | P14 to P17 | D | General-purpose I/O port.<br>Only enabled in single-chip mode. |
| | | PPG0 to PPG3 | | Functions as output pin of PPG timer 0/1, 2/3. Only valid if output configuration is enabled. |
| | | AD12 to AD15 | | I/O pin for upper 4-bit of external address data bus.<br>Only enabled during external bus mode. |
| 42 | 41 | P20 | D | General-purpose I/O port.<br>When the bits of high address control register (HACR) are set to “1” in external bus mode, these pins function as general purpose I/O ports. |
| | | TIN0 | | Functions as event input pin of TIN0 reload timer 0.<br>Set this to input port. |
| | | A16 | | Output pin of external address bus (A16) .<br>Only valid when the bits of high address control register (HACR) are set to “0” in external bus mode. |
| 43 | 42 | P21 | D | General-purpose I/O port.<br>When the bits of high address control register (HACR) are set to “1” in external bus mode, these pins function as general purpose I/O ports. |
| | | TOT0 | | Functions as event output pin of TOT0 reload timer 0.<br>Only valid if output configuration enabled. |
| | | A17 | | Output pin of external address bus (A17) .<br>Only valid when the bits of high address control register (HACR) are set to “0” in external bus mode. |
| 44 | 43 | P22 | D | General-purpose I/O port.<br>When the bits of high address control register (HACR) are set to “1” in external bus mode, these pins function as general purpose I/O ports. |
| | | TIN1 | | Functions as event input pin of TIN1 reload timer 1.<br>Set this to input port. |
| | | A18 | | Output pin of external address bus (A18) .<br>Only valid when the bits of high address control register (HACR) are set to “0” in external bus mode. |
| 45 | 44 | P23 | D | General-purpose I/O port.<br>When the bits of high address control register (HACR) are set to “1” in external bus mode, these pins function as general purpose I/O ports. |
| | | TOT1 | | Functions as event output pin for TOT1 reload timer 1.<br>Only valid if output configuration enabled. |
| | | A19 | | Output pin for external address bus (A19) .<br>Only valid when the bits of high address control register (HACR) are set to “0” in external bus mode. |

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*(Continued)*

| Pin No. | | Pin Name | Circuit Type | Description |
|---|---|---|---|---|
| QFP-64P *1 | LQFP-64P *2 | | | |
| 46 to 49 | 45 to 48 | P24 to P27 | D | General-purpose I/O port.<br>When the bits of high address control register (HACR) are set to “1” in external bus mode, these pins function as general purpose I/O ports. |
| | | INT4 to INT7 | | Functions as external interrupt input pin. Set this to input port. |
| | | A20 to A23 | | Output pin for external address bus (A20 to A23) .<br>Only valid when the bits of high address control register (HACR) are set to “0” in external bus mode. |
| 50 | 49 | $V_{SS}$ | — | Power supply (0 V) input pin. |
| 51 | 50 | P30 | D | General-purpose I/O port.<br>Only enabled in single-chip mode. |
| | | SOT0 | | UART0 serial data output pin.<br>Only valid if UART0 serial data output configuration is enabled. |
| | | ALE | | Address latch authorization output pin.<br>Only enabled during external bus mode. |
| 52 | 51 | P31 | D | General-purpose I/O port.<br>Only enabled in single-chip mode. |
| | | SCK0 | | UART0 serial clock I/O pin.<br>Only valid if UART0 serial clock I/O configuration is enabled. |
| | | $\overline{RD}$ | | Lead strobe output pin.<br>Only enabled during external bus mode. |
| 53 | 52 | P32 | D | General-purpose I/O port. |
| | | SIN0 | | UART0 serial data input pin.<br>Set this to input port. |
| | | $\overline{WRL}$ | | Write strobe output pin for lower 8-bit of data bus.<br>Only valid if $\overline{WRL}$ pin output is enabled, in external bus mode. |
| 54 | 53 | P33 | D | General-purpose I/O port. |
| | | $\overline{WRH}$ | | Write strobe output pin for upper 8-bit of data bus.<br>Only valid if external bus mode/16-bit bus mode/$\overline{WRH}$ pin output enabled. |
| 55 | 54 | P34 | D | General-purpose I/O port. |
| | | HRQ | | Hold request input pin.<br>Only valid if hold input is enabled, in external bus mode. |
| 56 | 55 | P35 | D | General-purpose I/O port. |
| | | $\overline{HAK}$ | | Hold addressing output pin.<br>Only valid if hold input is enabled, in external bus mode. |
| 57 | 56 | $V_{CC}$ | — | Power supply (5 V) input pin. |
| 58 | 57 | C | — | Capacity pin for power stabilization.<br>Please connect to an approximately 0.1 µF ceramic capacitor. |

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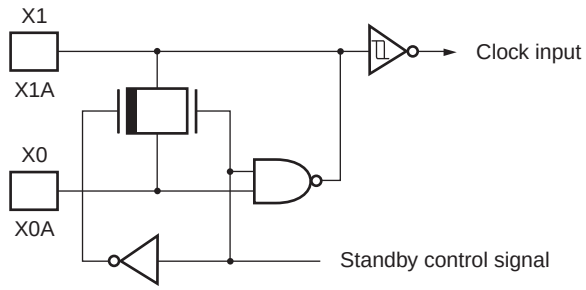
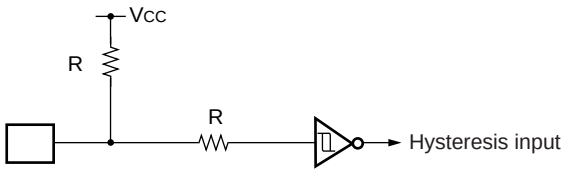
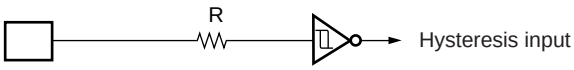
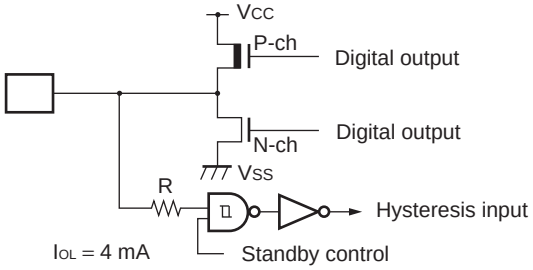
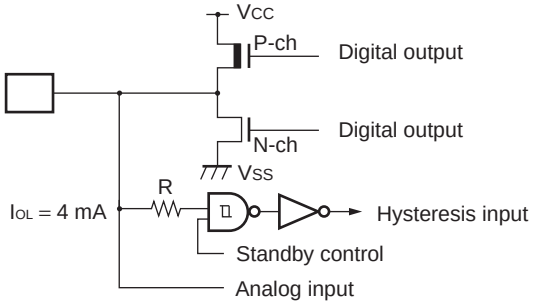
| Pin No. | | Pin Name | Circuit Type | Description |
|---|---|---|---|---|
| QFP-64P *1 | LQFP-64P *2 | | | |
| 59 | 58 | P36 | D | General-purpose I/O port. |
| | | FRCK | | Functions as an external clock input pin for a FRCK 16-bit free-run timer. Set this to input port. |
| | | RDY | | External ready input pin. Only valid if external ready input is enabled, in external bus mode. |
| 60 | 59 | P37 | D | General-purpose I/O port. |
| | | ADTG | | Functions as A/D converter external trigger input pin. Set this to input port. |
| | | CLK | | External clock output pin. Only valid if external clock output is enabled, in external bus mode. |
| 61 | 60 | P40 | D | General-purpose I/O port. |
| | | SIN1 | | UART1 serial data input pin. Set this to input port. |
| 62 | 61 | P41 | D | General-purpose I/O port. |
| | | SCK1 | | UART1 serial clock I/O pin. Only valid if UART1 clock I/O configuration is enabled. |
| 63 | 62 | P42 | D | General-purpose I/O port. |
| | | SOT1 | | UART1 serial data output pin. Only valid if UART1 serial data output configuration is enabled. |
| 64 | 63 | P43 | D | General-purpose I/O port. |
| | | TX | | CAN transmission output pin. Only valid if output configuration enabled. |
| 1 | 64 | P44 | D | General-purpose I/O port. |
| | | RX | | CAN reception input pin. Set this to input port. |

*1 : FPT-64P-M06

*2 : FPT-64P-M23

## ■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|---|---|---|
| A |  | • High speed oscillation feedback resistor : 1 MΩ approx.<br>• Low speed oscillation feedback resistor : 10 MΩ approx. |
| B |  | • Hysteresis input with pull-up<br>• Pull-up Resistor : 50 kΩ approx. |
| C |  | Hysteresis input |
| D |  | • CMOS hysteresis input<br>• CMOS level output<br>• Standby control available |
| E |  | • CMOS hysteresis input<br>• CMOS level output<br>• Doubles as analog input pin<br>• Standby control available |

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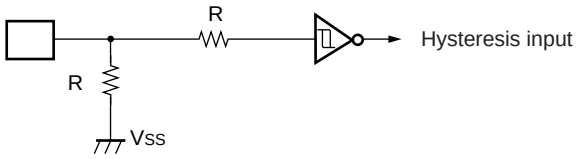
| Type | Circuit | Remarks |
|---|---|---|
| F |  | • Hysteresis input with pull-down<br>• Pull-down Resistor : 50 kΩ approx. (except Flash device) |

## ■ HANDLING DEVICES

- **Make sure you do not exceed the maximum rated values (in order to prevent latch-up) .**
  - CMOS IC chips may suffer latch-up if a voltage higher than $V_{CC}$ or lower than $V_{SS}$ is applied to an input or output pin with other than mid or high current resistance; or voltage exceeding the rating is applied across $V_{CC}$ and $V_{SS}$ pins.
  - Latch-ups can dramatically increase the power supply current, causing thermal breakdown of the device. Make sure that you do not exceed the maximum rated value of your device, in order to prevent a latch-up.
  - When turning the analog power supply on or off, make sure that the analog power voltage ($AV_{CC}$, AVR) and analog input voltages do not exceed the digital voltage ($V_{CC}$) .

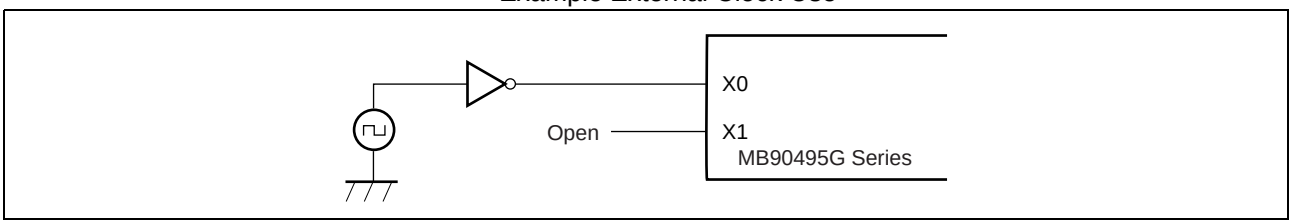
- **Handling Unused Pins**

Leaving unused input/output pins open may cause malfunctions and latch-ups, permanently damaging the device. Prevent this by connecting it to a pull-up or pull-down resistor of no less than 2 kΩ. Leave unused input/output pins open in output mode, or if in input mode, handle them in the same as input pins.

- **Notes on Using External Clock**

When using the external clock, drive pin X0 only, and leave pin X1 unconnected. See below for an example of external clock use.

Example External Clock Use




- **Notes on Not Using Subclock**

If you do not connect pins X0A and X1A to an oscillator, use pull-down handling on the X0A pin, and leave the X1A pin open.

- **Power Supply Pins**
  - If your product has multiple $V_{CC}$ or $V_{SS}$ pins, pins of the same potential are internally connected in the device in order to avoid abnormal operation, including latch-up. However, you should make sure to connect the pins' external power and ground lines, in order to lower unneeded emissions, prevent abnormal operation of strobe signals due to a rise in ground levels, and maintain total output current within rated levels.
  - Take care to connect the $V_{CC}$ and $V_{SS}$ pins of MB90495G Series devices to power lines via the lowest possible impedance.
  - It is recommended that you connect a bypass capacitor of approximately 0.1 µF between $V_{CC}$ and $V_{SS}$ pins near MB90495G Series device pins.

- **Crystal Oscillator Circuit**
  - Noise in the vicinity of X0 and X1 pins could cause abnormal operations in MB90495G Series devices. Make sure to provide bypass capacitors via the shortest possible distance from X0 and X1 pins, crystal oscillators (or ceramic resonators) , and ground lines. In addition, design your printed circuit boards so as to keep X0 and X1 wiring from crossing other wiring, if at all possible.
  - It is strongly recommended that you provide printed circuit board artwork surrounding X0 and X1 pins within a grand area, as this should stabilize operation.

- **A/D Converter Power-up and Analog Input Initiation Sequence**
  - Make sure to power up the A/D converter and analog input (pins AN0 to AN7) after turning on digital power ($V_{CC}$) .
  - Turn off digital power after turning off the A/D converter power supply and analog inputs. In this case, make sure that the voltage of AVR does not exceed $AV_{CC}$ (it is permissible to turn off analog and digital power simultaneously) .

- **Connecting Unused A/D Converter Pins**

If you are not using the A/D converter, set unused pins to $AV_{CC}$ = AVR = $V_{CC}$, $AV_{SS}$ = $V_{SS}$.

- **Notes for Powering Up**

Ensure that the voltage step-up time (between 0.2 V and 2.7 V) at power-up is no less than 50 μs, in order to prevent malfunction in the built-in step-down circuit.

- **Initialization**

The device contains built-in registers which are only initialized by a power-on reset. Cycle the power supply to initialize these registers.

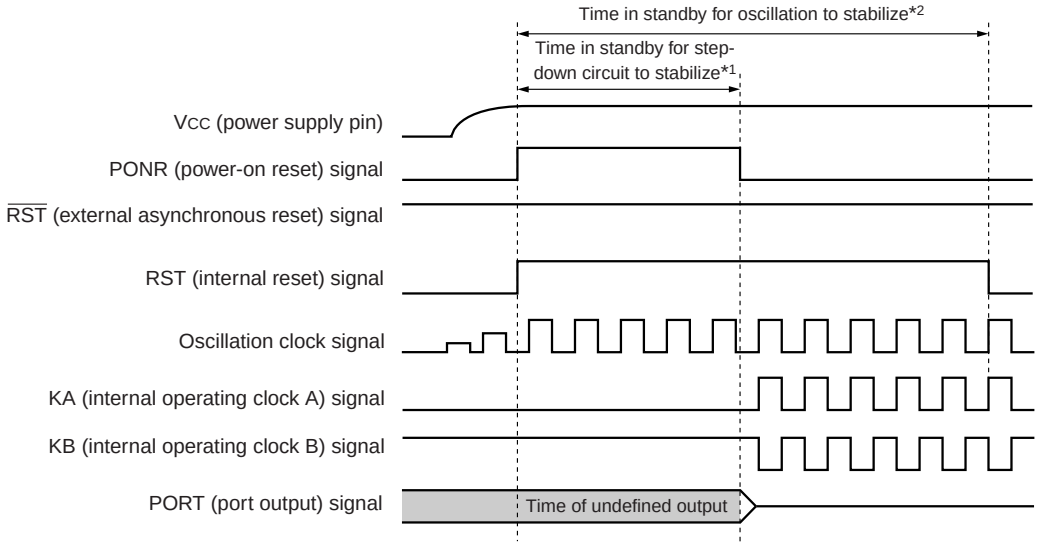
- **Stabilizing the Power Supply**

Make sure that the $V_{CC}$ power supply voltage is stable. Even at the rated operating $V_{CC}$ power supply voltage, large, sudden changes in the voltage could cause malfunctions. As a standard for stable power supply, keep $V_{CC}$ ripples (peak-to-peak value) at commercial power frequencies (50 Hz / 60 Hz) to no more than 10% of the power supply voltage, and momentary surges caused by switching the power supply and other events to more than 0.1 V/ms.

- **If Output from Ports 0/1 Becomes Undefined**

After power is turned on, if the $\overline{RST}$ pin is set to “H” during step-down circuit stabilization standby (during power-on reset) , ports 0 and 1 output will be undefined. If the $\overline{RST}$ pin is set to “L”, ports 0 and 1 will go into a high impedance state. Take careful note of the timing of events outlined in figures 1 and 2.

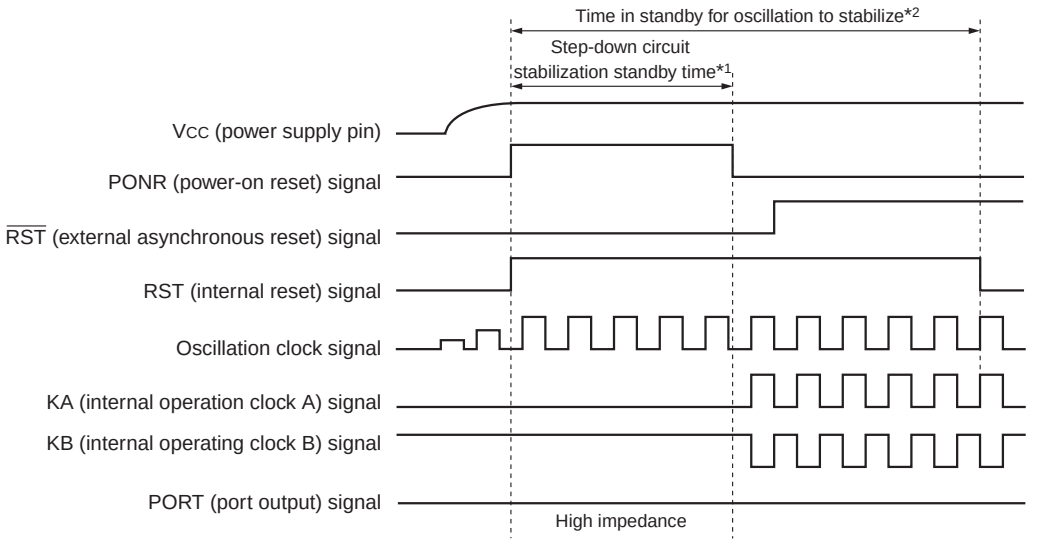
- **Figure 1 - Timing Chart of Undefined Output from Ports 0/1 (with $\overline{\text{RST}}$ pin set to "H")**




*1 : Step-down circuit stabilization standby time : $2^{17}$/oscillation clock frequency
(with 16-MHz oscillation clock frequency, about 8.19 ms)

*2 : Oscillation stabilization standby time : $2^{18}$/oscillation clock frequency
(with 16-MHz oscillation clock frequency, about 16.38 ms)

- **Figure 2 - Timing Chart of High Impedance State for Ports 0/1 (when $\overline{\text{RST}}$ pin is "L")**




*1 : Step-down circuit stabilization standby time : $2^{17}$/oscillation clock frequency
(with 16-MHz oscillation clock frequency, about 8.19 ms)

*2 : Oscillation stabilization standby time : $2^{18}$/oscillation clock frequency
(with 16-MHz oscillation clock frequency, about 16.38 ms)

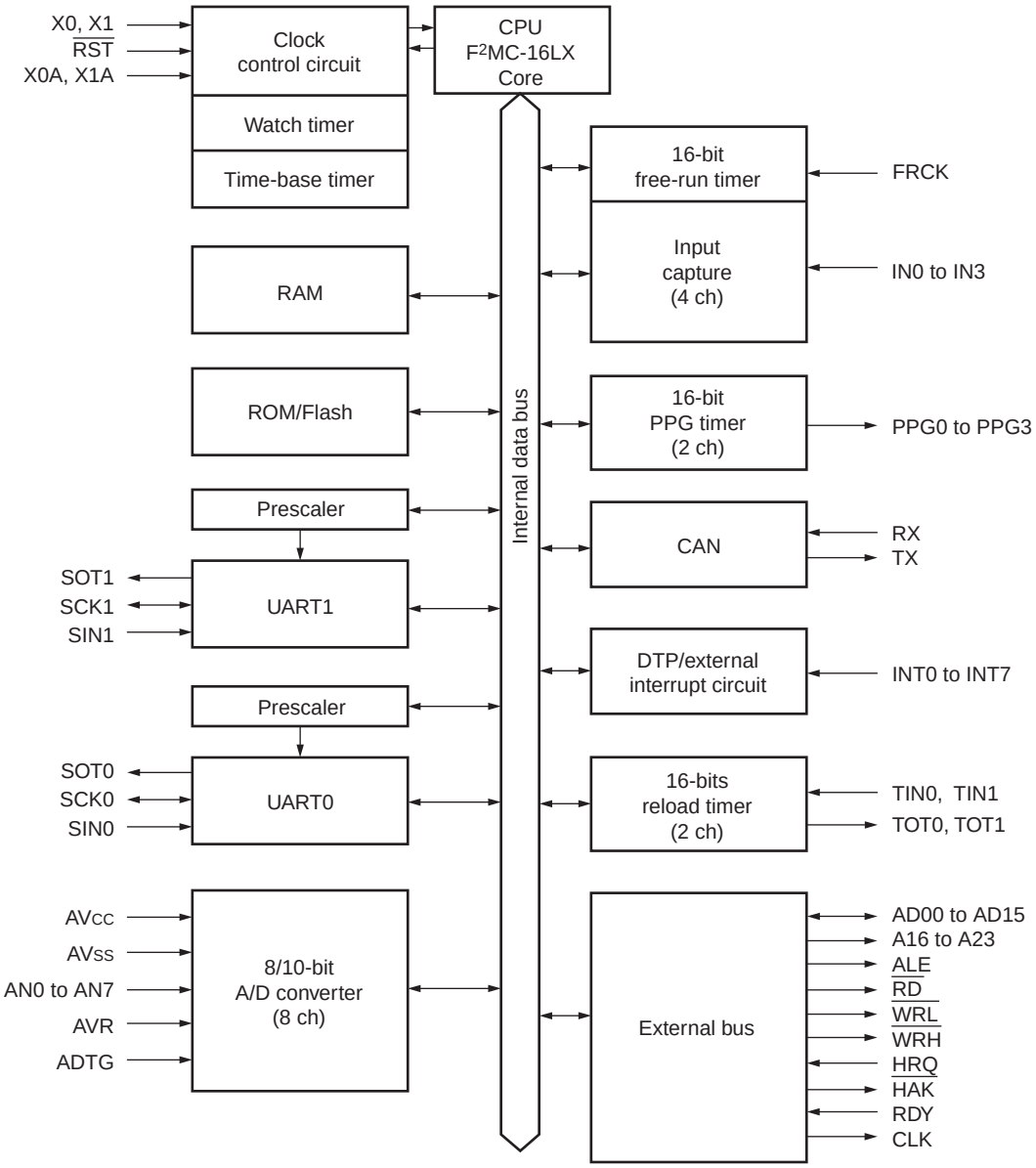
- **Caution on Operations during PLL Clock Mode**

If the PLL clock mode is selected in the microcontroller, it may attempt to continue the operation using the free-running frequency of the automatic oscillating circuit in the PLL circuitry even if the oscillator is out of place or the clock input is stopped. Performance of this operation, however, cannot be guaranteed.

- **Support for $T_A$ = + 125 °C**

If used exceeding $T_A$ = +105 °C, be sure to contact us for reliability limitations.

## ■ BLOCK DIAGRAM



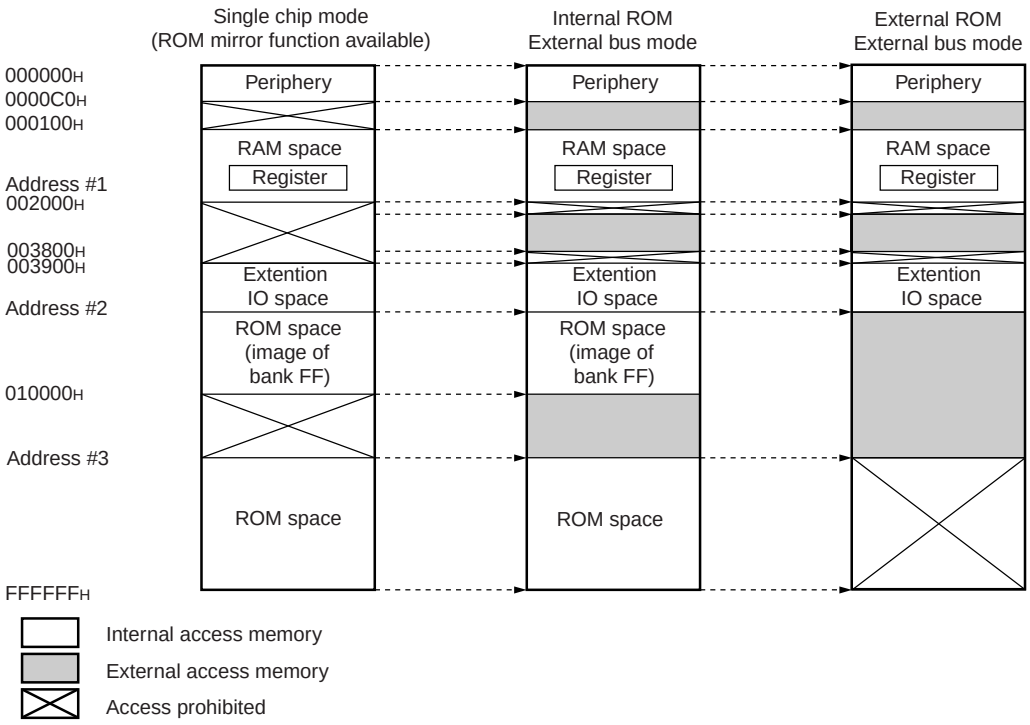
## ■ MEMORY MAP

The memory access modes of the MB90495G Series can be set to single chip mode, internal ROM - external bus mode, and external ROM - external bus mode.

### 1. Memory Allocation of the MB90495G

The MB90495G Series has 24-bit internal address bus and 24-bit external address bus output, enabling it to access up to 16 Mbytes of external access memory. The enable/disable time of the ROM mirror function is shown graphically in the memory map.

### 2. Memory Map




| Product | Address #1* | Address #2 | Address #3* |
|---|---|---|---|
| MB90V495G | 001900H | 004000H | (FC0000H) |
| MB90F497G | 000900H | 004000H | FF0000H |
| MB90497G | 000900H | 004000H | FF0000H |
| MB90F498G | 000900H | 004000H | FE0000H |

* : Addresses #1 and #3 are product-specific.

Note : When the internal ROM is operational, the ROM data in the upper address of bank 00 of the F²MC-16LX is visible in an image. This is called the ROM mirror function, and takes advantage of the small C compiler model. With the F²MC-16LX, the lower 16-bit address of bank FF and the lower 16-bit address of bank 00 are set identical to one another. This allows the ROM-internal table to be referenced without specifying a far pointer. For example, say the address "00C000H" is accessed. In actuality, the "FFC000H " address inside ROM will be accessed. However, as the ROM space in bank FF exceeds 48 Kbytes, the entire space cannot be viewed on bank 00's image. And so, since "FF4000H" to "FFFFFFH" ROM data will be visible on the "004000H" to "00FFFFH" image, save the ROM data table in the "FF4000H" to "FFFFFFH" space.

## ■ I/O MAP

| Address | Register Abbreviation | Register Name | Access | Resource Name | Initial Value |
|---|---|---|---|---|---|
| 000000H | PDR0 | Port 0 data register | R/W | Port 0 | XXXXXXXXB |
| 000001H | PDR1 | Port 1 data register | R/W | Port 1 | XXXXXXXXB |
| 000002H | PDR2 | Port 2 data register | R/W | Port 2 | XXXXXXXXB |
| 000003H | PDR3 | Port 3 data register | R/W | Port 3 | XXXXXXXXB |
| 000004H | PDR4 | Port 4 data register | R/W | Port 4 | XXXXXXXXB |
| 000005H | PDR5 | Port 5 data register | R/W | Port 5 | XXXXXXXXB |
| 000006H | PDR6 | Port 6 data register | R/W | Port 6 | XXXXXXXXB |
| 000007H to 00000FH | (system-reserved area) * | | | | |
| 000010H | DDR0 | Port 0 direction register | R/W | Port 0 | 0 0 0 0 0 0 0 0B |
| 000011H | DDR1 | Port 1 direction register | R/W | Port 1 | 0 0 0 0 0 0 0 0B |
| 000012H | DDR2 | Port 2 direction register | R/W | Port 2 | 0 0 0 0 0 0 0 0B |
| 000013H | DDR3 | Port 3 direction register | R/W | Port 3 | 0 0 0 0 0 0 0 0B |
| 000014H | DDR4 | Port 4 direction register | R/W | Port 4 | XXX 0 0 0 0 0B |
| 000015H | DDR5 | Port 5 direction register | R/W | Port 5 | 0 0 0 0 0 0 0 0B |
| 000016H | DDR6 | Port 6 direction register | R/W | Port 6 | XXXX 0 0 0 0B |
| 000017H to 00001AH | (system-reserved area) * | | | | |
| 00001BH | ADER | Analog input enable register | R/W | 8/10-bit A/D converter | 1 1 1 1 1 1 1 1B |
| 00001CH to 00001FH | (system-reserved area) * | | | | |
| 000020H | SMR0 | Serial mode register 0 | R/W | UART0 | 0 0 0 0 0 0 0 0B |
| 000021H | SCR0 | Serial control register 0 | R/W | | 0 0 0 0 0 1 0 0B |
| 000022H | SIDR0/ SODR0 | Serial input data register 0/ Serial output data register 0 | R/W | | XXXXXXXXB |
| 000023H | SSR0 | Serial status register 0 | R/W | | 0 0 0 0 1 X 0 0B |
| 000024H | CDCR0 | Communication prescaler control register 0 | R/W | | 0 XXX 1 1 1 1B |
| 000025H | SES0 | Serial edge selection register 0 | R/W | | XXXXXXX 0B |
| 000026H | SMR1 | Serial mode register 1 | R/W | UART1 | 0 0 0 0 0 0 0 0B |
| 000027H | SCR1 | Serial control register 1 | R/W | | 0 0 0 0 0 1 0 0B |
| 000028H | SIDR1/ SODR1 | Serial input data register 1/ Serial output data register 1 | R/W | | XXXXXXXXB |

*(Continued)*

| Address | Register Abbreviation | Register Name | Access | Resource Name | Initial Value |
|---|---|---|---|---|---|
| 000029H | SSR1 | Serial status register 1 | R/W | UART1 | 0 0 0 0 1 0 0 0B |
| 00002AH | (system-reserved area) * | | | | |
| 00002BH | CDCR1 | Communication prescaler control register 1 | R/W | UART1 | 0 XXX 0 0 0 0B |
| 00002CH to 00002FH | (system-reserved area) * | | | | |
| 000030H | ENIR | DTP/external interrupt enable register | R/W | DTP/external interrupt | 0 0 0 0 0 0 0 0B |
| 000031H | EIRR | DTP/external interrupt condition register | R/W | | XXXXXXXXB |
| 000032H | ELVR | Detection level configuration register | R/W | | 0 0 0 0 0 0 0 0B |
| 000033H | | | R/W | | 0 0 0 0 0 0 0 0B |
| 000034H | ADCS | A/D control status register | R/W | 8/10-bit A/D converter | 0 0 0 0 0 0 0 0B |
| 000035H | | | R/W | | 0 0 0 0 0 0 0 0B |
| 000036H | ADCR | A/D data register | R | | XXXXXXXXB |
| 000037H | | | R/W | | 0 0 1 0 1 XXXB |
| 000038H to 00003FH | (system-reserved area) * | | | | |
| 000040H | PPGC0 | PPG0 operation mode control register | R/W | 8/16-bit PPG timer 0/1 | 0 X 0 0 0 XX 1B |
| 000041H | PPGC1 | PPG1 operation mode control register | R/W | | 0 X 0 0 0 0 0 1B |
| 000042H | PPG01 | PPG0/1 count clock selection register | R/W | | 0 0 0 0 0 0 XXB |
| 000043H | (system-reserved area) * | | | | |
| 000044H | PPGC2 | PPG2 operation mode control register | R/W | 8/16-bit PPG timer 2/3 | 0 X 0 0 0 XX 1B |
| 000045H | PPGC3 | PPG3 operation mode control register | R/W | | 0 X 0 0 0 0 0 1B |
| 000046H | PPG23 | PPG2/3 count clock selection register | R/W | | 0 0 0 0 0 0 XXB |
| 000047H to 00004FH | (system-reserved area) * | | | | |
| 000050H | IPCP0 | Input capture data register 0 | R | 16-bit I/O timer | XXXXXXXXB |
| 000051H | | | | | XXXXXXXXB |
| 000052H | IPCP1 | Input capture data register 1 | R | | XXXXXXXXB |
| 000053H | | | | | XXXXXXXXB |
| 000054H | ICS01 | Input capture control status register | R/W | | 0 0 0 0 0 0 0 0B |
| 000055H | ICS23 | | | | 0 0 0 0 0 0 0 0B |
| 000056H | TCDT | Timer counter data register | R/W | | 0 0 0 0 0 0 0 0B |
| 000057H | | | | | 0 0 0 0 0 0 0 0B |

*(Continued)*

| Address | Register Abbreviation | Register Name | Access | Resource Name | Initial Value |
|---|---|---|---|---|---|
| 000058H | TCCS | Timer counter control status register | R/W | 16-bit I/O timer | 0 0 0 0 0 0 0 0B |
| 000059H | | | | | 0 XXXXXXXB |
| 00005AH | IPCP2 | Input capture data register 2 | R | | XXXXXXXXB |
| 00005BH | | | | | XXXXXXXXB |
| 00005CH | IPCP3 | Input capture data register 3 | R | | XXXXXXXXB |
| 00005DH | | | | | XXXXXXXXB |
| 00005EH to 000065H | (system-reserved area) * | | | | |
| 000066H | TMCSR0 | Timer control status register | R/W | 16-bit reload timer 0 | 0 0 0 0 0 0 0 0B |
| 000067H | | | R/W | | XXXX0 0 0 0B |
| 000068H | TMCSR1 | | R/W | 16-bit reload timer 1 | 0 0 0 0 0 0 0 0B |
| 000069H | | | R/W | | XXXX0 0 0 0B |
| 00006AH to 00006EH | (system-reserved area) * | | | | |
| 00006FH | ROMM | ROM mirror function selection register | W | ROM mirror function selection module | XXXXXXX 1B |
| 000070H to 00007FH | (system-reserved area) * | | | | |
| 000080H | BVALR | Message buffer valid register | R/W | CAN controller | 0 0 0 0 0 0 0 0B |
| 000081H | (system-reserved area) * | | | | |
| 000082H | TREQR | Send request register | R/W | CAN controller | 0 0 0 0 0 0 0 0B |
| 000083H | (system-reserved area) * | | | | |
| 000084H | TCANR | Send cancel register | W | CAN controller | 0 0 0 0 0 0 0 0B |
| 000085H | (system-reserved area) * | | | | |
| 000086H | TCR | Send complete register | R/W | CAN controller | 0 0 0 0 0 0 0 0B |
| 000087H | (system-reserved area) * | | | | |
| 000088H | RCR | Reception complete register | R/W | CAN controller | 0 0 0 0 0 0 0 0B |
| 000089H | (system-reserved area) * | | | | |
| 00008AH | RRTRR | Reception RTR register | R/W | CAN controller | 0 0 0 0 0 0 0 0B |
| 00008BH | (system-reserved area) * | | | | |
| 00008CH | ROVRR | Reception overrun register | R/W | CAN controller | 0 0 0 0 0 0 0 0B |
| 00008DH | (system-reserved area) * | | | | |
| 00008EH | RIER | Reception complete interrupt enable register | R/W | CAN controller | 0 0 0 0 0 0 0 0B |

*(Continued)*

| Address | Register Abbreviation | Register Name | Access | Resource Name | Initial Value |
|---|---|---|---|---|---|
| 00008F$_H$ to 00009D$_H$ | (system-reserved area) * | | | | |
| 00009E$_H$ | PACSR | Address detection control register | R/W | ROM correction function | 0 0 0 0 0 0 0 0$_B$ |
| 00009F$_H$ | DIRR | Delayed interrupt request generate/ cancel register | R/W | Delayed interrupt generation module | XXXXXXX 0$_B$ |
| 0000A0$_H$ | LPMCR | Low power consumption mode control register | R/W | Low-power consumption modes | 0 0 0 1 1 0 0 0$_B$ |
| 0000A1$_H$ | CKSCR | Clock selection register | R/W | Clock | 1 1 1 1 1 1 0 0$_B$ |
| 0000A2$_H$ to 0000A4$_H$ | (system-reserved area) * | | | | |
| 0000A5$_H$ | ARSR | Auto ready function selection register | W | External access | 0 0 1 1 XX 0 0$_B$ |
| 0000A6$_H$ | HACR | High address control register | W | | 0 0 0 0 0 0 0 0$_B$ |
| 0000A7$_H$ | ECSR | Bus control signal selection register | W | | 0 0 0 0 0 0 0 X$_B$ or 0 0 0 0 1 0 0 X$_B$ |
| 0000A8$_H$ | WDTC | Watchdog timer control register | R/W | Watchdog timer | XXXXX 1 1 1$_B$ |
| 0000A9$_H$ | TBTC | Time-base timer control register | R/W | Time-base timer | 1 XX 0 0 1 0 0$_B$ |
| 0000AA$_H$ | WTC | Watch timer control register | R/W | Watch timer | 1 X 0 0 1 0 0 0$_B$ |
| 0000AB$_H$ to 0000AD$_H$ | (system-reserved area) * | | | | |
| 0000AE$_H$ | FMCS | Flash memory control status register | R/W | 512-Kbit flash memory | 0 0 0 X 0 0 0 0$_B$ |
| 0000AF$_H$ | (system-reserved area) * | | | | |
| 0000B0$_H$ | ICR00 | Interrupt control register 00 | R/W | Interrupt controller | 0 0 0 0 0 1 1 1$_B$ |
| 0000B1$_H$ | ICR01 | Interrupt control register 01 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000B2$_H$ | ICR02 | Interrupt control register 02 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000B3$_H$ | ICR03 | Interrupt control register 03 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000B4$_H$ | ICR04 | Interrupt control register 04 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000B5$_H$ | ICR05 | Interrupt control register 05 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000B6$_H$ | ICR06 | Interrupt control register 06 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000B7$_H$ | ICR07 | Interrupt control register 07 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000B8$_H$ | ICR08 | Interrupt control register 08 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000B9$_H$ | ICR09 | Interrupt control register 09 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000BA$_H$ | ICR10 | Interrupt control register 10 | R/W | | 0 0 0 0 0 1 1 1$_B$ |

*(Continued)*

| Address | Register Abbreviation | Register Name | Access | Resource Name | Initial Value |
|---|---|---|---|---|---|
| 0000BB$_H$ | ICR11 | Interrupt control register 11 | R/W | Interrupt controller | 0 0 0 0 0 1 1 1$_B$ |
| 0000BC$_H$ | ICR12 | Interrupt control register 12 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000BD$_H$ | ICR13 | Interrupt control register 13 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000BE$_H$ | ICR14 | Interrupt control register 14 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000BF$_H$ | ICR15 | Interrupt control register 15 | R/W | | 0 0 0 0 0 1 1 1$_B$ |
| 0000C0$_H$ to 0000FF$_H$ | (system-reserved area) * | | | | |
| 001FF0$_H$ | PADR0 | Detection address configuration register 0 (lower) | R/W | ROM correction function | XXXXXXXX$_B$ |
| 001FF1$_H$ | | Detection address configuration register 0 (mid) | R/W | | XXXXXXXX$_B$ |
| 001FF2$_H$ | | Detection address configuration register 0 (upper) | R/W | | XXXXXXXX$_B$ |
| 001FF3$_H$ | PADR1 | Detection address configuration register 1 (lower) | R/W | | XXXXXXXX$_B$ |
| 001FF4$_H$ | | Detection address configuration register 1 (mid) | R/W | | XXXXXXXX$_B$ |
| 001FF5$_H$ | | Detection address configuration register 1 (upper) | R/W | | XXXXXXXX$_B$ |
| 003900$_H$ | TMR0/ TMRLR0 | 16-bit timer register 0/ 16-bit reload register 0 | R/W | 16-bit reload timer 0 | XXXXXXXX$_B$ |
| 003901$_H$ | | | | | XXXXXXXX$_B$ |
| 003902$_H$ | TMR1/ TMRLR1 | 16-bit timer register 1/ 16-bit reload register 1 | R/W | 16-bit reload timer 1 | XXXXXXXX$_B$ |
| 003903$_H$ | | | | | XXXXXXXX$_B$ |
| 003904$_H$ to 00390F$_H$ | (system-reserved area) * | | | | |
| 003910$_H$ | PRLL0 | PPG0 reload register L | R/W | 8/16-bit PPG timer | XXXXXXXX$_B$ |
| 003911$_H$ | PRLH0 | PPG0 reload register H | R/W | | XXXXXXXX$_B$ |
| 003912$_H$ | PRLL1 | PPG1 reload register L | R/W | | XXXXXXXX$_B$ |
| 003913$_H$ | PRLH1 | PPG1 reload register H | R/W | | XXXXXXXX$_B$ |
| 003914$_H$ | PRLL2 | PPG2 reload register L | R/W | | XXXXXXXX$_B$ |
| 003915$_H$ | PRLH2 | PPG2 reload register H | R/W | | XXXXXXXX$_B$ |
| 003916$_H$ | PRLL3 | PPG3 reload register L | R/W | | XXXXXXXX$_B$ |
| 003917$_H$ | PRLH3 | PPG3 reload register H | R/W | | XXXXXXXX$_B$ |
| 003918$_H$ to 003BFF$_H$ | (system-reserved area) * | | | | |
| 003C00$_H$ to 003C0F$_H$ | RAM (general-purpose RAM) | | | | |

*(Continued)*

| Address | Register Abbreviation | Register Name | Access | Resource Name | Initial Value |
|---|---|---|---|---|---|
| 003C10H to 003C13H | IDR0 | ID register 0 | R/W | CAN controller | XXXXXXXXB to XXXXXXXXB |
| 003C14H to 003C17H | IDR1 | ID register 1 | R/W | | XXXXXXXXB to XXXXXXXXB |
| 003C18H to 003C1BH | IDR2 | ID register 2 | R/W | | XXXXXXXXB to XXXXXXXXB |
| 003C1CH to 003C1FH | IDR3 | ID register 3 | R/W | | XXXXXXXXB to XXXXXXXXB |
| 003C20H to 003C23H | IDR4 | ID register 4 | R/W | | XXXXXXXXB to XXXXXXXXB |
| 003C24H to 003C27H | IDR5 | ID register 5 | R/W | | XXXXXXXXB to XXXXXXXXB |
| 003C28H to 003C2BH | IDR6 | ID register 6 | R/W | | XXXXXXXXB to XXXXXXXXB |
| 003C2CH to 003C2FH | IDR7 | ID register 7 | R/W | | XXXXXXXXB to XXXXXXXXB |
| 003C30H, 003C31H | DLCR0 | DLC register 0 | R/W | | XXXXXXXXB XXXXXXXXB |
| 003C32H, 003C33H | DLCR1 | DLC register 1 | R/W | | XXXXXXXXB XXXXXXXXB |
| 003C34H, 003C35H | DLCR2 | DLC register 2 | R/W | | XXXXXXXXB XXXXXXXXB |
| 003C36H, 003C37H | DLCR3 | DLC register 3 | R/W | | XXXXXXXXB XXXXXXXXB |
| 003C38H, 003C39H | DLCR4 | DLC register 4 | R/W | | XXXXXXXXB XXXXXXXXB |
| 003C3AH, 003C3BH | DLCR5 | DLC register 5 | R/W | | XXXXXXXXB XXXXXXXXB |
| 003C3CH, 003C3DH | DLCR6 | DLC register 6 | R/W | | XXXXXXXXB XXXXXXXXB |
| 003C3EH, 003C3FH | DLCR7 | DLC register 7 | R/W | | XXXXXXXXB XXXXXXXXB |
| 003C40H to 003C47H | DTR0 | Data register 0 | R/W | | XXXXXXXXB to XXXXXXXXB |

*(Continued)*

| Address | Register Abbreviation | Register Name | Access | Resource Name | Initial Value |
|---|---|---|---|---|---|
| 003C48H to 003C4FH | DTR1 | Data register 1 | R/W | CAN controller | XXXXXXXXB to XXXXXXXXB |
| 003C50H to 003C57H | DTR2 | Data register 2 | R/W | | XXXXXXXXB to XXXXXXXXB |
| 003C58H to 003C5FH | DTR3 | Data register 3 | R/W | | XXXXXXXXB to XXXXXXXXB |
| 003C60H to 003C67H | DTR4 | Data register 4 | R/W | | XXXXXXXXB to XXXXXXXXB |
| 003C68H to 003C6FH | DTR5 | Data register 5 | R/W | | XXXXXXXXB to XXXXXXXXB |
| 003C70H to 003C77H | DTR6 | Data register 6 | R/W | | XXXXXXXXB to XXXXXXXXB |
| 003C78H to 003C7FH | DTR7 | Data register 7 | R/W | | XXXXXXXXB to XXXXXXXXB |
| 003C80H to 003CFFH | (system-reserved area) * | | | | |
| 003D00H, 003D01H | CSR | Control status register | R/W | CAN controller | 0 XXXX 0 0 1B<br>0 0 XXX 0 0 0B |
| 003D02H | LEIR | Display last event register | R/W | | 0 0 0 XX 0 0 0B |
| 003D03H | (system-reserved area) * | | | | |
| 003D04H, 003D05H | RTEC | Receive/transmit error counter | R | CAN controller | 0 0 0 0 0 0 0 0B<br>0 0 0 0 0 0 0 0B |
| 003D06H, 003D07H | BTR | Bit timing register | R/W | | 1 1 1 1 1 1 1 1B<br>X 1 1 1 1 1 1 1B |
| 003D08H | IDER | IDE register | R/W | | XXXXXXXXB |
| 003D09H | (system-reserved area) * | | | | |
| 003D0AH | TRTRR | Transmit RTR register | R/W | CAN controller | 0 0 0 0 0 0 0 0B |
| 003D0BH | (system-reserved area) * | | | | |
| 003D0CH | RFWTR | Remote frame reception standby register | R/W | CAN controller | XXXXXXXXB |
| 003D0DH | (system-reserved area) * | | | | |
| 003D0EH | TIER | Transmit complete interrupt enable register | R/W | CAN controller | 0 0 0 0 0 0 0 0B |

*(Continued)*

*(Continued)*

| Address | Register Abbreviation | Register Name | Access | Resource Name | Initial Value |
|---|---|---|---|---|---|
| 003D0F$_H$ | (system-reserved area) * | | | | |
| 003D10$_H$, 003D11$_H$ | AMSR | Acceptance mask selection register | R/W | CAN controller | XXXXXXXX$_B$ XXXXXXXX$_B$ |
| 003D12$_H$, 003D13$_H$ | (system-reserved area) * | | | | |
| 003D14$_H$ to 003D17$_H$ | AMR0 | Acceptance mask register 0 | R/W | CAN controller | XXXXXXXX$_B$ to XXXXXXXX$_B$ |
| 003D18$_H$ to 003D1B$_H$ | AMR1 | Acceptance mask register 1 | R/W | | XXXXXXXX$_B$ to XXXXXXXX$_B$ |
| 003D1C$_H$ to 003FFF$_H$ | (system-reserved area) * | | | | |

Explanation of reset values
0 : The reset value of this bit is 0.
1 : The reset value of this bit is 1.
X : The reset value of this bit is undefined.

* : System-reserved area contains system-internal addresses, and cannot be used.

## ■ INTERRUPT CONDITIONS AND INTERRUPT VECTOR/REGISTER

| Interrupt Condition | EI²OS Compatible | Interrupt Vector | | | Interrupt Register | | Priority *3 |
|---|---|---|---|---|---|---|---|
| | | Number | | Address | ICR | Address | |
| Reset | × | #08 | 08H | FFFFDCH | — | — | Highest |
| INT 9 instruction | × | #09 | 09H | FFFFD8H | — | — | ↑ |
| Exception processing | × | #10 | 0AH | FFFFD4H | — | — | |
| Can controller reception complete (RX) | × | #11 | 0BH | FFFFD0H | ICR00 | 0000B0H (*1) | |
| Can controller reception complete (TX) / Node status transition (NS) | × | #12 | 0CH | FFFFCCH | | | |
| Reserved | × | #13 | 0DH | FFFFC8H | ICR01 | 0000B1H | |
| Reserved | × | #14 | 0EH | FFFFC4H | | | |
| External interrupt (INT0/INT1) | △ | #15 | 0FH | FFFFC0H | ICR02 | 0000B2H (*1) | |
| Time-base timer | × | #16 | 10H | FFFFBCH | | | |
| 16-bit reload timer 0 | △ | #17 | 11H | FFFFB8H | ICR03 | 0000B3H (*1) | |
| 8/10-bit A/D converter | △ | #18 | 12H | FFFFB4H | | | |
| 16-bit free-run timer overflow | △ | #19 | 13H | FFFFB0H | ICR04 | 0000B4H (*1) | |
| External interrupt (INT2/INT3) | △ | #20 | 14H | FFFFACH | | | |
| Reserved | × | #21 | 15H | FFFFA8H | ICR05 | 0000B5H (*2) | |
| PPG timer ch.0, ch.1 underflow | × | #22 | 16H | FFFFA4H | | | |
| Input capture 0 load | △ | #23 | 17H | FFFFA0H | ICR06 | 0000B6H (*1) | |
| External interrupt (INT4/INT5) | △ | #24 | 18H | FFFF9CH | | | |
| Input capture 1 load | △ | #25 | 19H | FFFF98H | ICR07 | 0000B7H (*1) | |
| PPG timer ch.2, ch.3 underflow | × | #26 | 1AH | FFFF94H | | | |
| External interrupt (INT6/INT7) | △ | #27 | 1BH | FFFF90H | ICR08 | 0000B8H (*1) | |
| Watch timer | △ | #28 | 1CH | FFFF8CH | | | |
| Reserved | × | #29 | 1DH | FFFF88H | ICR09 | 0000B9H (*1) | |
| Input capture 2 load<br>Input capture 3 load | × | #30 | 1EH | FFFF84H | | | |
| Reserved | × | #31 | 1FH | FFFF80H | ICR10 | 0000BAH (*1) | |
| Reserved | × | #32 | 20H | FFFF7CH | | | |
| Reserved | × | #33 | 21H | FFFF78H | ICR11 | 0000BBH (*1) | |
| Reserved | × | #34 | 22H | FFFF74H | | | |
| Reserved | × | #35 | 23H | FFFF70H | ICR12 | 0000BCH (*1) | |
| 16-bit reload timer 1 | ○ | #36 | 24H | FFFF6CH | | | |
| UART1 reception complete | ◎ | #37 | 25H | FFFF68H | ICR13 | 0000BDH (*1) | |
| UART1 transmission complete | △ | #38 | 26H | FFFF64H | | | |

*(Continued)*

*(Continued)*

| Interrupt Condition | EI²OS Compatible | Interrupt Vector | | | Interrupt Register | | Priority *3 |
|---|---|---|---|---|---|---|---|
| | | Number | | Address | ICR | Address | |
| UART0 reception complete | ◎ | #39 | 27H | FFFF60H | ICR14 | 0000BEH (*1) | ↓ Lowest |
| UART0 transmission complete | △ | #40 | 28H | FFFF5CH | | | |
| Flash memory | × | #41 | 29H | FFFF58H | ICR15 | 0000BFH (*1) | |
| Delayed interrupt generation module | × | #42 | 2AH | FFFF54H | | | |

○ : Available
× : Not available
◎ : Available, EI²OS halt function supplied
△ : Available for interrupt conditions not shared by ICR

*1 : • The interrupt level is the same for peripheral devices sharing the ICR register.
• Peripheral devices that share the ICR register and use the extended intelligent I/O service only utilize one set.
• If one side of a peripheral device sharing the ICR register is set to extended intelligent I/O service, the other side cannot use interrupts.

*2 : Only the 16-bit reload timer is compatible with EI²OS. Since PPG does not support EI²OS, if you use EI²OS with the 16-bit reload timer, prohibit interrupts by PPG.

*3 : Priority if two or more interrupts with the same level are generated simultaneously.

## ■ PERIPHERAL RESOURCES

### 1. I/O Port

#### (1) Overview

General-purpose (parallel) I/O ports can be used as the I/O ports. The MB90495G Series has 7 ports (49) .

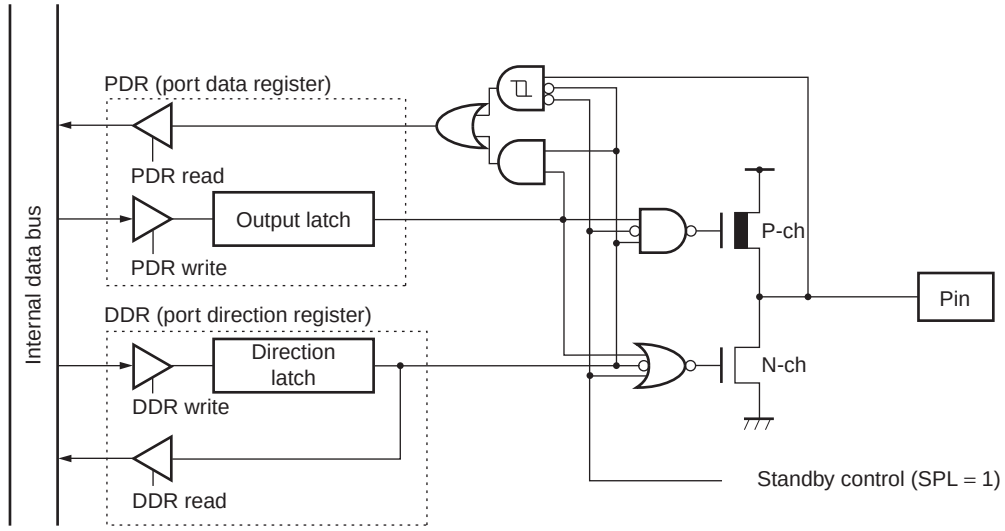
Each port doubles as a peripheral device I/O pin.

**• I/O Port Features**

I/O ports output data to I/O pins and load signals input to them, by means of the port data register (PDR) . Additionally, the port direction register (DDR) sets the I/O direction of the I/O pins at the bit level. Below is a description of each pin's function, and the peripheral device that shares it.

- Port 0 : general-purpose I/O port/doubles as external address data bus pin
- Port 1 : general-purpose I/O port/doubles as PPG timer output, input capture input, and external address data bus pin
- Port 2 : general-purpose I/O port/doubles as reload timer I/O, external interrupt input pin, and external address bus pin
- Port 3 : general-purpose I/O port/doubles as UART0 I/O, free-run timer, and A/D converter startup trigger pin
- Port 4 : general-purpose I/O port/doubles as UART1 I/O, and CAN controller transmit/receive pin
- Port 5 : general-purpose I/O port/doubles as analog input pin
- Port 6 : general-purpose I/O port/doubles as external interrupt input pin

- **Pin Block Diagram for Port 0 (single chip mode)**



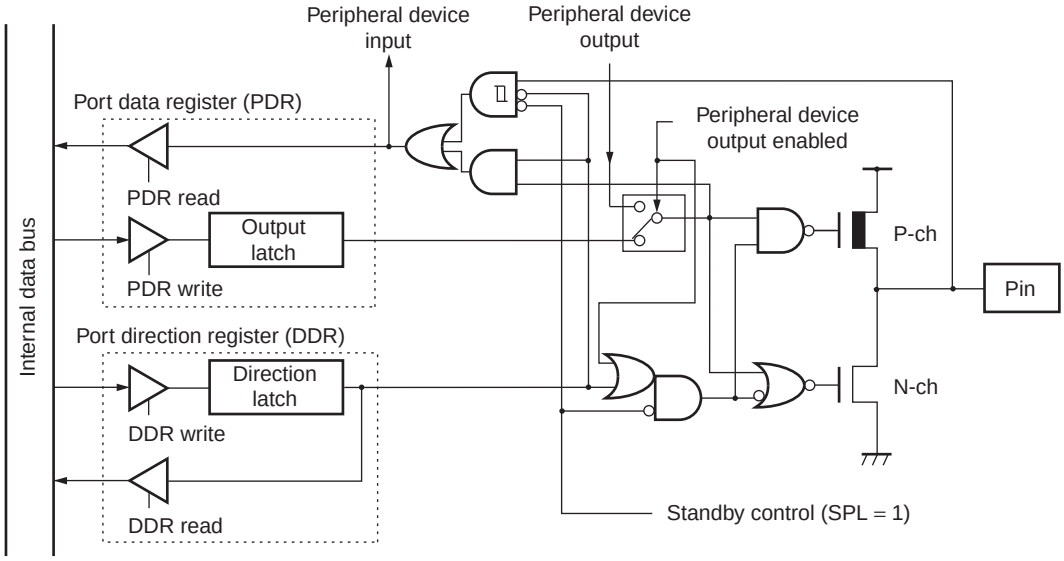

Standby control : control stop mode (SPL = 1) , time-base timer mode (SPL = 1) and watch mode (SPL = 1)

- **Port 0 register (single chip mode)**
  - The port 0 register contains the port 0 data register (PDR0) and the port 0 direction register (DDR0) .
  - The bits making up the register are in a one-to-one relation to the port 0 pin.

**Compatibility between port 0 register and pin**

| Port Name | Related register bit and corresponding pin | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Port 0 | PDR0, DDR0 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| | Corresponding pin | P07 | P06 | P05 | P04 | P03 | P02 | P01 | P00 |

- **Block Diagram for Pins of Ports 1, 2, 3 and 4 (single-chip mode)**




Standby control : control stop mode (SPL = 1) , time-base timer mode (SPL = 1) and watch mode (SPL = 1)

- **Port 1 register (single-chip mode)**
- The port1 register contains the port 1 data register (PDR1) and the port 1 direction register (DDR1) .
- The bits making up the register are in a one-to-one relationship with the port 1 pins.

**Port 1 Register and Corresponding Pins**

| Port Name | Related register bit and corresponding pin | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Port 1 | PDR1, DDR1 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| | Corresponding pin | P17 | P16 | P15 | P14 | P13 | P12 | P11 | P10 |

- **Port 2 register**
- The port2 register contains the port 2 data register (PDR2) , the port 2 direction register (DDR2) and the high address control register (HACR).
- The high address control register (HACR) enables or disables the output of external addresses (A16 to A23). When the register enables the output of the external addresses, the port can not be used as a peripheral device and a general-purpose I/O port.
- The bits making up the register are in a one-to-one relationship with the port 2 pins.

**Port 2 Register and Corresponding Pins**

| Port Name | Related register bit and corresponding pin | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Port 2 | PDR2, DDR2, HACR | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| | Corresponding pin | P27 | P26 | P25 | P24 | P23 | P22 | P21 | P20 |

- **Port 3 register**
- The port3 register contains the port 3 data register (PDR3) and the port 3 direction register (DDR3) .
- The bus control signal selection register (ECSR) enables or disables the input and output of external bus control signals ($\overline{WRL}$ / $\overline{WRH}$, HRQ / $\overline{HAK}$, RDY, CLK). When the register enables the input and output of the external bus control signals, the port can not be used as a peripheral device and a general-purpose I/O port.
- The bits making up the register are in a one-to-one relationship with the port 3 pins.

**Port 3 Register and Corresponding Pins**

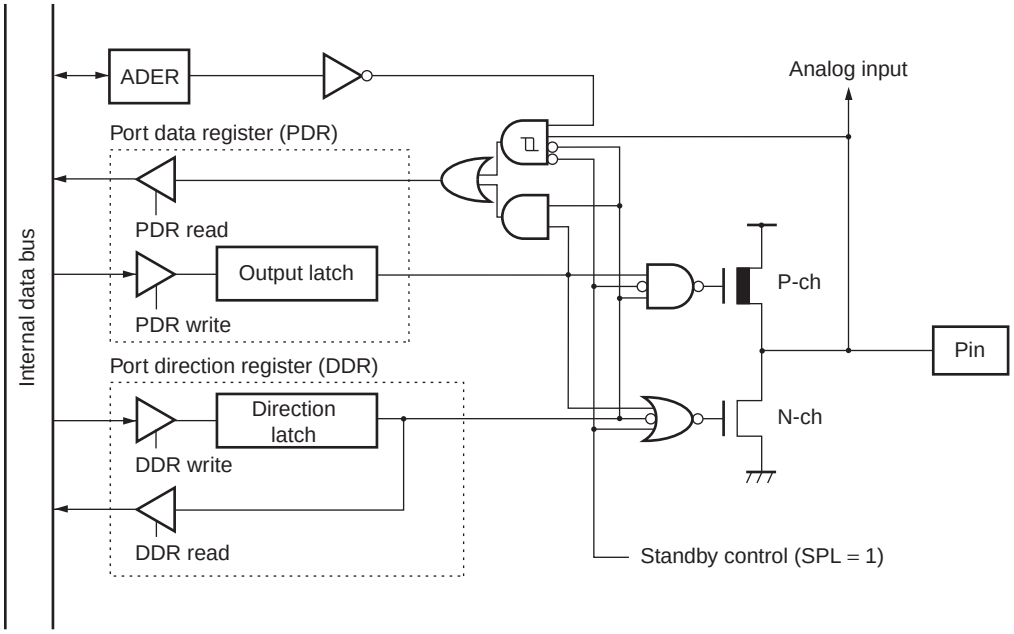
| Port Name | Related register bit and corresponding pin | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Port 3 | PDR3, DDR3 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| | ECSR | CKE | RYE | HDE | | WRE | | — | |
| | Corresponding pin | P37 | P36 | P35 | P34 | P33 | P32 | P31 | P30 |

- **Port 4 register**
- The port4 register contains the port 4 data register (PDR4) and the port 4 direction register (DDR4) .
- The bits making up the register are in a one-to-one relationship with the port 4 pins.

**Port 4 Register and Corresponding Pins**

| Port Name | Related register bit and corresponding pin | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Port 4 | PDR4, DDR4 | — | — | — | bit4 | bit3 | bit2 | bit1 | bit0 |
| | Corresponding pin | — | — | — | P44 | P43 | P42 | P41 | P40 |

- **Block Diagram of Port 5 Pins**



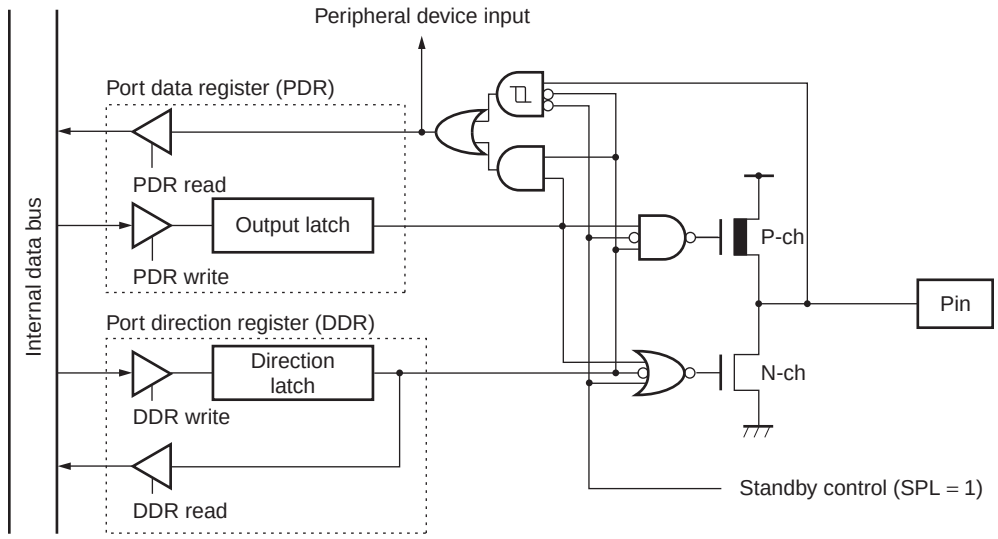

Standby control : control stop mode (SPL = 1) , time-base timer mode (SPL = 1) , and watch mode (SPL = 1)

- **Port 5 register**
- The port 5 register contains the port 5 data register (PDR5) , the port 5 direction register (DDR5) and the analog input enable register (ADER) .
- The analog data enable register (ADER) enables or disables the input of analog signals by the analog input pin.
- The bits making up the register are in a one-to-one correspondence with the pins of port 5.

**Port 5 Register and Corresponding Pins**

| Port Name | Related register bit and corresponding pin | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Port 5 | PDR5, DDR5 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| | ADER | ADE7 | ADE6 | ADE5 | ADE4 | ADE3 | ADE2 | ADE1 | ADE0 |
| | Corresponding pin | P57 | P56 | P55 | P54 | P53 | P52 | P51 | P50 |

- **Block Diagram of Port 6 Pins**




Standby control : control stop mode (SPL = 1) , time-base timer mode (SPL = 1) , and watch mode (SPL = 1)

- **Port 6 register**
- The port 6 register contains the port 6 data register (PDR6) and the port 6 direction register (DDR6) .
- The bits making up the register are in a one-to-one relationship with the port 6 pins.

**Port 6 Register and Corresponding Pins**

| Port Name | Related register bit and corresponding pin | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Port 6 | PDR6, DDR6 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| | Corresponding pin | — | — | — | — | P63 | P62 | P61 | P60 |

## 2. Time-base Timer

The time-base timer is an 18-bit free-run counter (time-base counter) for counting up in synchronization with the main clock (1/2 main oscillation clock) .

- Four interval times are available, and interrupt requests can be generated for each interval time.
- The time-base timer also has a function for supplying timers for oscillation stabilize standby time and operating clocks for peripheral devices.

- **Interval timer feature**
- When the time-base timer counter reaches the interval set by the interval time selection bits (TBTC : TBC1, TBC0) , it generates an overflow (TBTC : TBOF = 1) and interrupt request.
- If the interrupts due to overflow generation are enabled (TBTC : TBIE = 1) , when an overflow is generated (TBTC : TBOF = 1) , an interrupt is generated.
- Select from the following 4 time-base timer intervals :

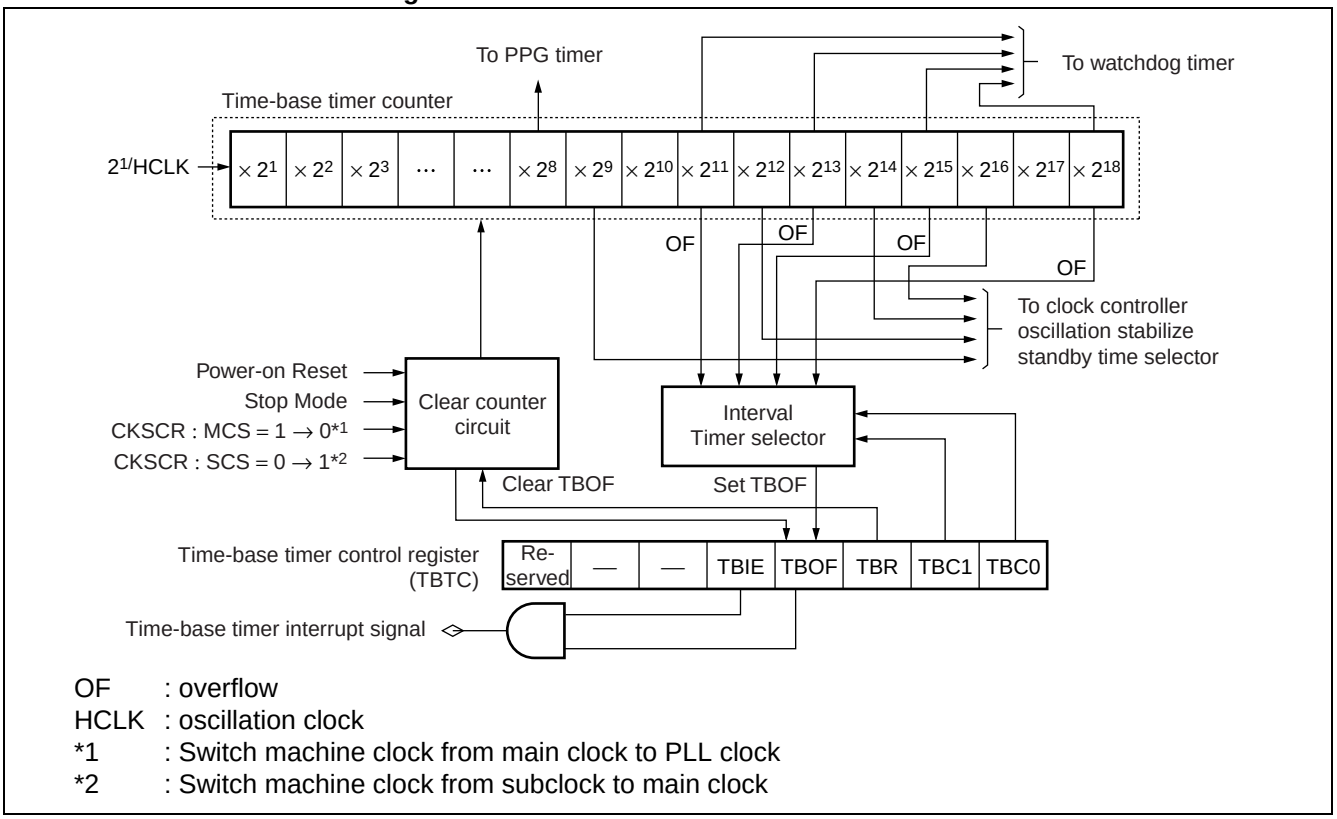
**Time-base timer interval times**

| Count Clock | Interval Time |
|---|---|
| 2/HCLK (0.5 µs) | $2^{12}$/HCLK (approx. 1.0 ms) |
| | $2^{14}$/HCLK (approx. 4.1 ms) |
| | $2^{16}$/HCLK (approx. 16.4 ms) |
| | $2^{19}$/HCLK (approx. 131.1 ms) |

HCLK : oscillation clock

The number in parentheses ( ) for 4-MHz oscillation clock operation

- **Time-base Timer Block Diagram**




OF : overflow
HCLK : oscillation clock
*1 : Switch machine clock from main clock to PLL clock
*2 : Switch machine clock from subclock to main clock

See below for the actual interrupt request number of the time-base timer :
Interrupt request number : #16 ($10_H$)

## 3. Watchdog Timer

The watchdog timer is a 2-bit timer used as a count clock for the timer-based or watch timer.

If the counter is not cleared within the interval time, it resets the CPU.

- **Watchdog Timer Function**
  - The watchdog timer is a timer counter used to deal with runaway programs. Once the watchdog timer is launched, it is necessary to keep clearing its counter within the specified interval. If the specified interval passes without the watchdog timer counter being cleared, the CPU will be reset. This feature is called the watchdog timer.
  - The watchdog timer interval traces back to the clock interval input as the count clock. A watchdog reset is generated for the smallest to largest times.
  - The clock source output destination is set by the watchdog clock selection bit of the watch timer control register (WTC : WDCS) .
  - The watchdog timer interval is set time-base timer output selection bit/watch timer output selection bit of the watchdog timer control register (WDTC : WT1, WT0) .

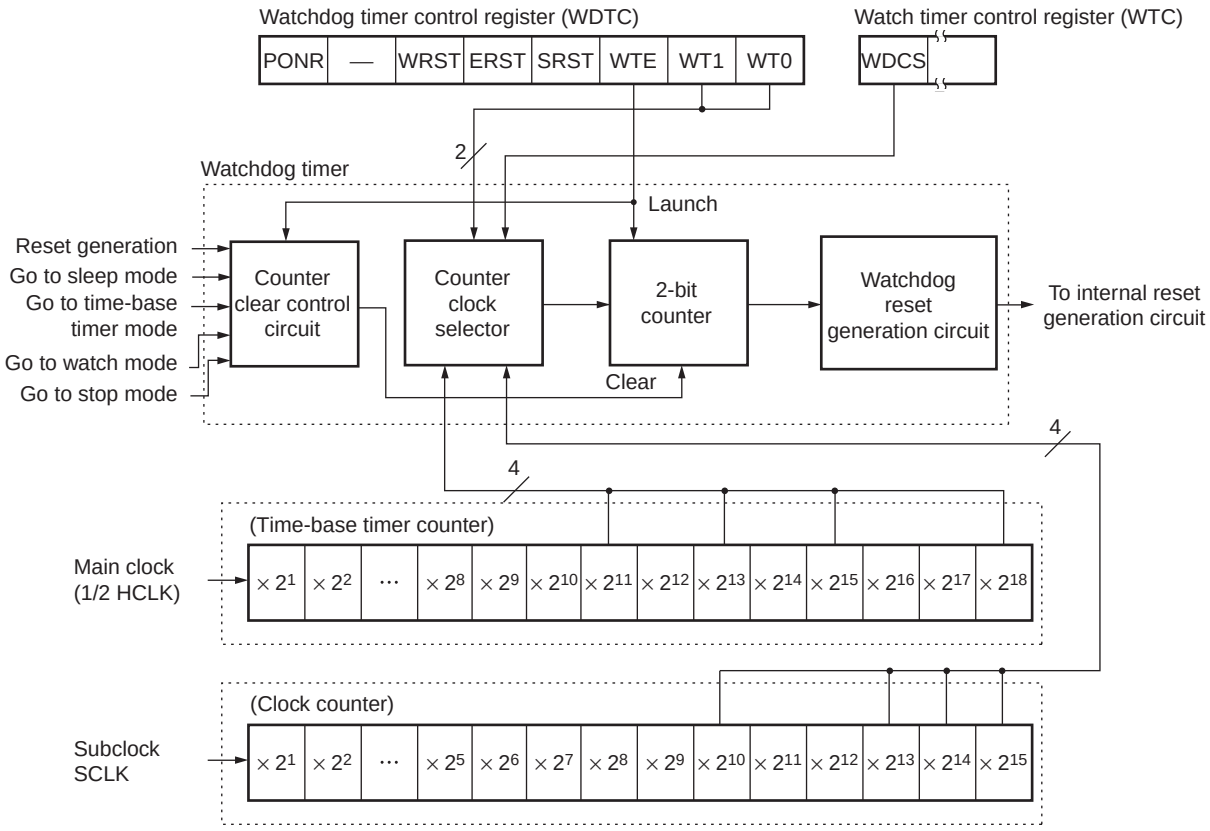
**Watchdog Timer Intervals**

| Minimum | Maximum | Clock Interval | Minimum | Maximum | Clock Interval |
|---|---|---|---|---|---|
| Approx. 3.58 ms | Approx. 4.61 ms | $2^{14} \pm 2^{11}$/ HCLK | Approx. 0.457 s | Approx. 0.576 s | $2^{12} \pm 2^{9}$/ SCLK |
| Approx. 14.33 ms | Approx. 18.3 ms | $2^{16} \pm 2^{13}$/ HCLK | Approx. 3.584 s | Approx. 4.608 s | $2^{15} \pm 2^{12}$/ SCLK |
| Approx. 57.23 ms | Approx. 73.73 ms | $2^{18} \pm 2^{15}$/ HCLK | Approx. 7.168 s | Approx. 9.216 s | $2^{16} \pm 2^{13}$/ SCLK |
| Approx. 458.75 ms | Approx. 589.82 ms | $2^{21} \pm 2^{18}$/ HCLK | Approx. 14.336 s | Approx. 18.432 s | $2^{17} \pm 2^{14}$/ SCLK |

HCLK : oscillation clock (4 MHz) ; SCLK : Subclock (8.192 kHz)

Notes: • If the count clock of the watchdog timer is set to time-base timer output (overflow signal) , then clearing the time-base timer could make it take longer to reset the watchdog.
• If you are using a subclock as the machine clock, make sure to select watch timer output by setting the watchdog timer clock source selection bit (WDCS) of the watch timer control register (WTC) to 0.

- **Watchdog Timer Block Diagram**




HCLK : Oscillation clock
SCLK : Subclock

## 4. 16-bit I/O Timer

The 16-bit I/O timer is a complex module comprising one 16-bit free-run timer, and two input capture units (4 input pins) . Clock interval input signals and pulse widths can be measured based on the 16-bit free-run timer.

- **16-bit I/O Timer Configuration**
  The 16-bit I/O timer is made up of the following modules :
  - One 16-bit free-run timer
  - Two input capture units (each unit having 2 input pins)
- **16-bit I/O Timer Function**

### (1) 16-bit free-run timer function

The 16-bit free-run timer consists of a 16-bit up counter, a time counter control status register, and prescaler. The 16-bit up counter counts up in synchronization with a fraction of the machine clock.

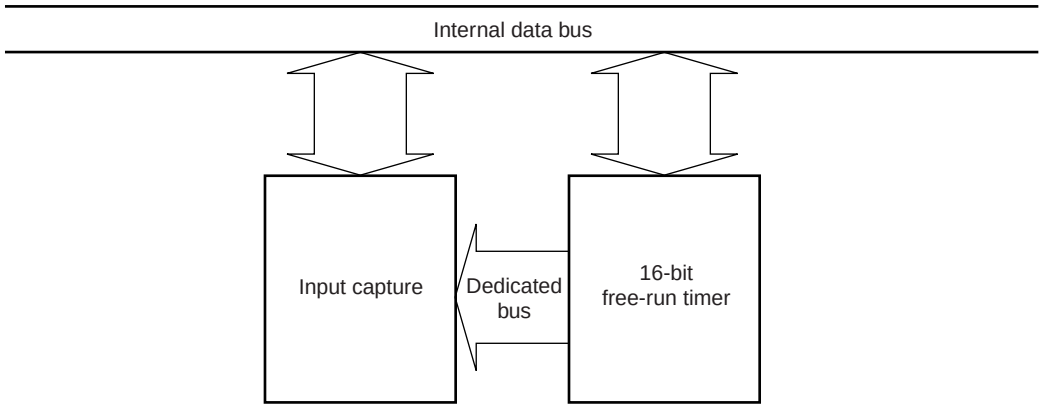
- The count clock can be set to one of eight fractions of the machine clock. The external clock signals input to the 16-bit free-run timer clock input pin (FRCK) can be used as the count clock.
- Interrupts can be generated in response to counter value overflows.
- Interrupts launch the extended intelligent I/O service (EI$^2$OS) .
- The count value of the 16-bit free-run timer can be cleared to "0000$_H$" by either a reset, or software clear via the timer count clear bit (TCCS : CLR) .
- The count value of the 16-bit free-run timer is output to the input capture, and used as the base time for capture operation.

### (2) Input Capture Function

When the input capture detects that an external signal edge has been input to an input pin, it stores the count value of the 16-bit free-run timer in the input capture data register, for the point at which the edge was detected. The input capture consists of an input capture register corresponding to four I/O pins, an input capture control status register, and an edge detection circuit.

- When an edge is detected, either rising, falling, or both can be selected.
- An interrupt request can be generated to the CPU when an input signal edge is detected.
- Interrupts launch the extended intelligent I/O service (EI$^2$OS) .
- Since the input capture has four pairs of input pins and input capture data registers, it can measure up to 4 phenomena.

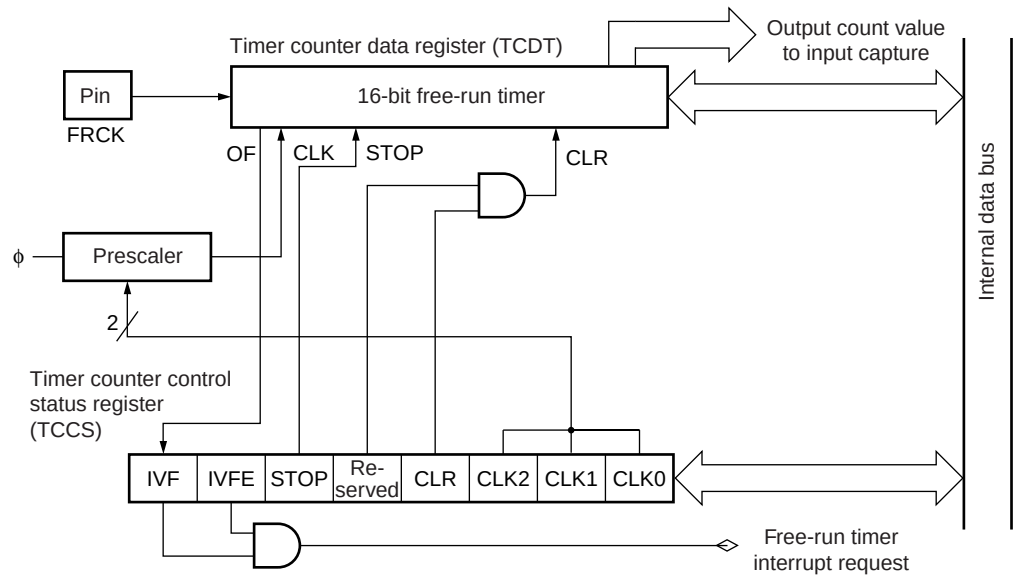
- **Block Diagram of 16-bit I/O Timer**




16-bit free-run timer: The counter value of the 16-bit free-run timer is used as the base time of the input capture.

Input capture: Input capture detects rising, falling and both edges for external signals input to input pins, and stores the counter value of the 16-bit free-run timer. Interrupts can be generated in response to input signal edge detection.

- **Block Diagram of 16-bit Free-run Timer**




ϕ : Machine clock
OF : overflow

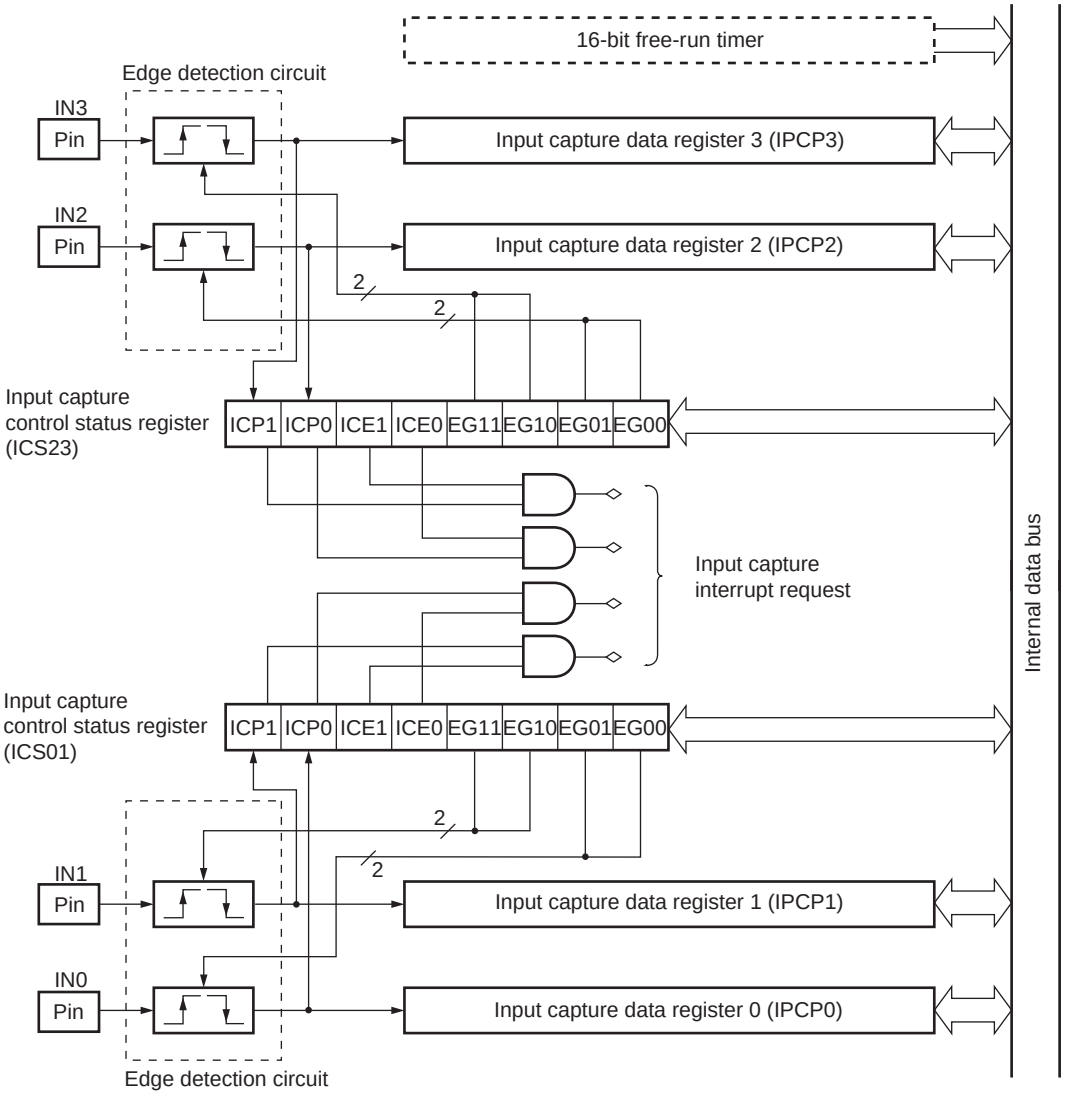
Note: The 16-bit I/O timer contains one 16-bit free-run timer.
The interrupt request number of the 16-bit free-run timer is as follows :
Interrupt request number : 19 ($13_H$)

Prescaler: Takes a fraction of the machine clock, and supplies a count clock to the 16-bit up-counter. One of four machine clock fractions can be selected by setting the timer counter control status register (TCCS) .

Timer Counter Register (TCDT) :
This is a 16-bit up-counter. It is possible to read the current counter value of the 16-bit free-run timer by reading this counter. The counter can be set to an arbitrary value by writing to it while stopped.

Timer Counter Control Status Register (TCCS) :
TCCS selects the divide ratio of a machine clock, executes software clear of counter values. and enables or disables counter operation. Also TCCS confirms and clears an overflow generation flag, and enables or disables interruption.

- **Input Capture Block Diagram**



## 5. 16-bit Reload Timer

The functions of the 16-bit reload timer are as follows :

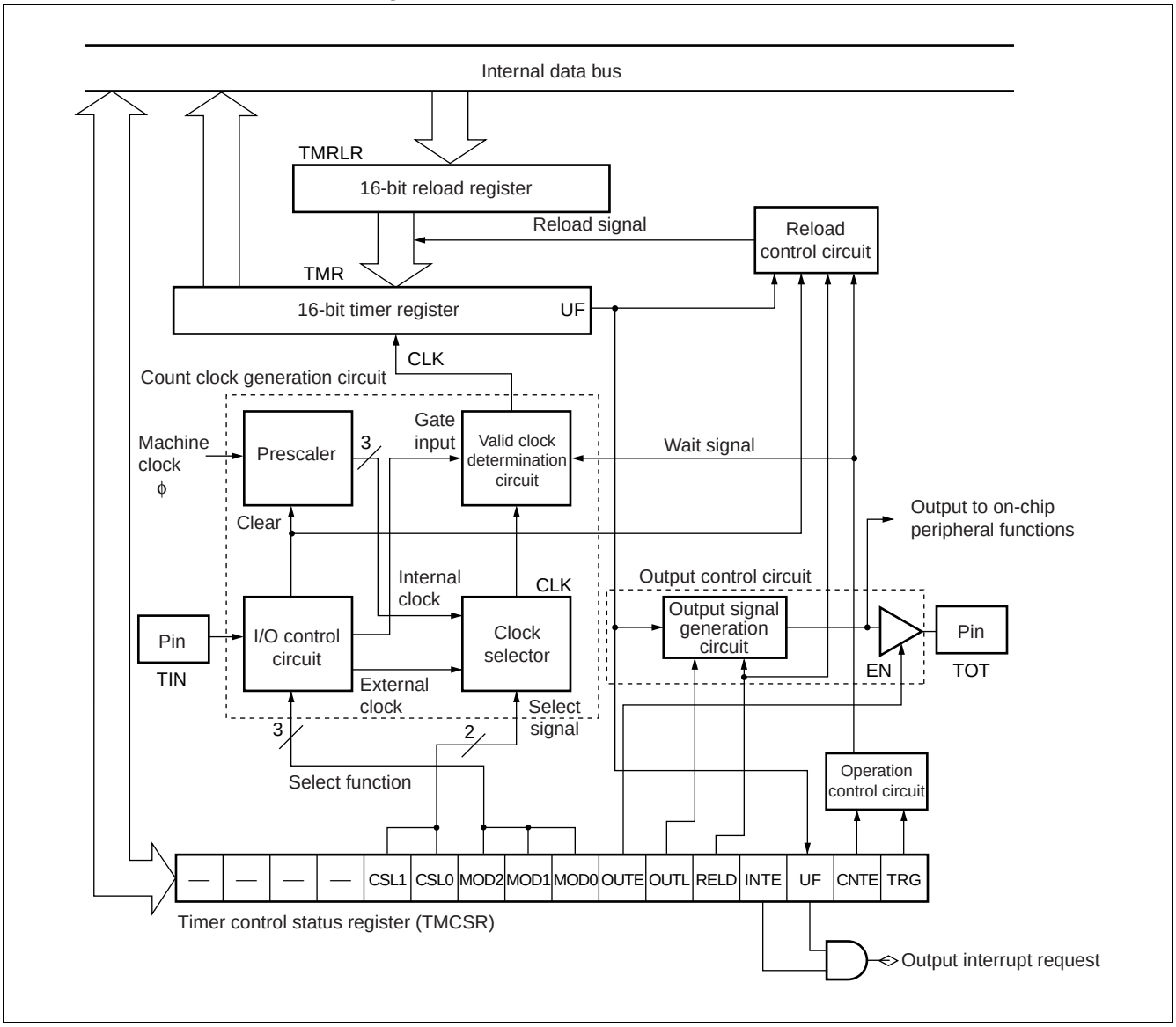
- Choose one of three internal clocks or an external event clock as the count clock.
- Choose a software or external launch trigger.
- An interrupt can be sent to the CPU in response to an underflow generated by the 16-bit timer register. Interrupts can be used to utilize the timer as an interval timer.
- When an underflow is generated by the 16-bit timer register (TMR) , select one-shot mode, where TMR counter operation is halted, or reload mode, where the 16-bit reload register value is reloaded, and TMR count operation continues.
- Supports extended intelligent I/O service (EI$^2$OS) .
- The MB90495G Series features two on-chip 16-bit reload timer channels.

- **16-bit Reload Timer Operation Mode**

| Count Clock | Launch Trigger | Operation in Case of Underflow |
|---|---|---|
| Internal clock mode | Software trigger<br>External trigger | One-shot mode<br>Reload mode |
| Event count mode | Software trigger | One-shot mode<br>Reload mode |

- **Internal Clock Mode**
- Set the count clock selection bits of the timer control status register (TMCSR : CSL1, CSL0) to “$00_B$”, “$01_B$” or “$10_B$” to set the 16-bit reload timer to internal clock mode.
- In internal clock mode, the timer counts down in synchronization with the internal clock.
- Set the count clock selection bits of the timer control status register (TMCSR : CSL1, CSL0) to select one of three count clock intervals.
- Select software-triggered or externally triggered (edge detection) launch.

- **16-bit Reload Timer Block Diagram**



## 6. Watch Timer

The watch timer is a 15-bit free-run counter that counts up in synchronization with the subclock.

- Eight different intervals can be selected, and interrupt requests generated for each interval time.
- Supplies a timer for subclock oscillation stabilization standby, and an operational clock for the watchdog timer.
- The subclock is always the count clock, regardless of the clock selection register (CKSCR) setting.

- **Interval timer feature**
- When the interval time set by the interval time selection bits (WTC : WTC2 to WTC0) is reached, the clock timer generates an overflow in the bits corresponding to the interval time of the watch timer counter, and sets the overflow flag bit (WTC : WTOF = 1) .
- Interrupts arising from overflows are enabled (WTC : WTIE = 1) , an interrupt request is generated when the overflow flag bit is set (WTC : WTOF = 1) .
- Select from one of the following 8 watch timer intervals :

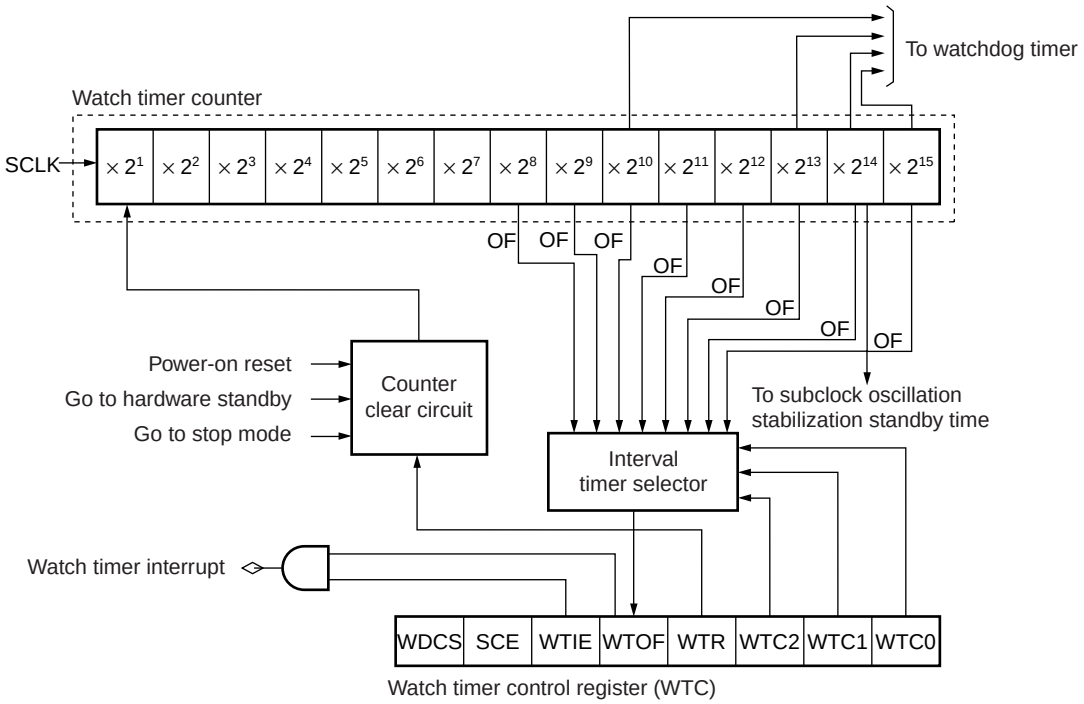
**Clock Timer Interval Times**

| Subclock Frequency | Interval Time |
|---|---|
| 1/SCLK (122 μs) | $2^8$/SCLK (31.25 ms) |
| | $2^9$/SCLK (62.5 ms) |
| | $2^{10}$/SCLK (125 ms) |
| | $2^{11}$/SCLK (250 ms) |
| | $2^{12}$/SCLK (500 ms) |
| | $2^{13}$/SCLK (1.0 s) |
| | $2^{14}$/SCLK (2.0 s) |
| | $2^{15}$/SCLK (4.0 s) |

SCLK : Subclock frequency

Figures in parentheses ( ) are a sample calculation with the subclock running at 8.192 kHz.

- **Watch Timer Block Diagram**




OF : Overflow
SCLK : Subclock

Notes: The actual interrupt request number generated by the watch timer is as follows :
Interrupt request number : #28 ($1C_H$)

Watch timer counter: 15-bit up counter using the subclock (SCLK) as its count clock.

Counter clear circuit: This circuit clears the watch timer counter.

## 7. 8/16-Bit PPG

The 8/16-bit PPG timer is a 2-channel reload timer module (PPG0, PPG1) capable of arbitrary synchronization and pulse output of duty ratio. Combining the 2 channel module can yield the following behavior :

- 8-bit PPG output, 2-channel independent operation mode
- 16-bit PPG output operation mode
- 8 + 8-bit PPG output operation mode

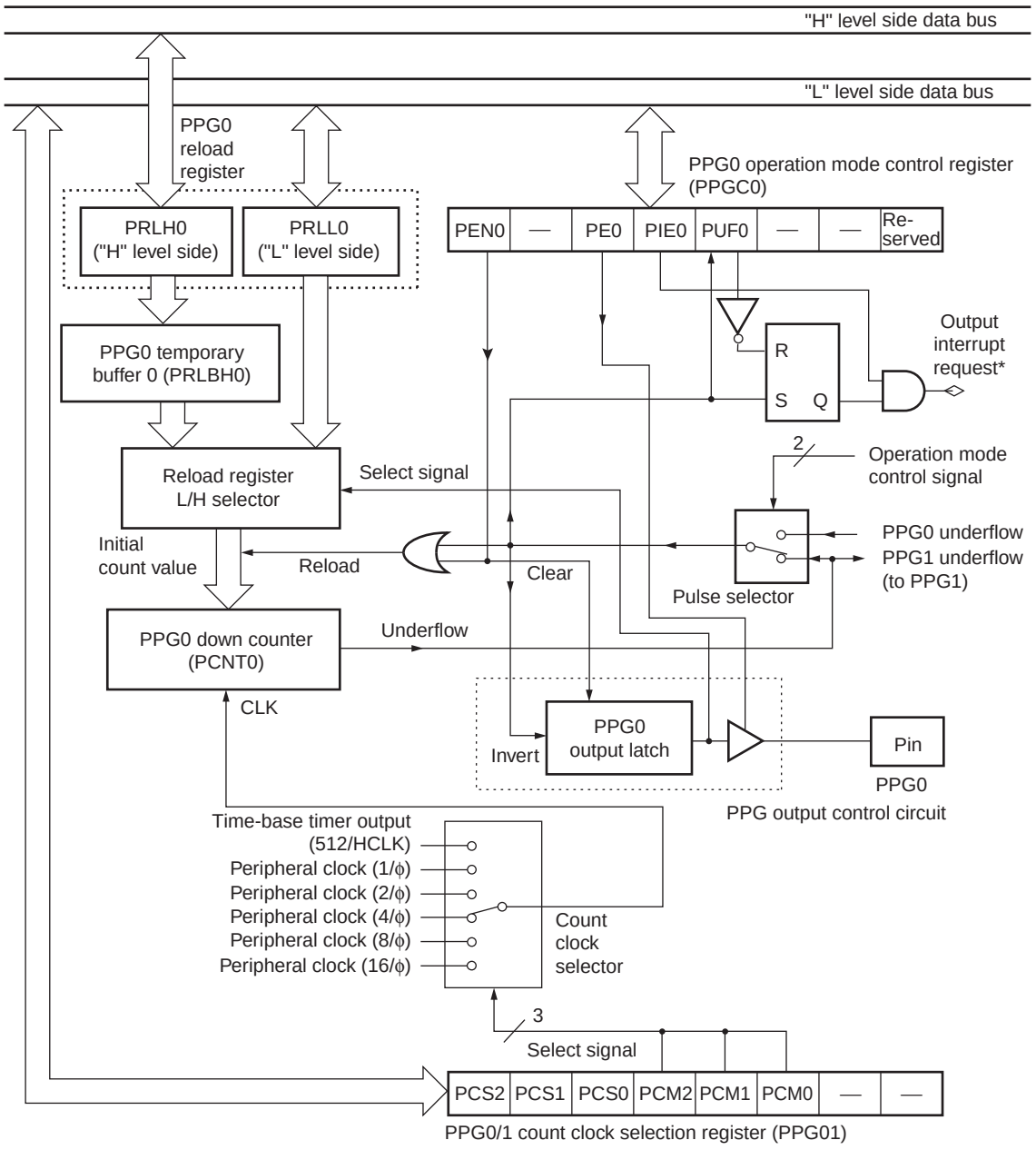
The MB90495G Series features two on-chip, 8/16-bit PPG timers. This section describes the functions of PPG0/1. PPG2/3 has the same functions as PPG0/1.

### • 8/16-bit PPG Timer Functions

The 8/16-bit PPG timer is made up of four 8-bit reload registers (PRLH0/PRLL0, PRLH1/PRLL1) , and two PPG down counters (PCNT0, PCNT1) .

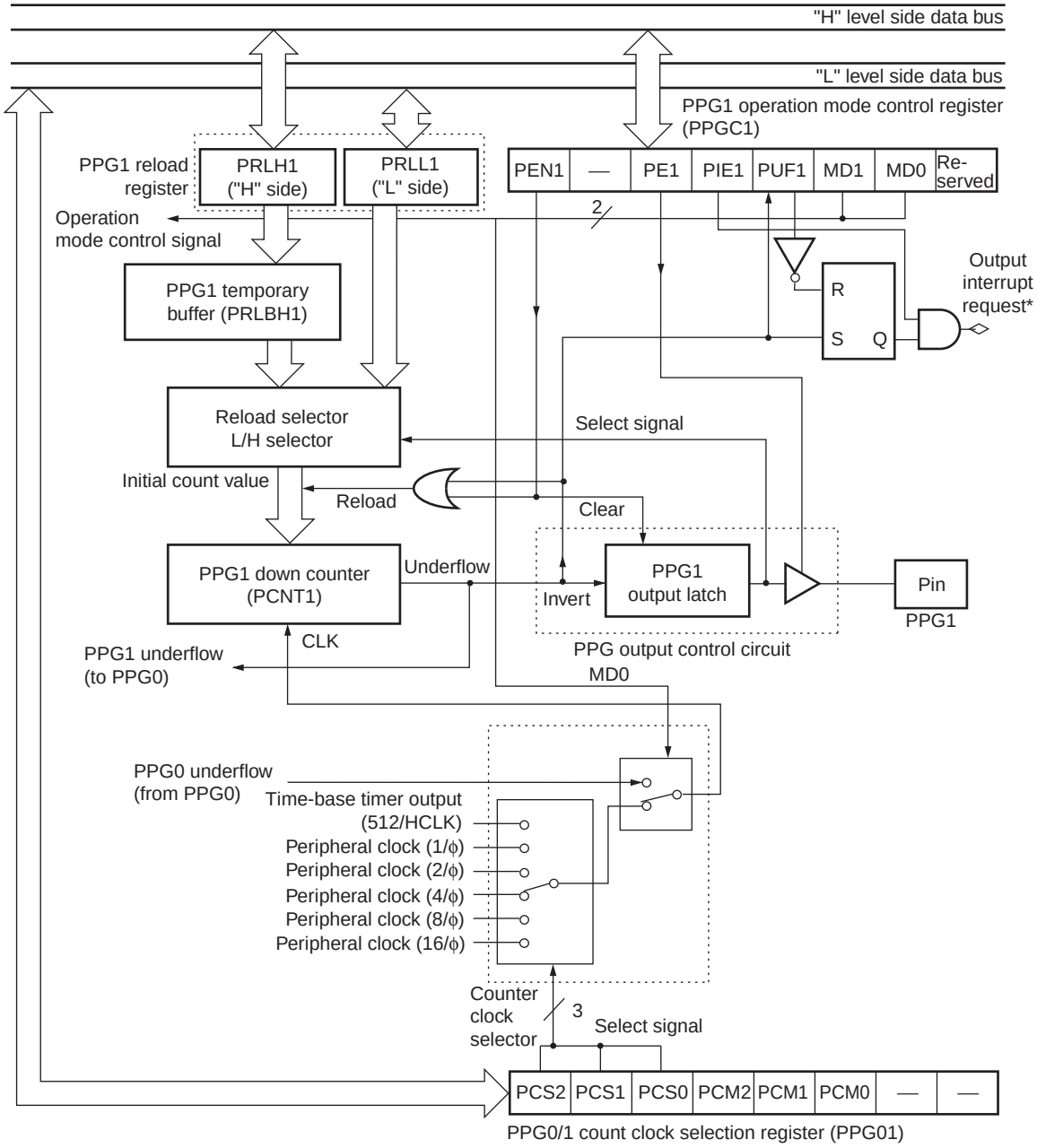
- Since you can set each output pulse to “H” or “L” width independently, the interval and duty ratio of each pulse can be set to an arbitrary value.
- Select one of 6 internal clocks as the count clock.
- Interrupt requests can be generated for each interval time, allowing the timer to be used as an interval timer.
- The use of an external circuit allows the timer to be used as a D/A converter.

- **Block Diagram of 8/16-Bit PPG Timer 0**




| | |
|---|---|
| — | : Undefined |
| Reserved | : Reserved bit |
| HCLK | : Oscillation clock frequency |
| ϕ | : Machine clock frequency |
| * | : Interrupt output from 8/16-bit PPG timer 0 is merged with interrupt request output from PPG timer 1 into a single interrupt via an OR circuit. |

- **Block Diagram of 8/16-Bit PPG Timer1**




| | |
|---|---|
| — | : Undefined |
| Reserved | : Reserved bit |
| HCLK | : Oscillation clock frequency |
| ϕ | : Machine clock frequency |
| * | : Interrupt output from 8/16-bit PPG timer 1 is merged with interrupt request output from PPG timer 0 into a single interrupt via an OR circuit. |

## 8. Delayed Interrupt Generation Module

The delayed interrupt generation module generates interrupts for switching tasks.

This module can be used to generate hardware interrupts from the software.

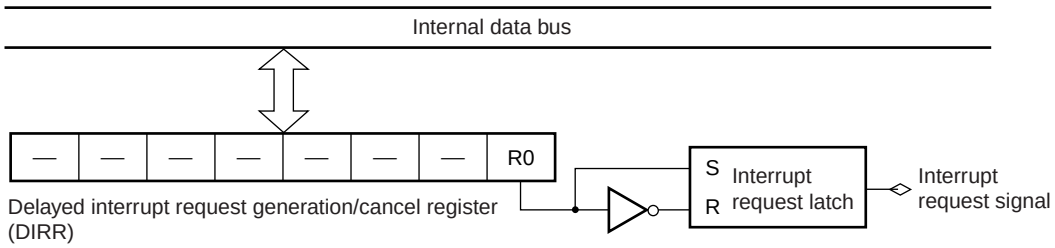
- **Overview of the Delayed Interrupt Generation Module**

  Use the delayed interrupt generation module to generate or cancel hardware interrupts from the software.

**Overview of the Delayed Interrupt Generation Module**

| | Functions and Control |
|---|---|
| Interrupt Condition | When the R0 bit of the delayed interrupt request generation/cancel register is set to 1 (DIRR : R0 = 1) : Generate interrupt request<br>When the R0 bit of the delayed interrupt request generation/cancel register is set to 0 (DIRR : R0 = 0) : Cancel interrupt request |
| Interrupt number | #42 ($2A_H$) |
| Interrupt control | There is no enable setting from the register |
| Interrupt flag | Stored in bit DIRR : R0 |
| EI$^2$OS | Does not support extended intelligent I/O service |

- **Delayed Interrupt/Generation Module Block Diagram**




— : Undefined

Interrupt request latch: This latch stores the delayed interrupt request generation/cancel register setting (generates/cancels delayed interrupt requests) .

Delayed interrupt request generation/cancel register (DIRR) : Generates or cancels delayed interrupt requests.

- **Interrupt number**

  Below is the interrupt number used by the delayed interrupt generation module.

  Interrupt number : #42 ($2A_H$)

## 9. DTP/External Interrupts

The DTP/external interrupt transmits interrupt requests or data transfer requests generated by peripheral devices to the CPU, generates external interrupt request, and starts the extended intelligent I/O service (EI$^2$OS) .

- **DTP/External Interrupt Functions**

Outputs interrupt requests from external peripheral devices to the CPU using the same procedure as for peripheral functions, and generates external interrupts, or starts the extended intelligent I/O service (EI$^2$OS) .

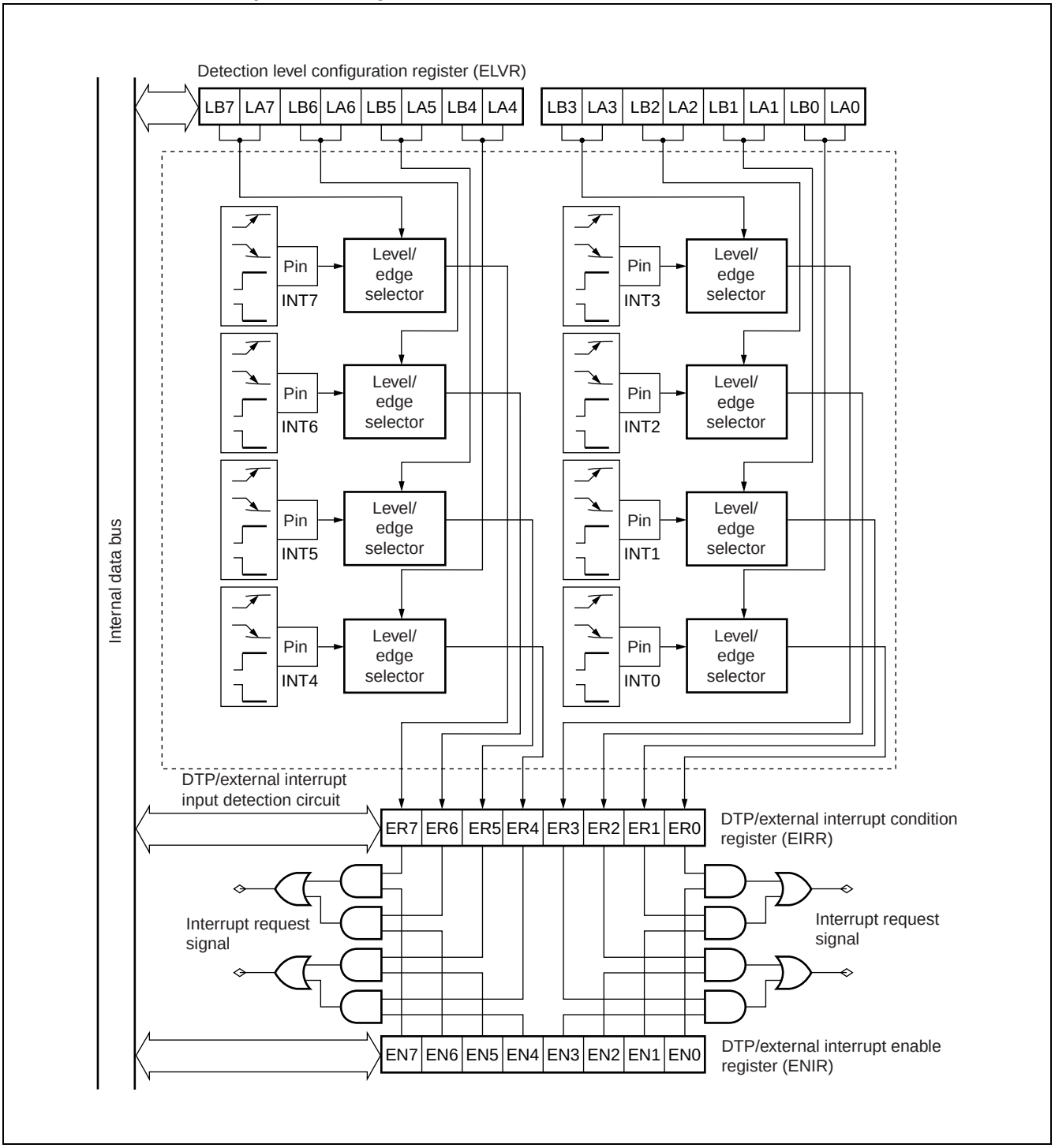
If the interrupt control register is configured to prohibit the extended intelligent I/O service (EI$^2$OS) (ICR : ISE = 0) , then the external interrupt feature becomes valid, and the process branches into interrupt processing.

If the EI$^2$OS is enabled (ICR : ISE = 1) , then the DTP function becomes valid, and the EI$^2$OS automatically transmits data, and after transmitting data a specified number of times, branches into interrupt processing.

**Overview of DTP/External Interrupts**

| | External interrupt | DTP functions |
|---|---|---|
| Input pins | 8 (INT0 to INT7) | |
| Interrupt condition | Each pin sets individually in the detection level configuration register (ELVR) | |
| | “H” / “L” level/rising edge/falling edge input | “H” / “L” level input |
| Interrupt numbers | #15 ($0F_H$) , #20 ($14_H$) , #24 ($18_H$) , #27 ($1B_H$) | |
| Interrupt control | The DTP/external interrupt enable register (ENIR) enables or prohibits interrupt request output | |
| Interrupt flag | Interrupt conditions stored by DTP/external interrupt condition register (EIRR) | |
| Process selection | Set EI$^2$OS to be prohibited (ICR : ISE = 0) | Set EI$^2$OS to be enabled (ICR : ISE = 1) |
| Processing | Branch to external interrupt process | After the EI$^2$OS conducts automatic data forwarding the specified number of times, branches to interrupt processing. |

- **DTP/External Interrupt Block Diagram**



## 10. 8/10-bit A/D Converter

The 8/10-bit A/D converter converts analog voltage to 8 or 10-bit digital values, by means of RC successive approximation conversion.

- The input signal can be selected from an 8-channel analog input pin set.
- Select a software trigger, internal timer output, or external trigger as the start trigger.

- **Functions of the 8/10-bit A/D Converter**

Converts analog voltage (input voltage) input to the analog input pins to 8-bit or 10-bit digital values. (A/D conversion)

The 8/10-bit A/D converter has the following features :

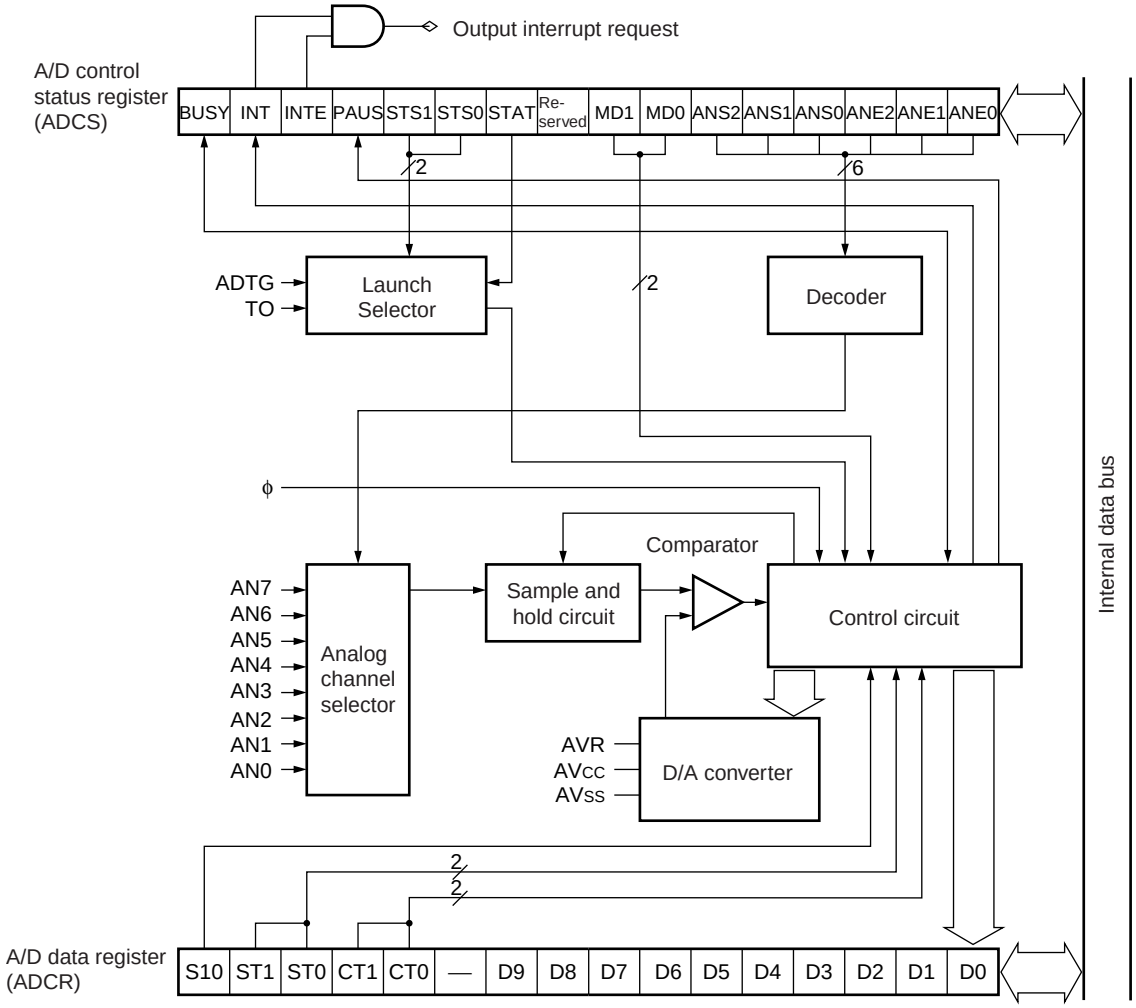
- Single-channel A/D conversion time is a minimum of 6.12 µs, including sampling time.*
- Single-channel sampling time is a minimum of 2.0 µs.*
- RC-type successive approximation with sampling and hold circuits is used for conversion.
- Select 8 or 10-bit resolution.
- Analog input pins can use up to 8 channels.
- A/D conversion results are stored in the A/D data register, allowing them to be used to generate interrupts.
- Interrupt requests launch the EI$^2$OS. Use the EI$^2$OS to prevent dropped data even with continuous A/D conversion.
- Select software, internal timer output, or external trigger (falling edge) as the start trigger.

* : With machine clock operating at 16 MHz

- **Conversion Modes of the 8/10-bit A/D Converter**

| Conversion Mode | Description |
|---|---|
| Single conversion mode | Conducts A/D conversion for each channel in turn, from the start channel to the end channel. When A/D conversion of the end channel is completed, the A/D conversion function halts. |
| Continuous conversion mode | Conducts A/D conversion for each channel in turn, from the start channel to the end channel. When A/D conversion of the end channel is completed, the function returns to the start channel and continues A/D conversion. |
| Stop conversion mode | Suspends each channel and conducts A/D conversion, one at a time. When A/D conversion of the end channel is completed, the function returns to the start channel and repeats the A/D conversion and channel stop. |

- **8/10-bit A/D Converter Block Diagram**




TO : Internal timer output
— : Undefined
Reserved : Make sure this is always set to “01”
ϕ : Machine clock

## 11. UART0/1

The UART is a general-purpose serial data communications interface for synchronous or asynchronous communication with external devices.

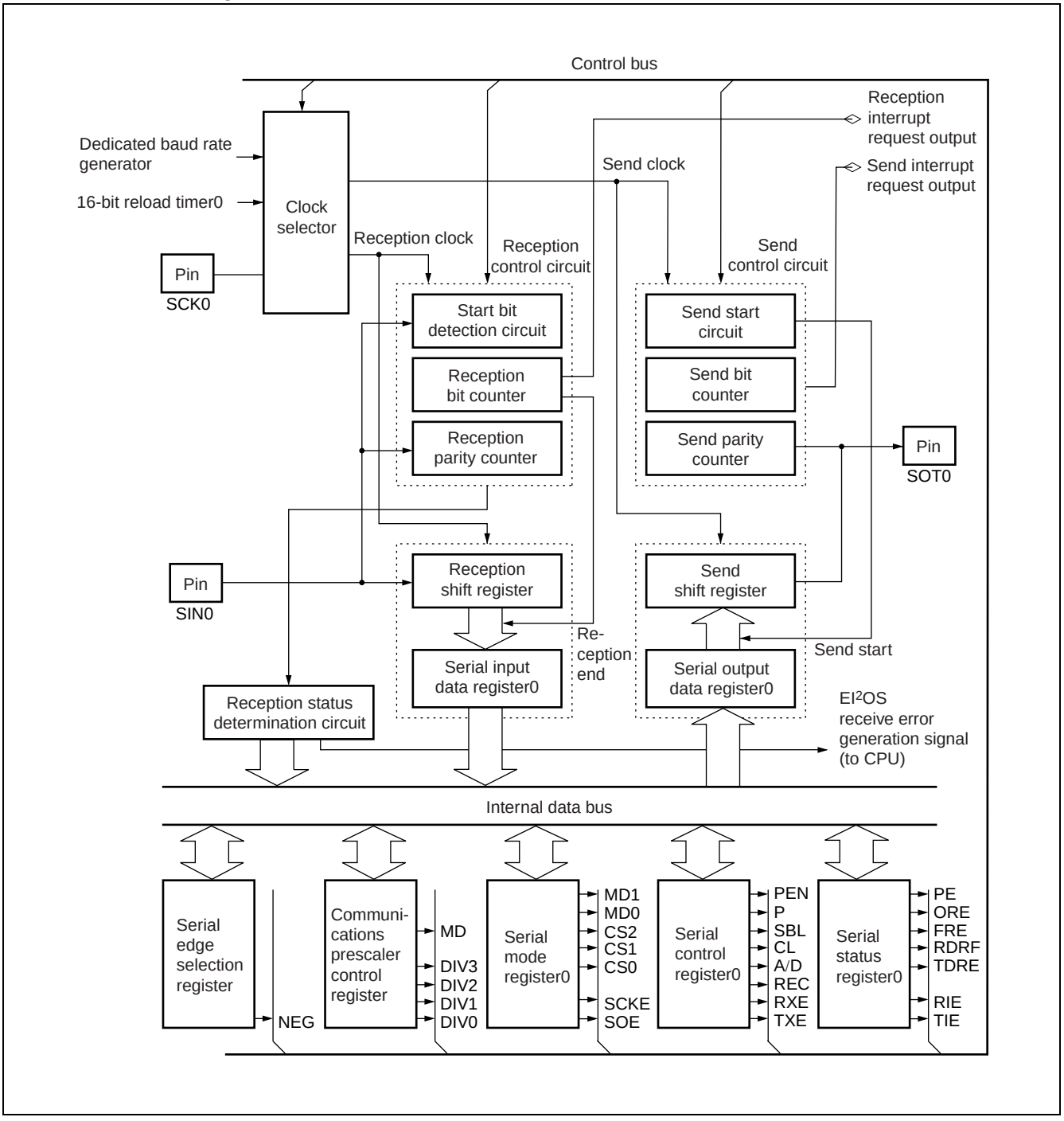
- The UART has a clock-synchronous/clock-asynchronous two-way communications feature .
- Also supplies a master/slave communications feature (multi-processor mode) . (It can be used only master side.)
- Interrupts can be generated upon send complete, receive complete, or reception error detection.
- Supports extended intelligent I/O service (EI$^2$OS) .

- **UART0/1 Functions**

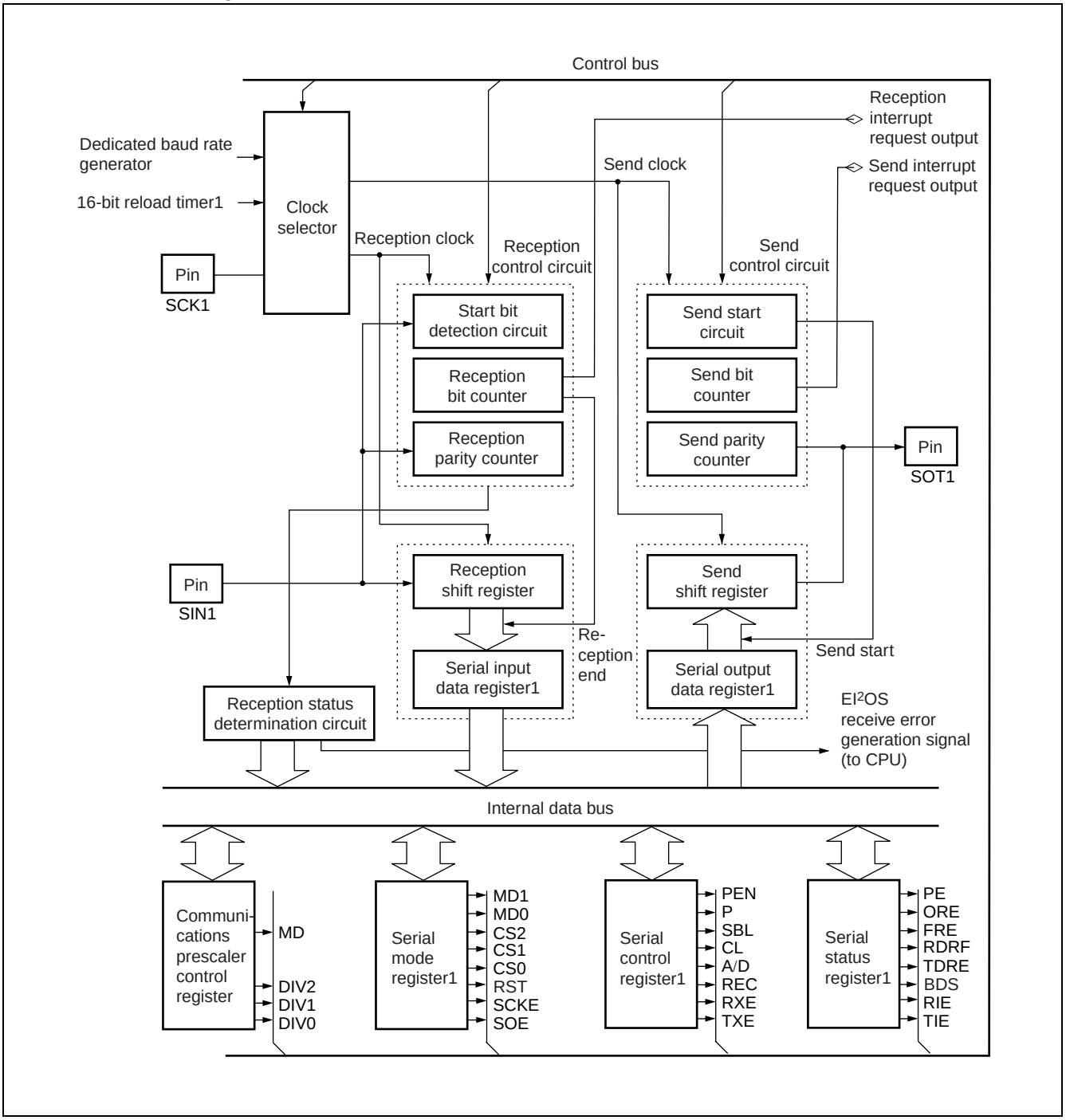
| | **Functions** |
|---|---|
| Data Buffer | Full-duplex double buffer |
| Transfer mode | • Clock-synchronous (no start, stop, or parity bit)<br>• Clock-asynchronous (start-stop synchronization) |
| Baud Rate | • Select from 8 dedicated baud rate generators<br>• External clock input possible<br>• Clock supplied from internal timer (16-bit reload timer) available |
| Data length | • 7-bit (asynchronous normal mode only)<br>• 8-bit |
| Signal method | Non Return to Zero (NRZ) |
| Reception Error Detection | • Framing error<br>• Overrun error<br>• Parity error (not available in operation mode 1 (multi processor mode) ) |
| Interrupt Requests | • Receive interrupt (reception complete, reception error detected)<br>• Send interrupt (send complete)<br>• Both send and receive support extended intelligent I/O service (EI$^2$OS) |
| Master/Slave Communications Function (In multiprocessor mode) | 1-to-n (master to slave) communication available (can only be used as master) |

Note : During clock-synchronous forwarding, just the data is forwarded, with no stop or start bit appended.

- **UART0 Block Diagram**



- **UART1 Block Diagram**



## 12. CAN Controller

CAN (Controller Area Network) is a serial communications protocol conforming to CAN version 2.0 A and B. Sending and receiving is available in standard and extended frame format.

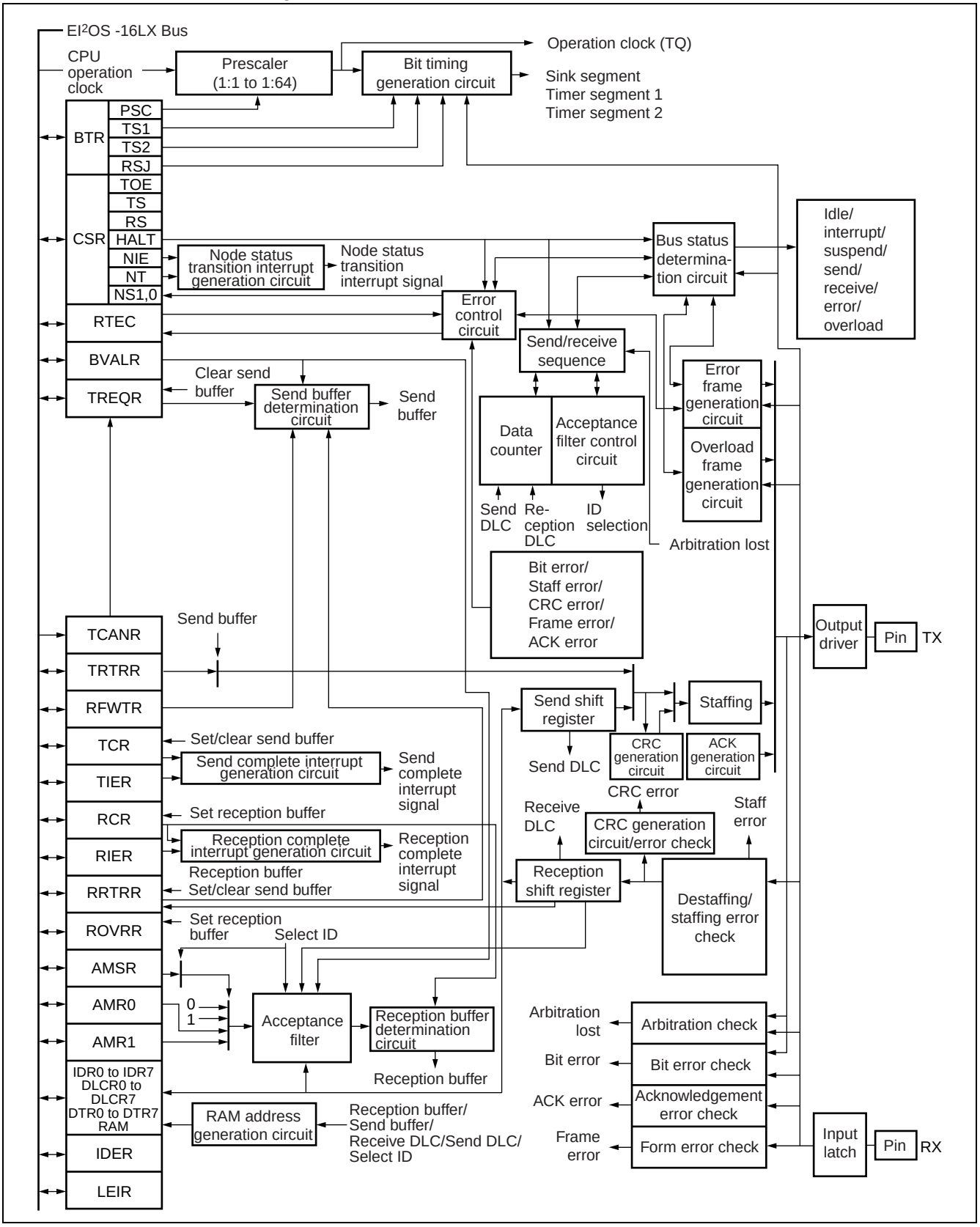
- **Can Controller Features**
- The CAN controller format conforms to CAN versions 2.0 A and B.
- Sending and receiving is available in standard and extended frame format.
- Supports automatic data frame formatting through remote frame reception.
- Baud rate : 10 kbps to 1 Mbps. When using at 1 Mbps, the machine clock must be operated at 8 MHz or more.

**Data Transmission Baud Rates**

| Machine clock | Baud rate (Max) |
|---|---|
| 16 MHz | 1 Mbps |
| 12 MHz | 1 Mbps |
| 8 MHz | 1 Mbps |
| 4 MHz | 500 kbps |
| 2 MHz | 250 kbps |

- Supplies 8 send/receive message buffers.
- Sending and receiving available in standard frame format (ID 11-bit) , and extended frame format (ID 29-bit) .
- Message data can be set to 0 to 8 bytes.
- Possible to configure a multi-level message buffer.
- The CAN controller has two built-in acceptance masks, each of which can be set to a different mask for reception message IDs.
- The two acceptance masks can receive in standard or extended frame format.
- Configure four types of partial masks with full-bit compare, full-bit mask, and acceptance mask register 0/1.

- **CAN Controller Block Diagram**

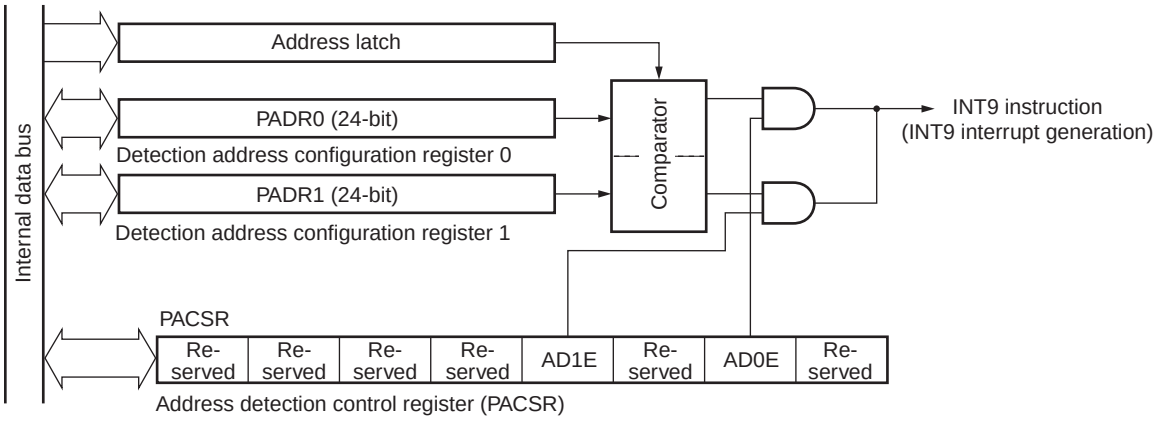


## 13. ROM Correction Function

In the case that the address of the instruction after the one that a program is currently processing matches the address configured in the detection address configuration register, the program forces the next instruction to be processed into an INT9 instruction, and branches to the interrupt process program. Since processing can be conducted using INT9 interrupts, programs can be repaired using batch processing.

- **Overview of the ROM Correction Function**
- The address of the instruction after the one that a program is currently processing is always stored in an address latch via the internal data bus. ROM correction constantly compares the address stored in the address latch with the one configured in the detection address configuration register. If the two compared addresses match, the CPU forcibly changes this instruction into an INT9 instruction, and executes an interrupt processing program.
- There are two detection address configuration registers : PADR0 and PADR1. Each register provides an interrupt enable bit. This allows you to individually configure each register to enable/prohibit the generation of interrupts when the address stored in the address latch matches the one configured in the detection address configuration register.

- **ROM Correction Block Diagram**



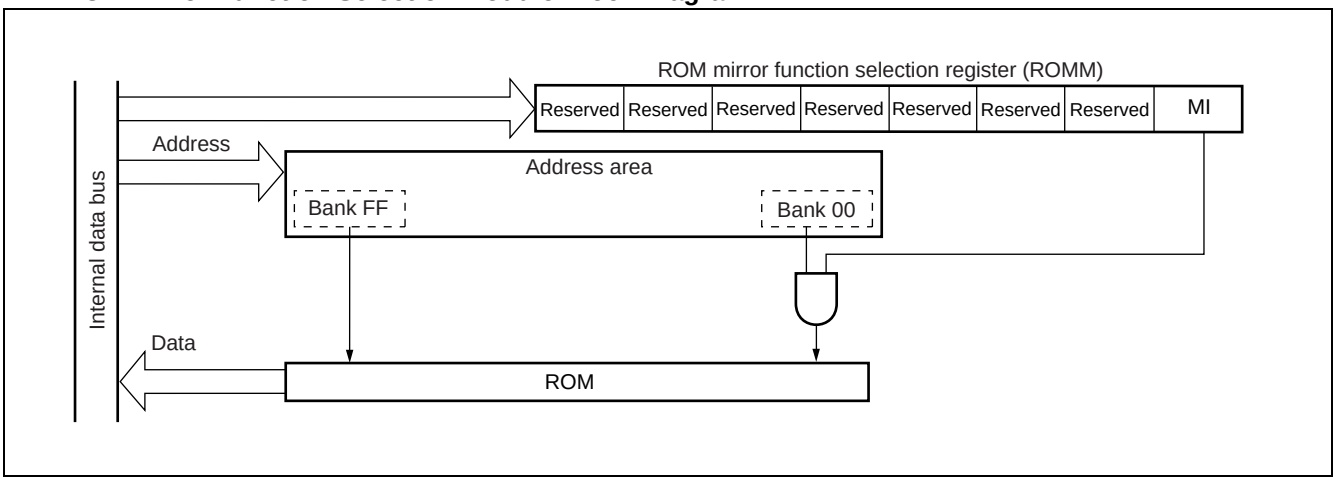

Reserved : Make sure this is always set to “01”

- Address latch
  Stores value of address output to internal data bus.
- Address detection control register (PACSR)
  Set this register to enable/prohibit interrupt output when an address match is detected.
- Detection address configuration register (PADR0, PADR1)
  Configure an address with which to compare the address latch value.

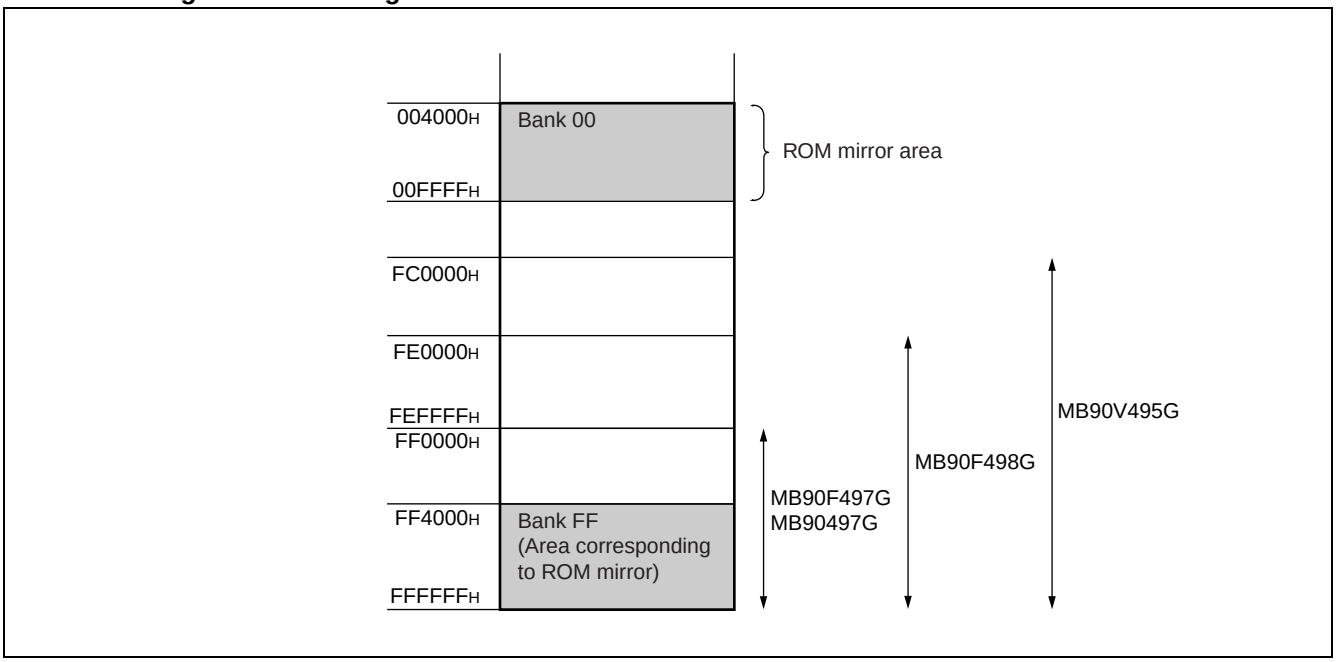
## 14. ROM Mirror Function Selection Module

The ROM mirror function selection module configures ROM-internal data arrayed inside bank FF to be readable by accessing bank 00.

- **ROM Mirror Function Selection Module Block Diagram**




- **Accessing Bank FF through ROM Mirror Function**



## 15. 512-K/1-M bit Flash Memory

- **Overview**

There are three methods available for writing/deleting data to/from flash memory :

1. Parallel writer
2. Serial dedicated writer
3. Program runtime write/delete

- **Overview of 512-K/1-M bit flash memory**

512-Kbit flash memory is arrayed in bank $FF_H$ on the CPU memory map, 1-Mbit flash memory is arrayed in bank $FE_H$ to $FF_H$ on the CPU memory map. The flash memory interface circuit provides read and program access from the CPU.

Since instructions from the CPU are carried out via the flash memory interface circuit, flash memory can be overwritten at the implementation level. This allows you to efficiently improve programs and data.

- **Features of 512-K/1-M bit Flash Memory**
  - 512-Kbit flash memory : 64 KWords × 8-bit/32 KWords × 16-bit (16-Kbyte + 8-Kbyte + 8-Kbyte + 32-Kbyte) sector architecture
  - 1-Mbit flash memory : 128 KWords × 8-bit/64 KWords × 16-bit (16-Kbyte + 8-Kbyte + 8-Kbyte + 32-Kbyte + 64-Kbyte) sector architecture
  - Auto program algorithm (Embedded Algorithm : same as MBM29LV200)
  - On-chip delete suspend/delete resume functions
  - Data polling, write/delete completion detection through toggle bit
  - Write/delete completion detection from CPU overwrite
  - Sector-specific deletion available (sectors can be combined as desired)
  - Write/delete iterations (minimum) : 10,000

Notes : There is no function to read the manufacture or device code.
These codes also cannot be accessed through commands.

- **Flash memory write/delete**
  - It is not possible to simultaneously write to and read from flash memory.
  - When writing to or deleting from flash memory, first copy the program residing in flash memory into RAM, then execute the program copied into RAM. This will allow you to write to flash memory.

- **List of Flash Memory Registers and Reset Values**

Flash memory control status register (FMCS)

| bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | X | 0 | 0 | 0 | 0 |

× : Undefined

- **Sector Architecture of 512-K/1-M bit Flash memory**
- Sector architecture

  512-Kbit flash memory : When accessing from the CPU, SA0 to SA3 are arrayed in the Bank FF register.

  1-Mbit flash memory : When accessing from the CPU, SA0 is arrayed in the Bank FE register, SA1 to SA4 are arrayed in the Bank FF register.

**Sector Architecture of 512-K/1-M bit Flash Memory**

| 512-Kbit Flash Memory | CPU Addresses | Writer Address* |
|---|---|---|
| SA0 (32 Kbytes) | FF0000H<br>FF7FFFH | 70000H<br>77FFFH |
| SA1 (8 Kbytes) | FF8000H<br>FF9FFFH | 78000H<br>79FFFH |
| SA2 (8 Kbytes) | FFA000H<br>FFBFFFH | 7A000H<br>7BFFFH |
| SA3 (16 Kbytes) | FFC000H<br>FFFFFFH | 7C000H<br>7FFFFH |

| 1-Mbit Flash Memory | CPU Addresses | Writer Address* |
|---|---|---|
| SA0 (64 Kbytes) | FE0000H<br>FEFFFFH | 60000H<br>6FFFFH |
| SA1 (32 Kbytes) | FF0000H<br>FF7FFFH | 70000H<br>77FFFH |
| SA2 (8 Kbytes) | FF8000H<br>FF9FFFH | 78000H<br>79FFFH |
| SA3 (8 Kbytes) | FFA000H<br>FFBFFFH | 7A000H<br>7BFFFH |
| SA4 (16 Kbytes) | FFC000H<br>FFFFFFH | 7C000H<br>7FFFFH |

* : If a parallel write is writing data to Flash memory, the write address corresponds to the CPU address. If a general-purpose writer is used to write/delete, this address is written to/over.

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

($V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage | $V_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | |
| | $AV_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | $V_{CC}$ = $AV_{CC}$ *1 |
| | AVR | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | $AV_{CC}$ ≥ AVR *1 |
| Input voltage | $V_I$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | *2 |
| Output voltage | $V_O$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | *2 |
| Maximum clamp current | $I_{CLAMP}$ | – 2.0 | + 2.0 | mA | *6 |
| Total maximum clamp current | $\Sigma\lvert I_{CLAMP} \rvert$ | — | 20 | mA | *6 |
| “L” level maximum output current | $I_{OL}$ | — | 15 | mA | *3 |
| “L” level average output current | $I_{OLAV}$ | — | 4 | mA | *4 |
| “L” level maximum total output current | $\Sigma I_{OL}$ | — | 100 | mA | |
| “L” level average total output current | $\Sigma I_{OLAV}$ | — | 50 | mA | *5 |
| “H” level maximum output current | $I_{OH}$ | — | –15 | mA | *3 |
| “H” level average output current | $I_{OHAV}$ | — | –4 | mA | *4 |
| “H” level maximum total output current | $\Sigma I_{OH}$ | — | –100 | mA | |
| “H” level average total output current | $\Sigma I_{OHAV}$ | — | –50 | mA | *5 |
| Power consumption | $P_D$ | — | 315 | mW | |
| Operating temperature | $T_A$ | –40 | +105 | °C | |
| | | –40 | +125 | °C | *7 |
| Storage temperature | $T_{stg}$ | –55 | +150 | °C | |

*1 : $AV_{CC}$ and AVR shall never exceed $V_{CC}$. Also, AVR shall never exceed $AV_{CC}$.

*2 : $V_I$ and $V_O$ shall never exceed $V_{CC}$ + 0.3 V. However, if the maximum current to/from an input is limited by some means with external components, the $I_{CLAMP}$ rating supersedes the $V_I$ rating.

*3 : The rating for the maximum output current is the peak value of one of the corresponding pins.

*4 : The standard for computing average output current is the average current output from one of the corresponding pins over a period of 100 ms (the average value is taken by multiplying operating current by operational rate) .

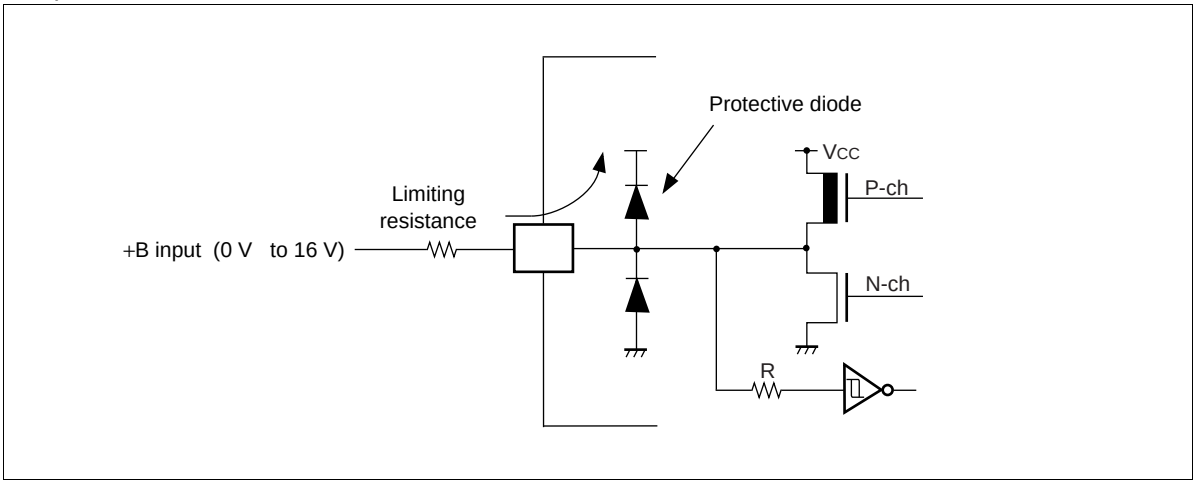
*5 : The standard for computing average total output current is the average current output from all of the corresponding pins over a period of 100 ms (the average value is taken by multiplying operating current by operational rate) .

*6 : • Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P44, P50 to P57, P60 to P63
• Use within recommended operating conditions.
• Use at DC voltage (current)
• The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
• The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
• Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the $V_{CC}$ pin, and this may affect other devices.

*(Continued)*

*(Continued)*

- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits:




*7 : If used exceeding $T_A$ = +105 °C, be sure to contact us for reliability limitations.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended Operating Conditions

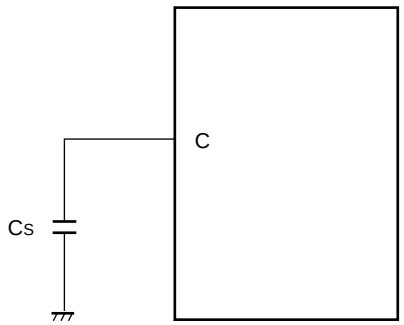
($V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Power supply voltage | $V_{CC}$, $AV_{CC}$ | 4.5 | 5.0 | 5.5 | V | During normal operation, $T_A$ = –40 °C to +105 °C |
| | | 4.75 | 5.0 | 5.25 | V | During normal operation, +105 °C < $T_A$ ≤ +125 °C |
| | | 3.0 | — | 5.5 | V | Maintaining stop operation state |
| Smoothing capacitor | $C_S$ | 0.022 | 0.1 | 1.0 | µF | *1 |
| Operating temperature | $T_A$ | –40 | — | +105 | °C | |
| | | –40 | — | +125 | °C | *2 |

*1 : Use a ceramic capacitor, or one with approximately the same frequency characteristics. The bypass capacitor of the $V_{CC}$ pin should have a greater capacity than $C_S$.
See the figure below for details about connecting a smooth capacitor to the $C_S$.

*2 : If used exceeding $T_A$ = +105 °C, be sure to contact us for reliability limitations.

• C Pin Connection Diagram




WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## 3. DC Characteristics

($V_{CC}$ = 5.0 V ± 5%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +125 °C)
($V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin Name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "H" level input voltage | $V_{IHS}$ | CMOS hysteresis input pin | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | |
| | $V_{IHM}$ | MD input pin | — | $V_{CC}$ – 0.3 | — | $V_{CC}$ + 0.3 | V | |
| "L" level input voltage | $V_{ILS}$ | CMOS hysteresis input pin | — | $V_{SS}$ – 0.3 | — | 0.2 $V_{CC}$ | V | |
| | $V_{ILM}$ | MD input pin | — | $V_{SS}$ – 0.3 | — | $V_{SS}$ + 0.3 | V | |
| "H" level output voltage | $V_{OH}$ | All output pins | $V_{CC}$ = 4.5 V, $I_{OH}$ = –4.0 mA | $V_{CC}$ – 0.5 | — | — | V | $T_A$ = –40 °C to +105 °C |
| | | | $V_{CC}$ = 4.75 V | $V_{CC}$ – 0.5 | — | — | V | +105 °C < $T_A$ ≤ +125 °C |
| "L" level output voltage | $V_{OL}$ | All output pins | $V_{CC}$ = 4.5 V, $I_{OL}$ = 4.0 mA | — | — | 0.4 | V | $T_A$ = –40 °C to +105 °C |
| | | | $V_{CC}$ = 4.75 V | — | — | 0.4 | V | +105 °C < $T_A$ ≤ +125 °C |
| Input leakage current | $I_{IL}$ | All output pins | $V_{CC}$ = 5.5 V, $V_{SS}$ < $V_I$ < $V_{CC}$ | –5 | — | + 5 | µA | $T_A$ = –40 °C to +105 °C |
| | | | $V_{CC}$ = 5.25 V, $V_{SS}$ < $V_I$ < $V_{CC}$ | –5 | — | + 5 | µA | +105 °C < $T_A$ ≤ +125 °C |
| Power supply current* | $I_{CC}$ | $V_{CC}$ | $V_{CC}$ = 5.0 V Internal 16-MHz operation, Normal mode | — | 30 | 40 | mA | MB90497G MB90F497G MB90F498G |
| | | | $V_{CC}$ = 5.0 V Internal 16-MHz operation, Flash memory write mode | — | 45 | 50 | mA | MB90F497G MB90F498G |
| | | | $V_{CC}$ = 5.0 V Internal 16-MHz operation, Flash memory delete mode | — | 45 | 50 | mA | MB90F497G MB90F498G |
| | $I_{CCS}$ | | $V_{CC}$ = 5.0 V Internal 16-MHz operation, Sleep mode | — | 11 | 18 | mA | MB90497G MB90F497G MB90F498G |

*(Continued)*

*(Continued)*

($V_{CC}$ = 5.0 V ± 5%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +125 °C)
($V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin Name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current* | $I_{CTS}$ | $V_{CC}$ | $V_{CC}$ = 5.0 V<br>Internal 2-MHz operation,<br>Timer mode | — | 0.6 | 1.2 | mA | MB90497G<br>MB90F497G<br>MB90F498G |
| | $I_{CCL}$ | | $V_{CC}$ = 5.0 V<br>Internal 8-kHz operation,<br>Subclock operation mode<br>$T_A$ = + 25 °C | — | 30 | 50 | µA | MB90497G |
| | | | | — | 300 | 500 | µA | MB90F497G<br>MB90F498G |
| | $I_{CCLS}$ | | $V_{CC}$ = 5.0 V<br>Internal 8-kHz operation,<br>Subclock sleep mode<br>$T_A$ = + 25 °C | — | 10 | 30 | µA | MB90497G<br>MB90F497G<br>MB90F498G |
| | $I_{CCT}$ | | $V_{CC}$ = 5.0 V<br>Internal 8-kHz operation,<br>Clock mode<br>$T_A$ = + 25 °C | — | 8 | 25 | µA | MB90497G<br>MB90F497G<br>MB90F498G |
| Power supply current* | $I_{CCH}$ | $V_{CC}$ | $V_{CC}$ = 5.0 V<br>Stop mode, $T_A$ = + 25 °C | — | 5 | 20 | µA | MB90497G<br>MB90F497G<br>MB90F498G |
| Input Capacity | $C_{IN}$ | Other than $AV_{CC}$, $AV_{SS}$, AVR, C, $V_{CC}$, or $V_{SS}$ | — | — | 5 | 15 | pF | |
| Pull up Resistor | $R_{UP}$ | $\overline{RST}$ | — | 25 | 50 | 100 | kΩ | |
| Pull down Resistor | $R_{DOWN}$ | MD2 | — | 25 | 50 | 100 | kΩ | |

* : This is when using the external clock as the power supply current test condition.

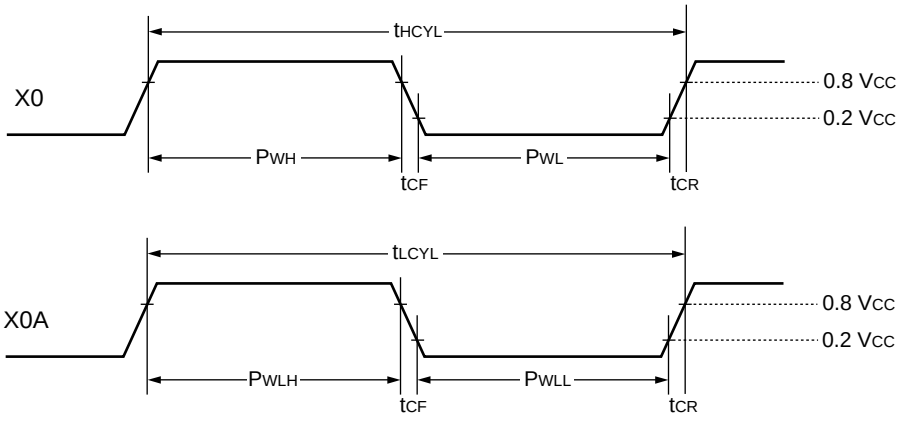
## 4. AC Characteristics

### (1) Clock Timing

($V_{CC}$ = 5.0 V ± 5%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +125 °C)
($V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

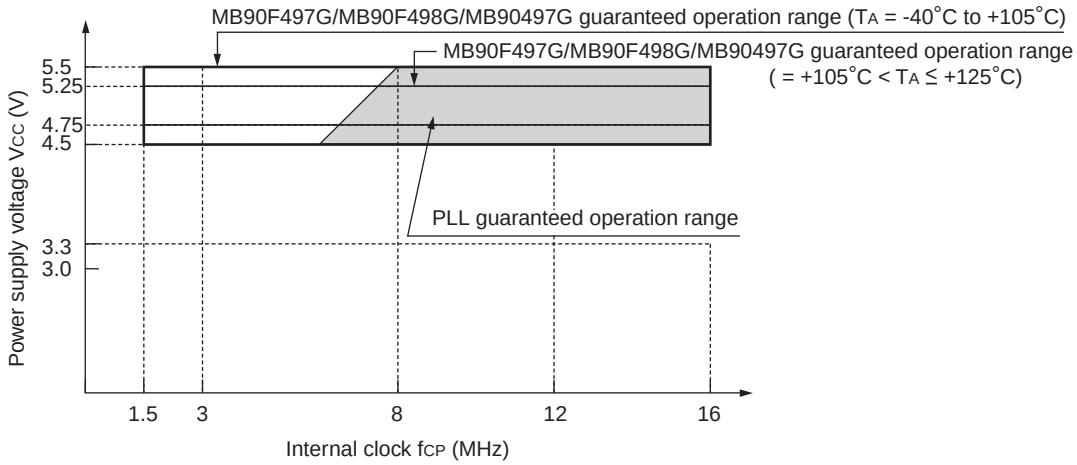
| Parameter | Symbol | Pin Name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Clock frequency | $f_C$ | X0, X1 | 3 | — | 16 | MHz | |
| | $f_{CL}$ | X0A, X1A | — | 32.768 | — | kHz | |
| Clock Cycle Time | $t_{HCYL}$ | X0, X1 | 62.5 | — | 333 | ns | |
| | $t_{LCYL}$ | X0A, X1A | — | 30.5 | — | µs | |
| Input clock pulse width | $P_{WH}$, $P_{WL}$ | X0 | 10 | — | — | ns | Duty ratio should be around 30 % to 70 % |
| | $P_{WLH}$, $P_{WLL}$ | X0A | — | 15.2 | — | µs | |
| Input clock rising/falling time | $t_{CR}$, $t_{CF}$ | X0 | — | — | 5 | ns | When external clock used |
| Internal operation clock frequency | $f_{CP}$ | — | 1.5 | — | 16 | MHz | When oscillation circuit used |
| | $f_{LCP}$ | — | — | 8.192 | — | kHz | When subclock used |
| Internal operation clock cycle time | $t_{CP}$ | — | 62.5 | — | 666 | ns | When using oscillation circuit |
| | $t_{LCP}$ | — | — | 122.1 | — | µs | When subclock used |

- X0/X1 Clock Timing

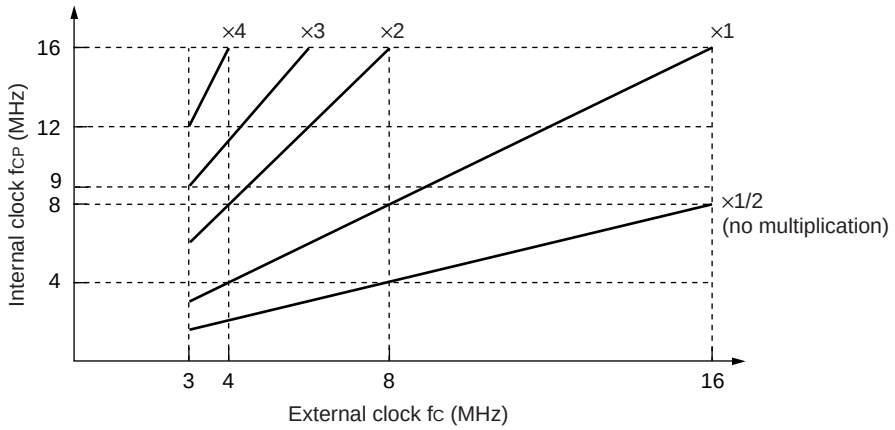


- PLL guaranteed operation range

Relationship between internal operating clock frequency and power supply voltage



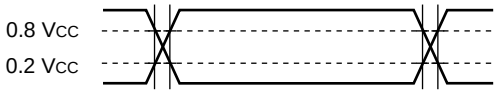

Relationship between external clock frequency and internal operation clock frequency




AC characteristics are specified by the following reference voltage values.

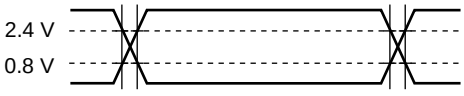
- Input Signal Waveform

Hysteresis Input Pin




- Output Signal Waveform

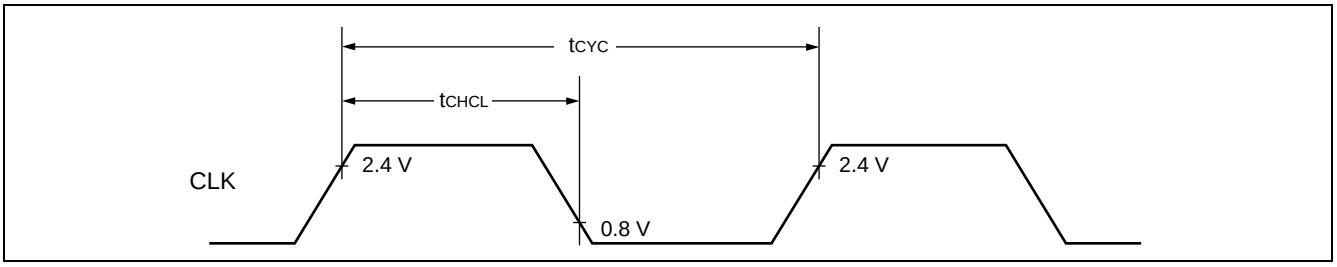
Output Pin



### (2) Clock Output Timing

($V_{CC}$ = 5.0 V ± 5%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +125 °C)
($V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin Name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Cycle time | $t_{CYC}$ | CLK | — | 62.5 | — | ns | |
| CLK ↑ → CLK ↓ | $t_{CHCL}$ | | | 20 | — | ns | |

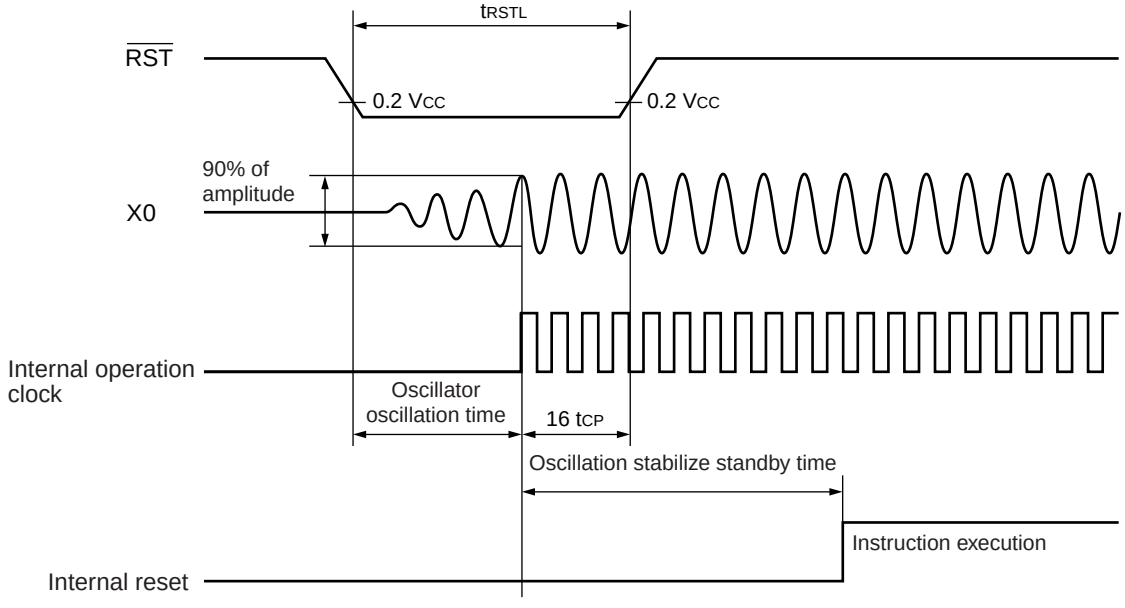



### (3) Reset Input Timing

| Parameter | Symbol | Pin Name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Reset input time | $t_{RSTL}$ | $\overline{RST}$ | — | 16 $t_{CP}$ | — | ns | Normal mode |
| | | | | Oscillator oscillation time* + 16 $t_{CP}$ | — | ms | Stop mode, Watch mode, Subclock mode, Subsleep mode |

* : Oscillator oscillation time is the time to reach 90% amplitude. For a crystal oscillator, this is a few to several dozen ms; for a ceramic oscillator, this is several hundred µs to a few ms, and for an external clock this is 0 ms.

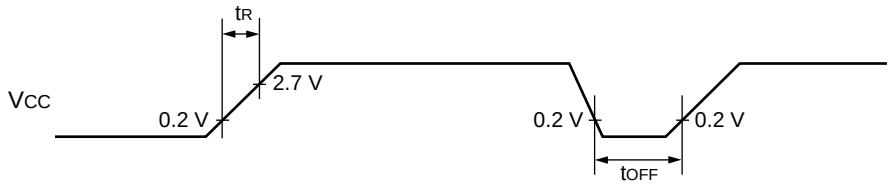
- Stop mode, Watch mode, Subclock mode, Subsleep mode



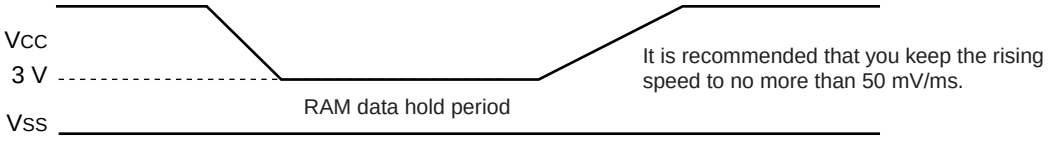
### (4) Power-on Reset

($V_{CC}$ = 5.0 V ± 5%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +125 °C)
($V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin Name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Power supply rising time | $t_R$ | $V_{CC}$ | — | 0.05 | 30 | ms | |
| Power supply cutoff time | $t_{OFF}$ | $V_{CC}$ | | 1 | — | ms | Due to repeated operations |




Sudden changes in the power supply voltage may cause a power-on reset. To change the power supply voltage while the device is in operation, it is recommended that you raise the voltage at a steady rate, in order to suppress fluctuations (see figure below). In this case, perform this operation when the PLL clock is not being used. If, however, the voltage falling speed is no more than 1 V/s, it is permissible to perform this operation while using the PLL clock.

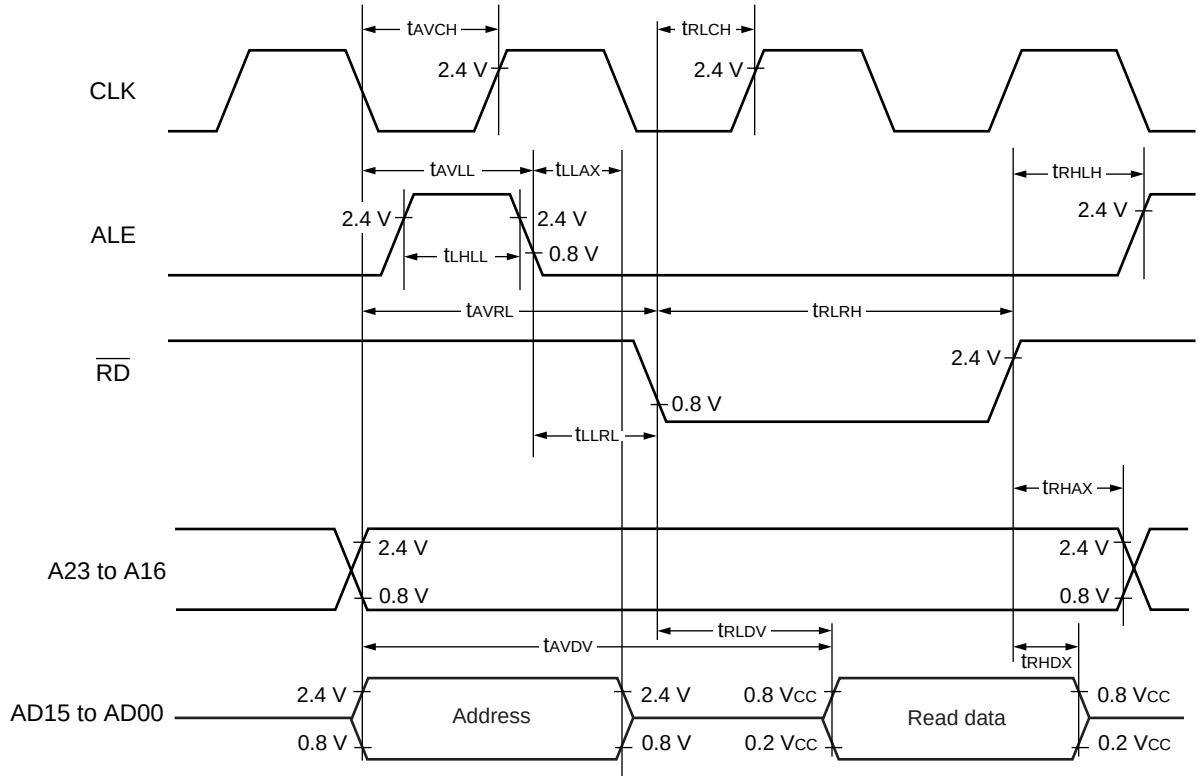


### (5) Bus Read Timing

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin Name | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| ALE pulse width | $t_{LHLL}$ | ALE | $t_{CP}/2 - 20$ | — | ns | |
| Valid address → ALE ↓ time | $t_{AVLL}$ | ALE, A23 to A16, AD15 to AD00 | $t_{CP}/2 - 20$ | — | ns | |
| ALE ↓ → address valid time | $t_{LLAX}$ | ALE, AD15 to AD00 | $t_{CP}/2 - 15$ | — | ns | |
| Valid address → $\overline{RD}$ ↓ time | $t_{AVRL}$ | A23 to A16, AD15 to AD00, $\overline{RD}$ | $t_{CP} - 15$ | — | ns | |
| Valid address → Valid data input | $t_{AVDV}$ | A23 to A16, AD15 to AD00 | — | $5\ t_{CP}/2 - 60$ | ns | |
| $\overline{RD}$ pulse width | $t_{RLRH}$ | $\overline{RD}$ | $3\ t_{CP}/2 - 20$ | — | ns | |
| $\overline{RD}$ ↓ → valid data input | $t_{RLDV}$ | $\overline{RD}$, AD15 to AD00 | — | $3\ t_{CP}/2 - 60$ | ns | |
| $\overline{RD}$ ↑ → data hold time | $t_{RHDX}$ | $\overline{RD}$, AD15 to AD00 | 0 | — | ns | |
| $\overline{RD}$ ↑ → ALE ↑ time | $t_{RHLH}$ | $\overline{RD}$, ALE | $t_{CP}/2 - 15$ | — | ns | |
| $\overline{RD}$ ↑ → address valid time | $t_{RHAX}$ | $\overline{RD}$, A23 to A16 | $t_{CP}/2 - 10$ | — | ns | |
| Valid address → CLK ↑ time | $t_{AVCH}$ | A23 to A16, AD15 to AD00, CLK | $t_{CP}/2 - 20$ | — | ns | |
| $\overline{RD}$ ↓ → CLK ↑ time | $t_{RLCH}$ | $\overline{RD}$, CLK | $t_{CP}/2 - 20$ | — | ns | |
| ALE ↓ → $\overline{RD}$ ↓ time | $t_{LLRL}$ | ALE, $\overline{RD}$ | $t_{CP}/2 - 15$ | — | ns | |

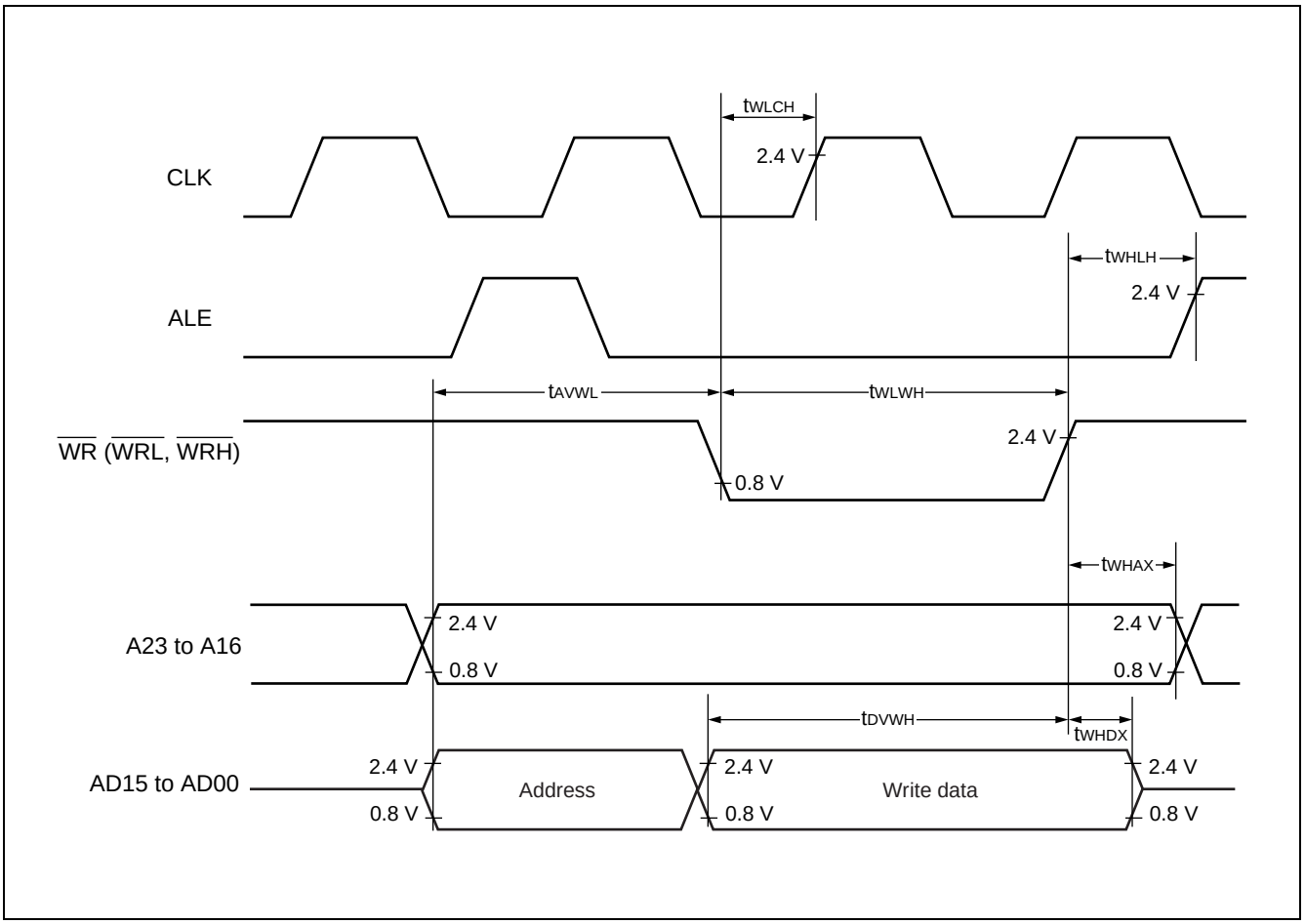
• Bus read timing



### (6) Bus Write Timing

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin Name | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Valid Address → $\overline{WR}$ ↓ time | $t_{AVWL}$ | A23 to A16, AD15 to AD00, $\overline{WR}$ | $t_{CP}$ – 15 | — | ns | |
| $\overline{WR}$ pulse width | $t_{WLWH}$ | $\overline{WR}$ | 3 $t_{CP}$/2 – 20 | — | ns | |
| Valid data output → $\overline{WR}$ ↑ time | $t_{DVWH}$ | AD15 to AD00, $\overline{WR}$ | 3 $t_{CP}$/2 – 20 | — | ns | |
| $\overline{WR}$ ↑ → data hold time | $t_{WHDX}$ | AD15 to AD00, $\overline{WR}$ | 20 | — | ns | |
| $\overline{WR}$ ↑ → address valid time | $t_{WHAX}$ | A23 to A16, $\overline{WR}$ | $t_{CP}$/2 – 10 | — | ns | |
| $\overline{WR}$ ↑ → ALE ↑ time | $t_{WHLH}$ | $\overline{WR}$, ALE | $t_{CP}$/2 – 15 | — | ns | |
| $\overline{WR}$ ↑ → CLK ↑ time | $t_{WLCH}$ | $\overline{WR}$, CLK | $t_{CP}$/2 – 20 | — | ns | |



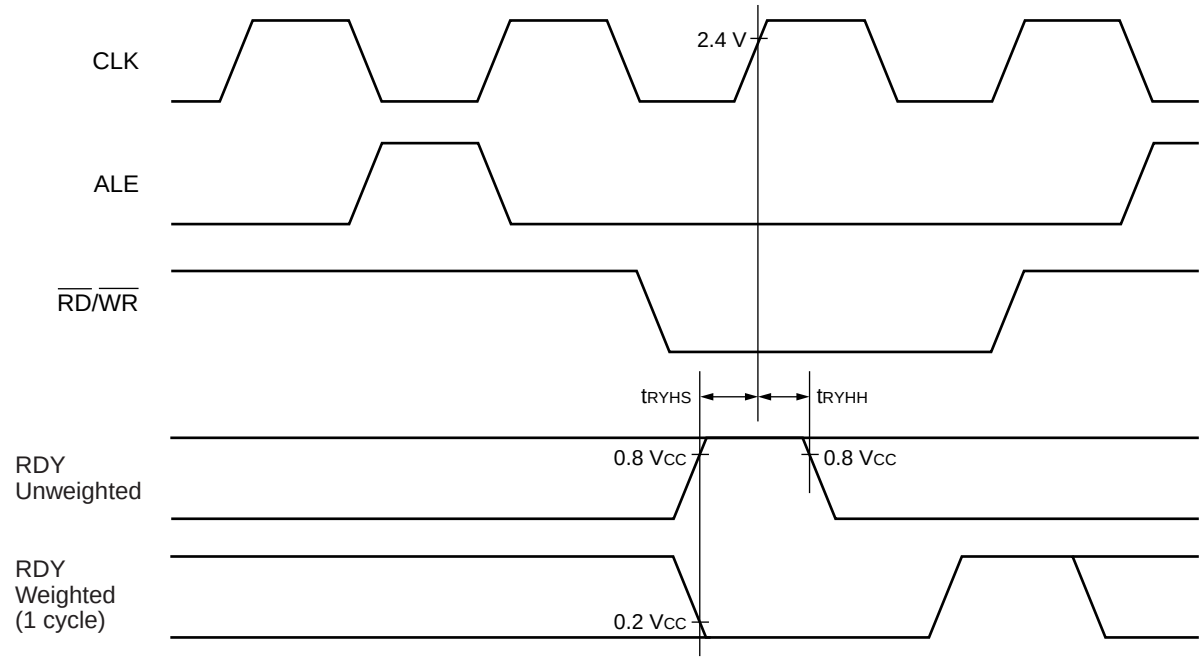
### (7) Ready Input Timing

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin Name | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| RDY setup time | $t_{RYHS}$ | RDY | 45 | — | ns | |
| RDY hold time | $t_{RYHH}$ | RDY | 0 | — | ns | |

Note : Use the automatic ready function if the setup time for the falling edge of the RDY signal is not sufficient.

• Ready Input timing



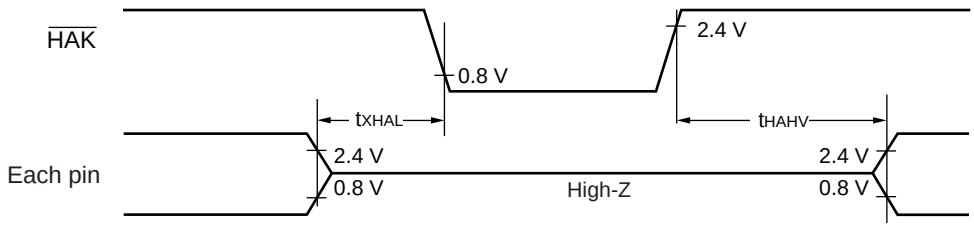

### (8) Hold Timing

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin Name | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Pin in floating status → $\overline{HAK}$ ↓ time | $t_{XHAL}$ | $\overline{HAK}$ | 30 | $t_{CP}$ | ns | |
| $\overline{HAK}$ ↑ → pin valid time | $t_{HAHV}$ | $\overline{HAK}$ | $t_{CP}$ | 2 $t_{CP}$ | ns | |

Note : It will take at least 1 cycle from the time the HRQ pin is loaded until the HAK changes.

• Hold Timing



### (9) UART Timing

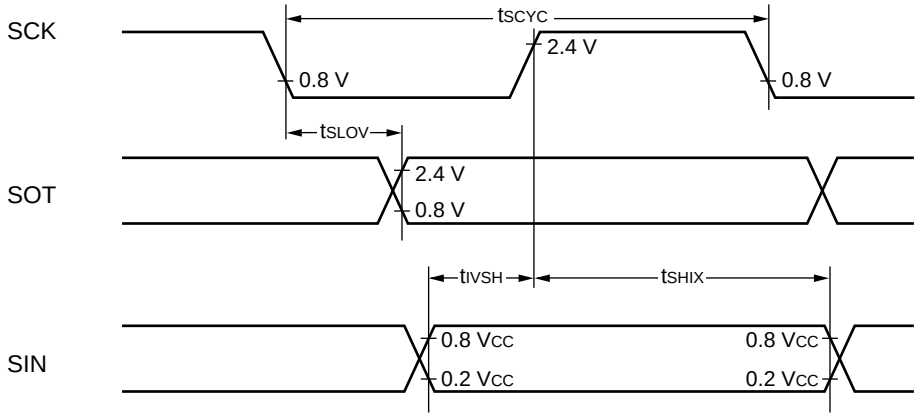
($V_{CC}$ = 5.0 V±5%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +125 °C)
($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin Name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock cycle time | $t_{SCYC}$ | SCK1 | Internal shift clock mode output pin : $C_L$ = 80 pF + 1 TTL | 8 $t_{CP}$* | — | ns | |
| SCK ↓ → SOT delay time | $t_{SLOV}$ | SCK1, SOT1 | | –80 | + 80 | ns | |
| Valid SIN → SCK ↑ | $t_{IVSH}$ | SCK1, SIN1 | | 100 | — | ns | |
| SCK ↑ → valid SIN hold time | $t_{SHIX}$ | SCK1, SIN1 | | 60 | — | ns | |
| Serial clock “H” pulse width | $t_{SHSL}$ | SCK1 | External shift clock mode output pin : $C_L$ = 80 pF + 1 TTL | 4 $t_{CP}$ | — | ns | |
| Serial clock “L” pulse width | $t_{SLSH}$ | SCK1 | | 4 $t_{CP}$ | — | ns | |
| SCK ↓ → SOT delay time | $t_{SLOV}$ | SCK1, SOT1 | | — | 150 | ns | |
| Valid SIN → SCK ↑ | $t_{IVSH}$ | SCK1, SIN1 | | 60 | — | ns | |
| SCK ↑ → valid SIN hold time | $t_{SHIX}$ | SCK1, SIN1 | | 60 | — | ns | |

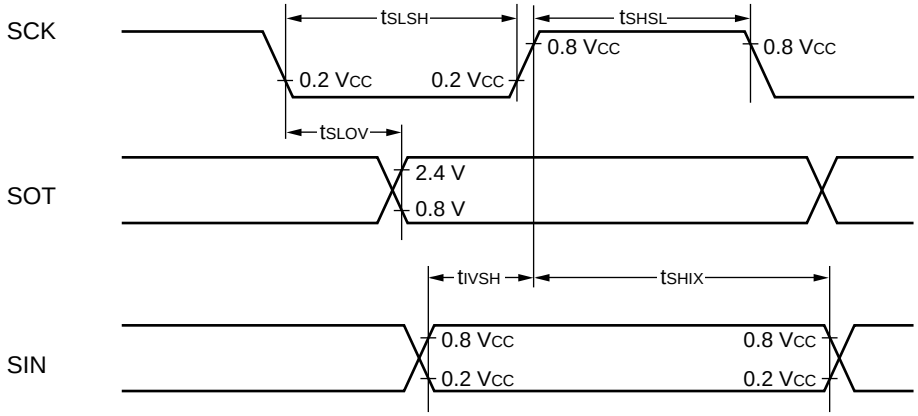
* : See “ (1) Clock Timing” for details about $t_{CP}$ (internal operating clock cycle time).

Notes : • AC characteristics are for CLK synchronous mode.
• $C_L$ is the load capacitor value connected to pins while testing.

- Internal shift clock mode




- External shift clock mode

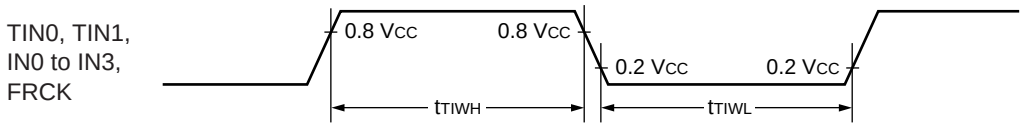


### (10) Timer Input Timing

($V_{CC}$ = 5.0 V±5%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +125 °C)
($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin Name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TIWH}$ | TIN0, TIN1, FRCK | — | 4 $t_{CP}$ | — | ns | |
| | $t_{TIWL}$ | IN0 to IN3, FRCK | | | | | |

- Timer Input Timing

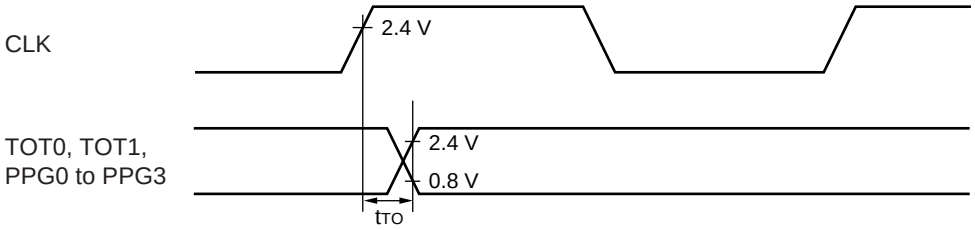



### (11) Timer Output Timing

($V_{CC}$ = 5.0 V±5%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +125 °C)
($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin Name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| CLK ↑ → $T_{OUT}$ change time | $t_{TO}$ | TOT0, TOT1, PPG0 to PPG3 | — | 30 | — | ns | |

- Timer Output Timing

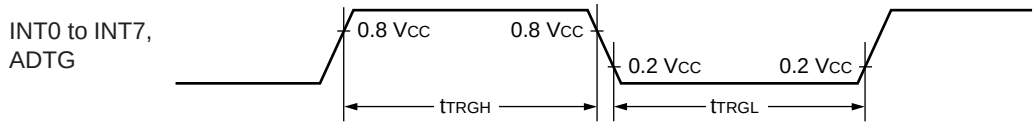



### (12) Trigger Input Timing

($V_{CC}$ = 5.0 V±5%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +125 °C)
($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +105 °C)

| Parameter | Symbol | Pin Name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TRGH}$ | INT0 to INT7, ADTG | — | 5 $t_{CP}$ | — | ns | Normal mode |
| | $t_{TRGL}$ | | | 1 | — | µs | Stop mode |

- Trigger Input Timing



## 5. A/D Converter

($V_{CC}$ = $AV_{CC}$ = 5.0 V±5%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, 3.0 V ≤ AVR – $AV_{SS}$, $T_A$ = –40 °C to +125 °C)
($V_{CC}$ = $AV_{CC}$ = 5.0 V±10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, 3.0 V ≤ AVR – $AV_{SS}$, $T_A$ = –40 °C to +105 °C)

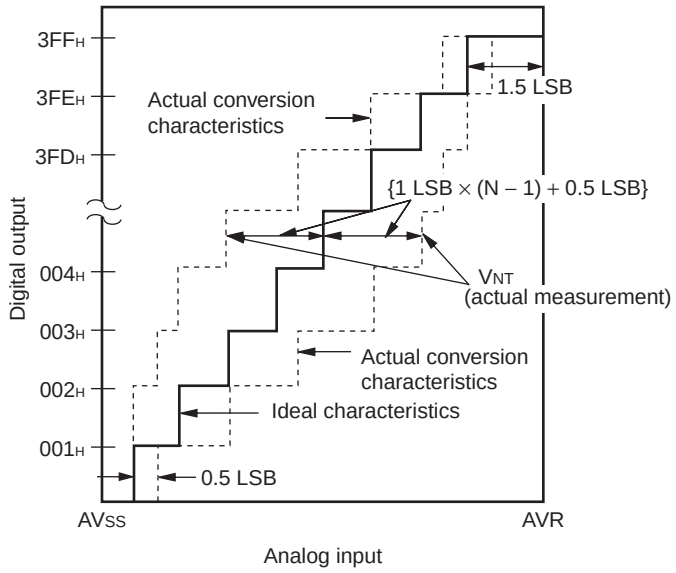
| Parameter | Symbol | Pin Name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | — | — | — | | 10 | bit | |
| Total error | — | — | — | — | ±5.0 | LSB | |
| Nonlinearity error | — | — | — | — | ±2.5 | LSB | |
| Differential linearity error | — | — | — | — | ±1.9 | LSB | |
| Zero transition voltage | $V_{OT}$ | AN0 to AN7 | $AV_{SS}$ – 3.5 LSB | $AV_{SS}$ + 0.5 LSB | $AV_{SS}$ + 4.5 LSB | V | 1 LSB = (AVR - $AV_{SS}$) / 1024 |
| Full-scale transition voltage | $V_{FST}$ | AN0 to AN7 | AVR – 6.5 LSB | AVR – 1.5 LSB | AVR + 1.5 LSB | V | |
| Conversion time | — | — | 66 $t_{CP}$ | — | — | ns | Machine clock of 16 MHz |
| Sampling period | — | — | 32 $t_{CP}$ | — | — | ns | |
| Analog port input current | $I_{AIN}$ | AN0 to AN7 | — | — | 10 | µA | |
| Analog input voltage | $V_{AIN}$ | AN0 to AN7 | $AV_{SS}$ | — | AVR | V | |
| Reference voltage | — | AVR | $AV_{SS}$ + 3.0 | — | $AV_{CC}$ | V | |
| Power supply current | $I_A$ | $AV_{CC}$ | — | 2 | 7 | mA | |
| | $I_{AH}$ | $AV_{CC}$ | — | — | 5 | µA | * |
| Reference voltage supply current | $I_R$ | AVR | — | 0.9 | 1.3 | mA | |
| | $I_{RH}$ | AVR | — | — | 5 | µA | * |
| Inter-channel variation | — | AN0 to AN7 | — | — | 4 | LSB | |

* : Current ($V_{CC}$ = $AV_{CC}$ = AVR = 5.0 V) when A/D converter is not operating and CPU is halted.

## 6. A/D Converter Glossary

| | | |
|---|---|---|
| Resolution | : | Analog changes that are identifiable with the A/D converter |
| Linearity error | : | The deviation of the straight line connecting the zero transition point ( “00 0000 0000” ←→ “00 0000 0001” ) with the full-scale transition point ( “11 1111 1110” ←→ “11 1111 1111” ) from actual conversion characteristics. |
| Differential linearity error | : | The deviation of input voltage needed to change the output code by 1 LSB from the ideal value. |
| Total error | : | The difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error, linearity error, and differential linearity error. |

Total error




$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$1\ \text{LSB} = (\text{ideal value})\ \frac{AVR - AV_{SS}}{1024}\ \text{[V]}$$

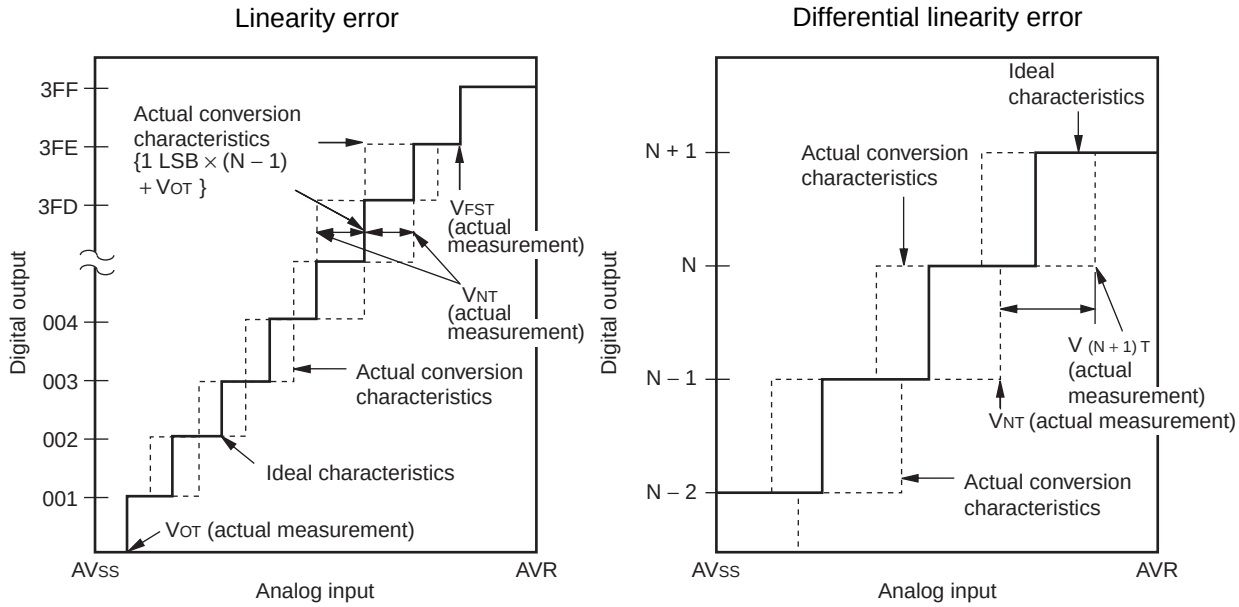
$V_{OT}$ (ideal value) $= AV_{SS} + 0.5$ LSB [V]

$V_{FST}$ (ideal value) $= AVR - 1.5$ LSB [V]

$V_{NT}$ : The voltage to transition digital output from (N – 1) to N.

*(Continued)*

*(Continued)*




$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB [LSB]}$$

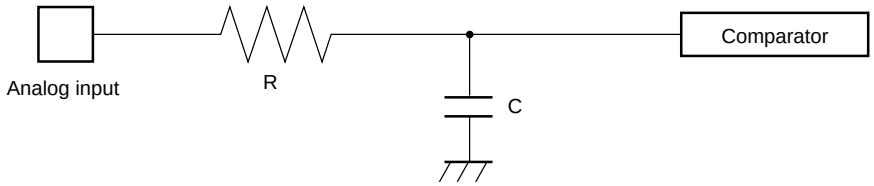
$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

$V_{OT}$ : Voltage for transition from digital output $000_H$ to $001_H$.
$V_{FST}$ : Voltage for transition from digital output $3FE_H$ to $3FF_H$.

## 7. Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions :
External circuit output impedance values of about 5 kΩ or lower are recommended.
If external capacitors are used, a capacitance of several thousand times the internal capacitor value is recommended in order to minimize the effect of voltage distribution between the external and internal capacitor.
If the output impedance of the external circuit is too high, the sampling time for analog voltages may not be sufficient (sampling period = 2.00 µs @ machine clock of 16 MHz) .

- Model Analog Input Circuit




MB90F497G, MB90F498G, MB90V495G R≒3.2 kΩ, C≒30 pF
MB90497G R≒2.6 kΩ, C≒28 pF

Note : The figures given here are the suggested values.

- **About Error**
  The smaller the absolute value of | AVR - $AV_{SS}$ |, the greater the relative error.

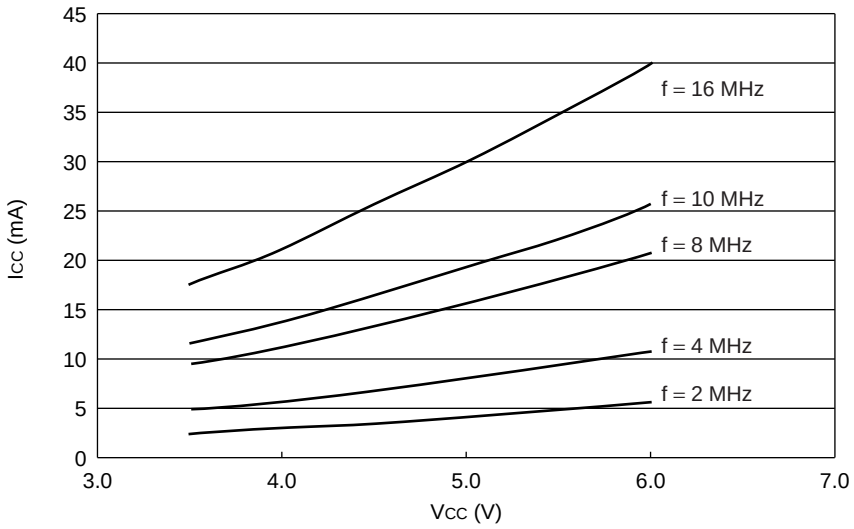
## 8. Flash Memory Program/Erase Characteristics

| Parameter | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Sector erase time | $T_A$ = + 25 °C<br>$V_{CC}$ = 5.0 V | — | 1 | 15 | s | Excludes $00_H$ programming prior erasure |
| Chip erase time | | — | 5 | — | s | Excludes $00_H$ programming prior erasure |
| Word (16-bit width) programming time | | — | 16 | 3,600 | µs | Excludes system-level overhead |
| Erase/Program cycle | — | 10,000 | — | — | cycle | |

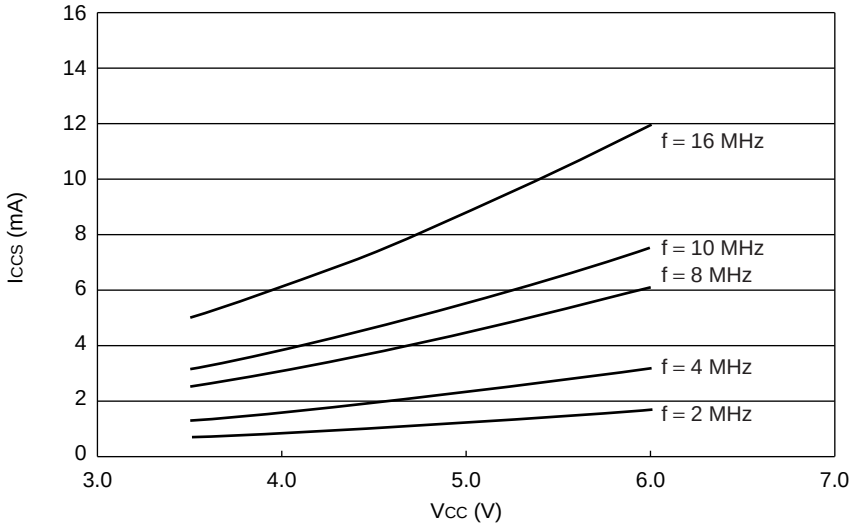
## ■ EXAMPLE CHARACTERISTICS

• MB90F497G/F498G

$I_{CC}$ – $V_{CC}$
$T_A$ = + 25 °C, external clock operation
f = internal operation frequency




$I_{CCS}$ – $V_{CC}$
$T_A$ = + 25 °C, external clock operation
f = internal operation frequency




*(Continued)*

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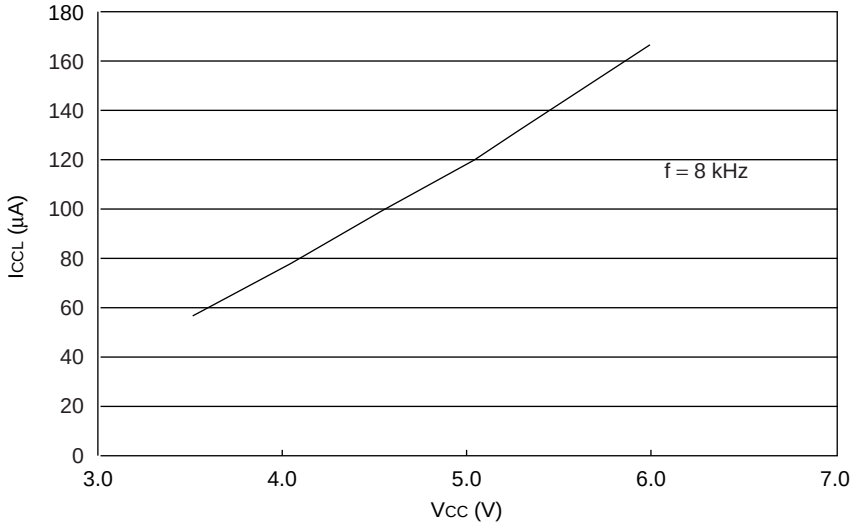
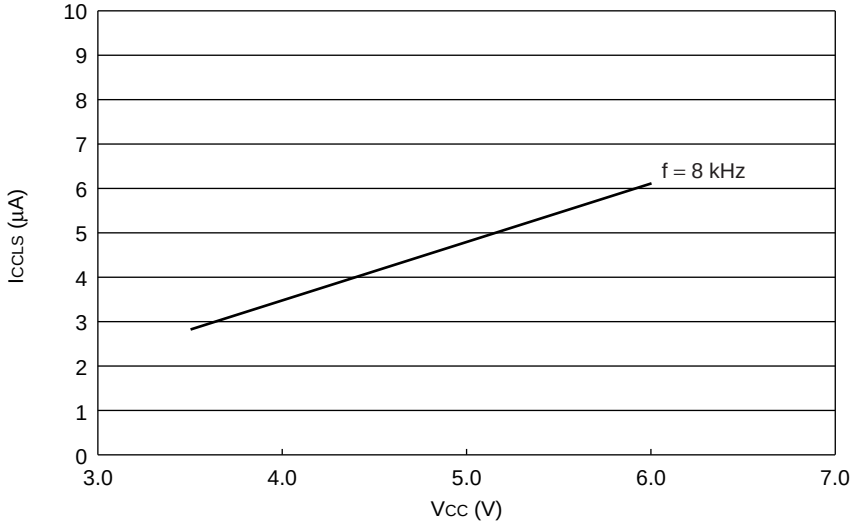
$I_{CCL}$ – $V_{CC}$
$T_A$ = + 25 °C, external clock operation
f = internal operation frequency




$I_{CCLS}$ – $V_{CC}$
$T_A$ = + 25 °C, external clock operation
f = internal operation frequency

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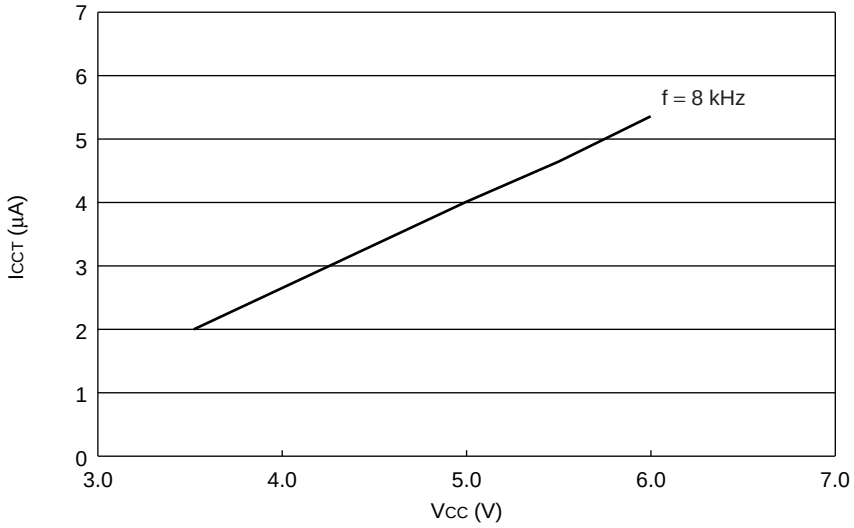
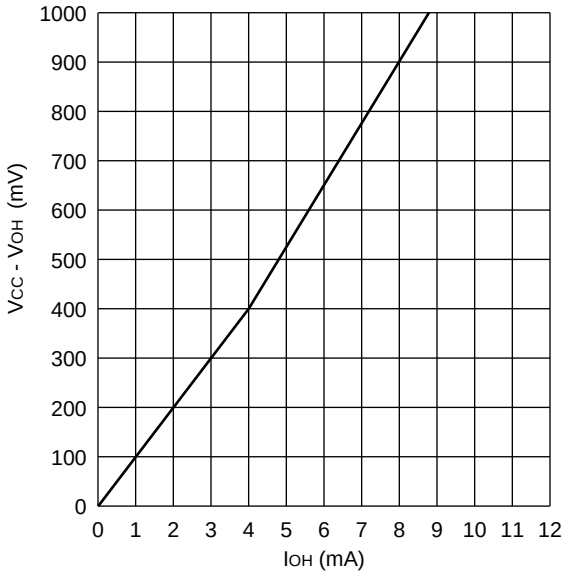
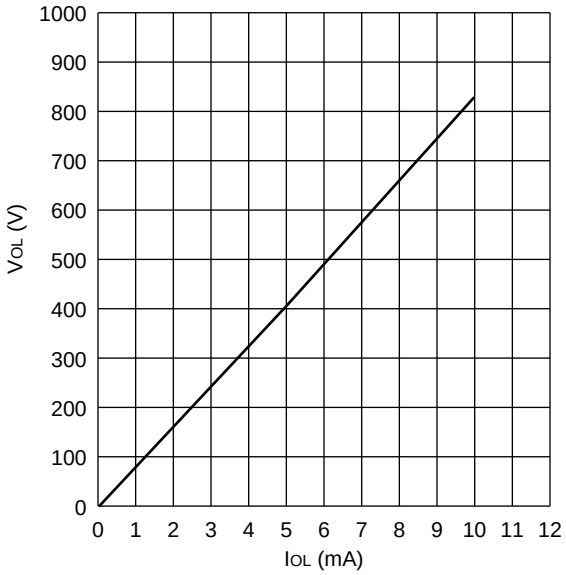
$I_{CCT}$ – $V_{CC}$
$T_A$ = + 25 °C, external clock operation
f = internal operation frequency




($V_{CC}$ – $V_{OH}$) – $I_{OH}$
$T_A$ = + 25 °C, $V_{CC}$ = 4.5 V

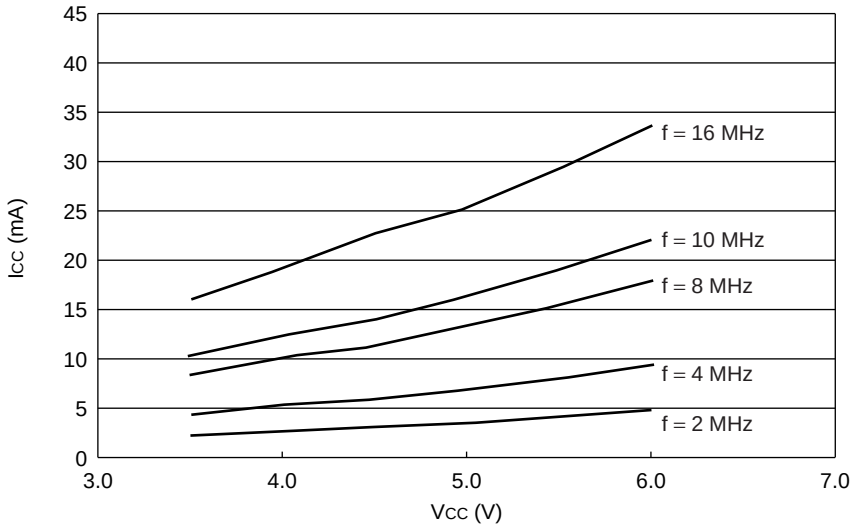



$V_{OL}$ – $I_{OL}$
$T_A$ = + 25 °C, $V_{CC}$ = 4.5 V

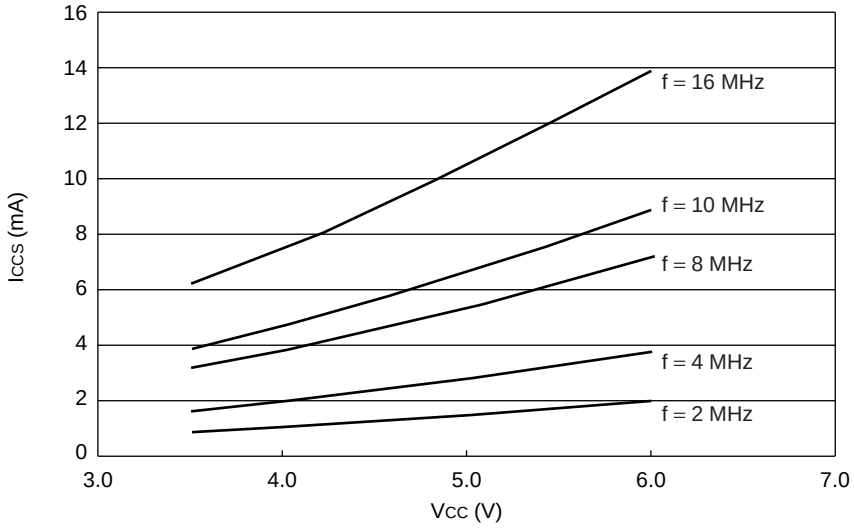


• MB90497G

$I_{CC} - V_{CC}$
$T_A = +25$ °C, external clock operation
f = internal operation frequency




$I_{CCS} - V_{CC}$
$T_A = +25$ °C, external clock operation
f = internal operation frequency

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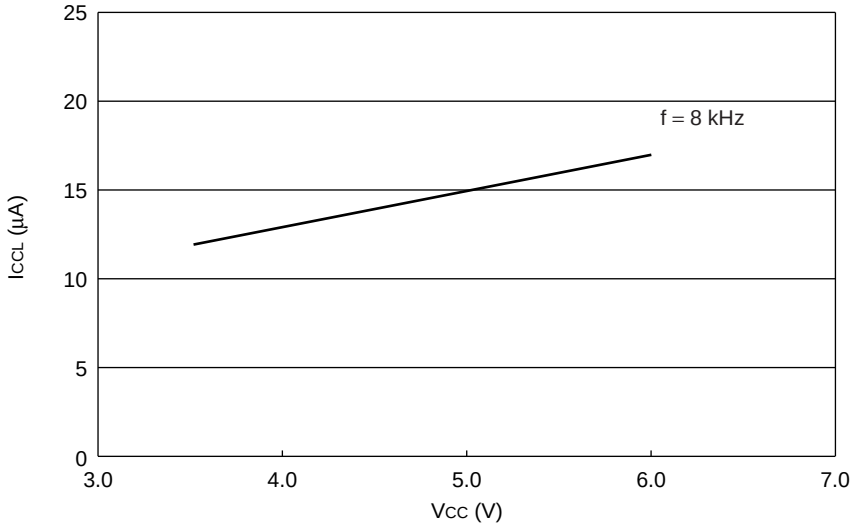
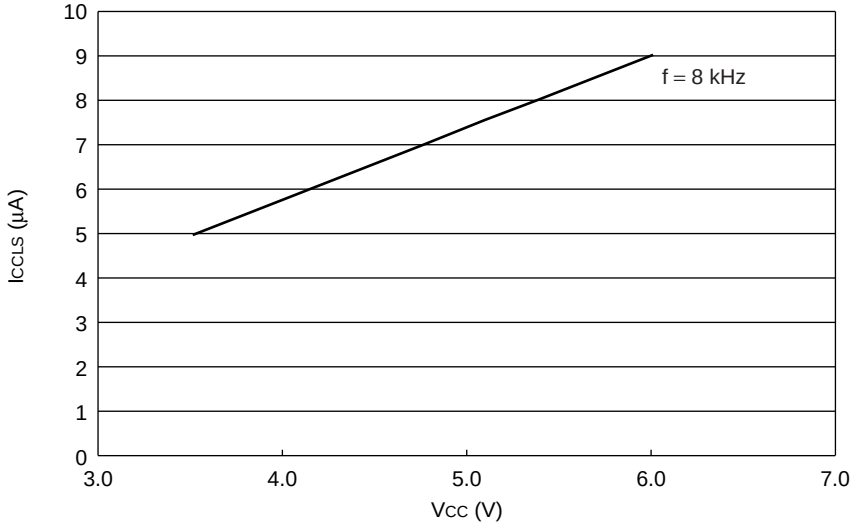
$I_{CCL}$ – $V_{CC}$
$T_A$ = + 25 °C, external clock operation
f = internal operation frequency




$I_{CCLS}$ – $V_{CC}$
$T_A$ = + 25 °C, external clock operation
f = internal operation frequency

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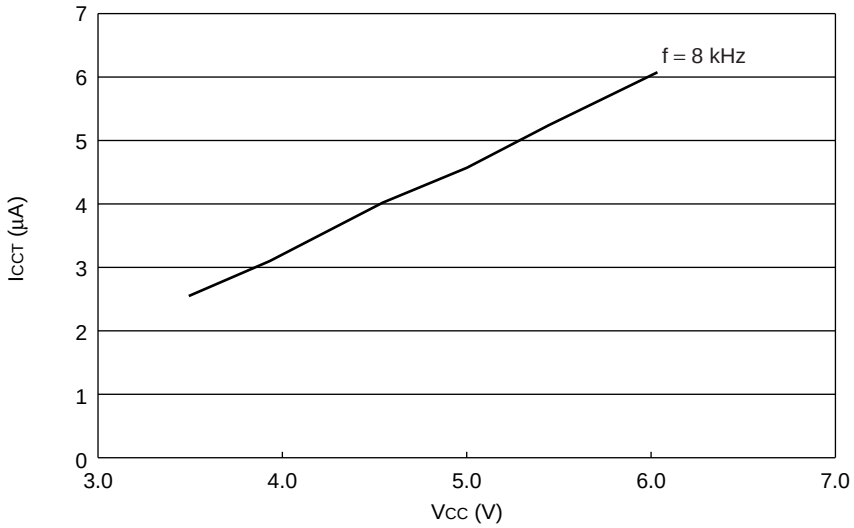
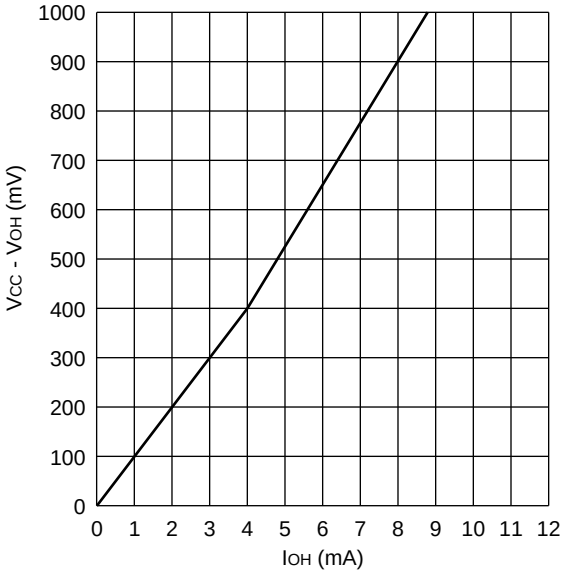
*(Continued)*

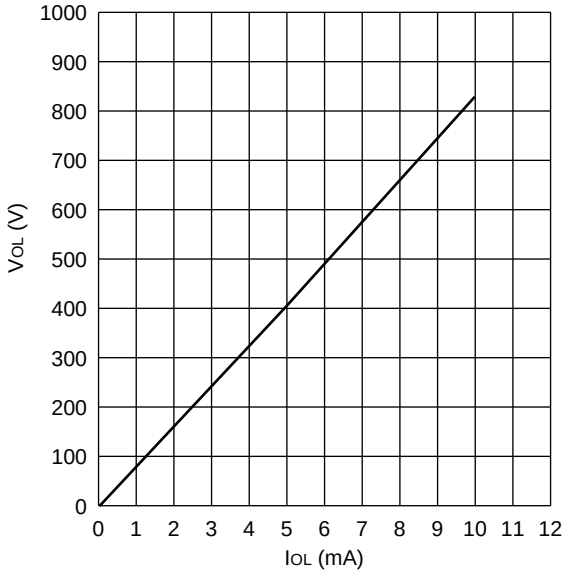
$I_{CCT}$ – $V_{CC}$
$T_A$ = + 25 °C, external clock operation
f = internal operation frequency




($V_{CC}$ – $V_{OH}$) – $I_{OH}$
$T_A$ = + 25 °C, $V_{CC}$ = 4.5 V



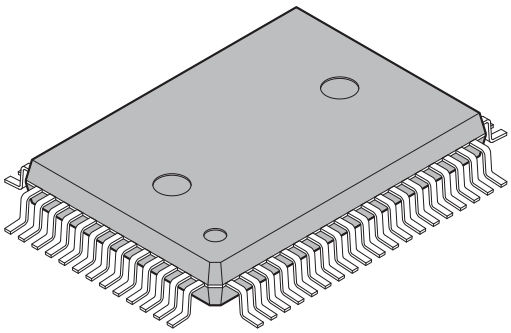

$V_{OL}$ – $I_{OL}$
$T_A$ = + 25 °C, $V_{CC}$ = 4.5 V



## ■ ORDERING INFORMATION

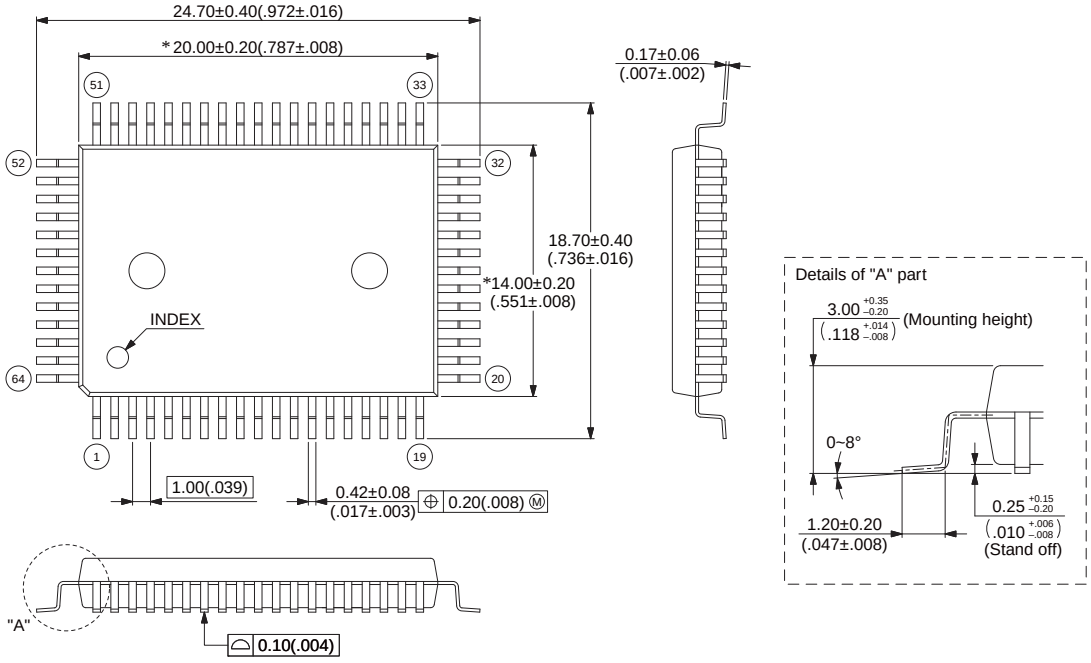
| Part Number | Package | Remarks |
|---|---|---|
| MB90F497GPF<br>MB90497GPF<br>MB90F498GPF | 64-pin plastic QFP<br>(FPT-64P-M06) | |
| MB90F497GPMC<br>MB90497GPMC<br>MB90F498GPMC | 64-pin plastic LQFP<br>(FPT-64P-M23) | |

## ■ PACKAGE DIMENSIONS

| 64-pin plastic QFP | | |
|---|---|---|
|  (FPT-64P-M06) | Lead pitch | 1.00 mm |
| | Package width × package length | 14 × 20 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 3.35 mm MAX |
| | Code (Reference) | P-QFP64-14×20-1.00 |
| | | |

64-pin plastic QFP
(FPT-64P-M06)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.





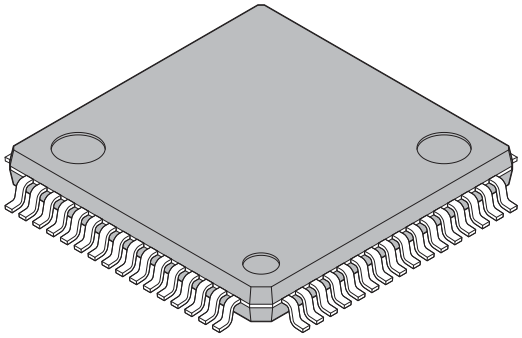

Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

*(Continued)*

*(Continued)*

64-pin plastic LQFP

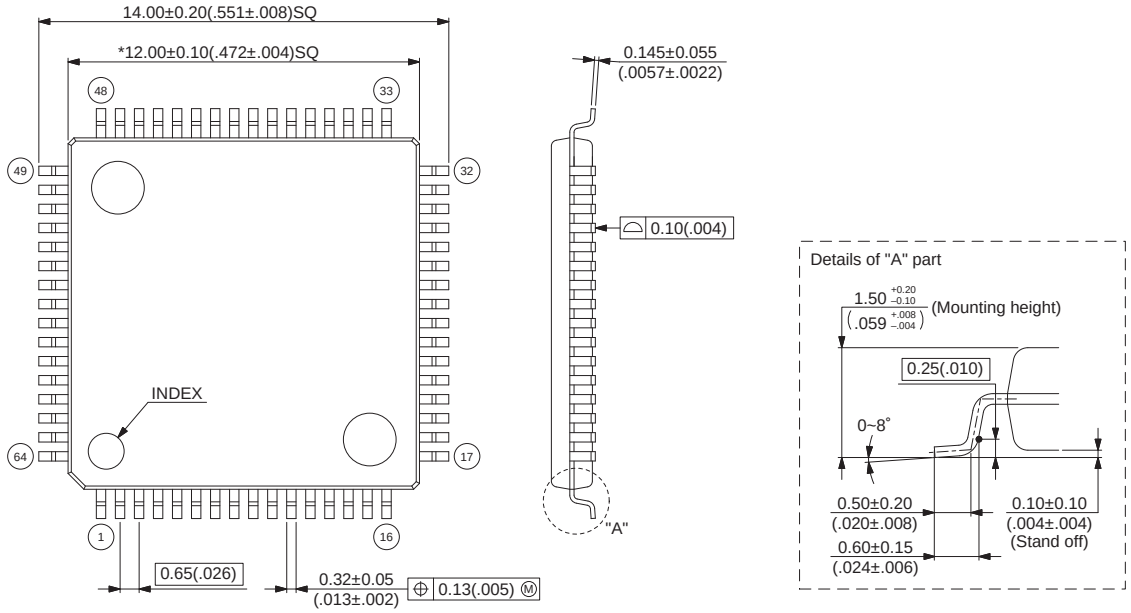


(FPT-64P-M23)

| | |
|---|---|
| Lead pitch | 0.65 mm |
| Package width × package length | 12.0 × 12.0 mm |
| Lead shape | Gullwing |
| Sealing method | Plastic mold |
| Mounting height | 1.70 mm MAX |
| Code (Reference) | P-LFQFP64-12×12-0.65 |
| | |

64-pin plastic LQFP
(FPT-64P-M23)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.






Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

## ■ MAIN CHANGES IN THIS EDITION

| Page | Section | Change Results |
|---|---|---|
| 18 | ■ BLOCK DIAGRAM<br>16-bit reload timer | Corrected the direction of arrow for TIN0, TIN1 signal.<br>"→ (output)"→ "← (input)" |
| 23 | ■ I/O MAP<br>Address : 0000AA$_H$ | Corrected the Initial Value of "Watch timer control register".<br>10001000$_B$ → 1X001000$_B$ |

The vertical lines marked in the left side of the page show the changes.

# MEMO

# MEMO

# MEMO

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