DS501-00006-0v01-E

Memory FRAM

4 M Bit (256 K × 16)

MB85R4002A

■ DESCRIPTIONS

The MB85R4002A is an FRAM (Ferroelectric Random Access Memory) chip consisting of 262,144 words × 16 bits of nonvolatile memory cells fabricated using ferroelectric process and silicon gate CMOS process technologies.
The MB85R4002A is able to retain data without using a back-up battery, as is needed for SRAM.
The memory cells used in the MB85R4002A can be used for 10^{10} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E^2PROM.
The MB85R4002A uses a pseudo-SRAM interface that is compatible with conventional asynchronous SRAM.

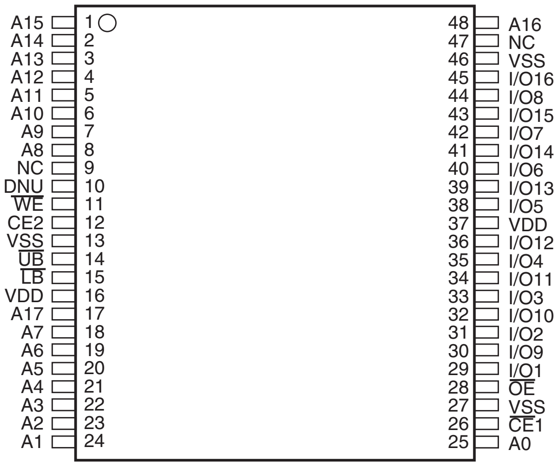
■ FEATURES

- Bit configuration : 262,144 words × 16 bits
- Read/write endurance : 10^{10} times
- Operating power supply voltage : 3.0 V to 3.6 V
- Operating temperature range : − 40 °C to + 85 °C
- Data retention : 10 years (+ 55 °C)
- $\overline{\text{LB}}$ and $\overline{\text{UB}}$ data byte control
- Package : 48-pin plastic TSOP (1)

2011.10

■ PIN ASSIGNMENTS

(TOP VIEW)

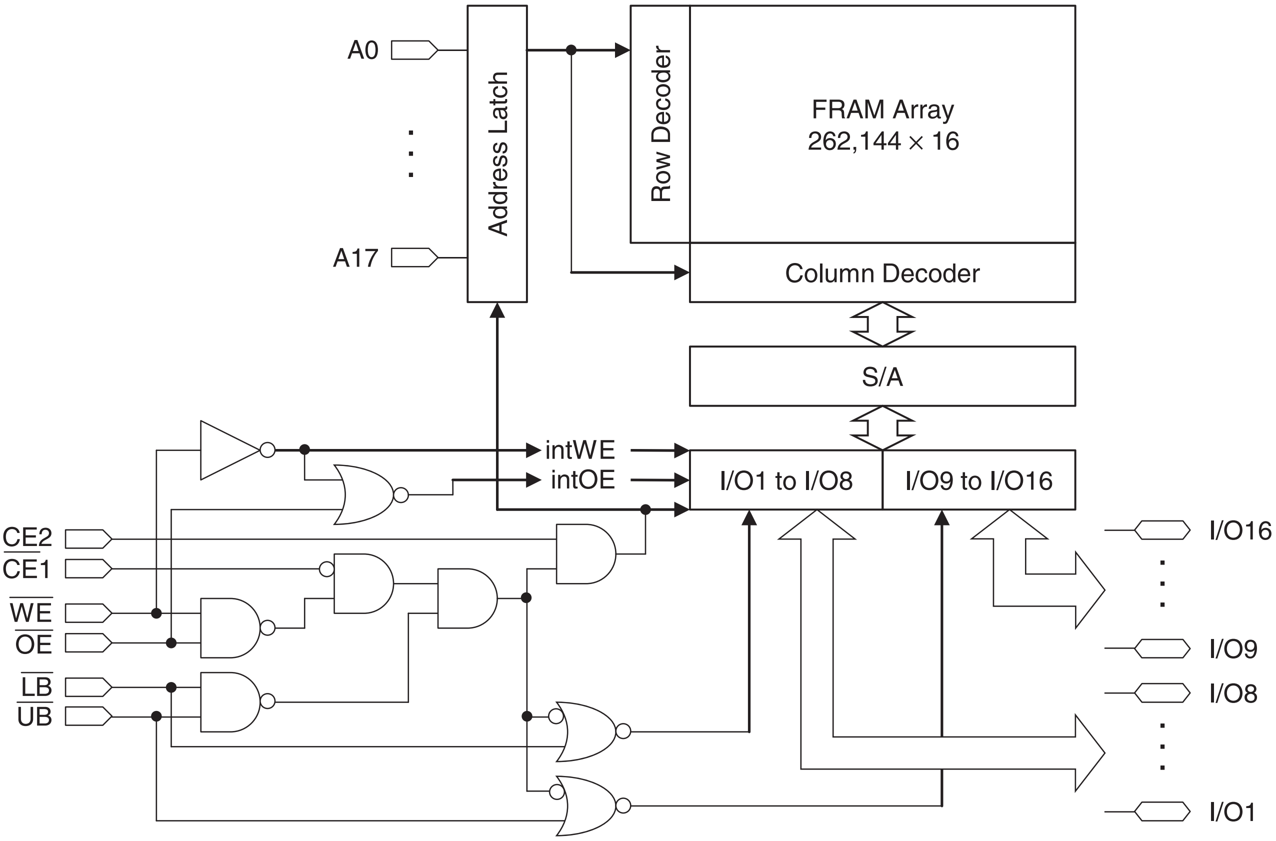


(FPT-48P-M48)

■ PIN DESCRIPTIONS

Pin Number	Pin Name	Functional Description
1 to 8, 17 to 25, 48	A0 to A17	Address Input pins
29 to 36, 38 to 45	I/O1 to I/O16	Data Input/Output pins
26	$\overline{CE}$1	Chip Enable 1 Input pin
12	CE2	Chip Enable 2 Input pin
11	$\overline{WE}$	Write Enable Input pin
28	$\overline{OE}$	Output Enable Input pin
14, 15	$\overline{LB}$, $\overline{UB}$	Data Byte Control Input pins
16, 37	VDD	Supply Voltage pins Connect all two pins to the power supply.
13, 27, 46	VSS	Ground pins Connect all three pins to ground.
9, 47	NC	No Connect pins
10	DNU	Do Not Use pin Make sure to connect this pin to VDD.

■ BLOCK DIAGRAM



■ FUNCTIONAL TRUTH TABLE

Mode	$\overline{\text{CE1}}$	CE2	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{LB}}$	$\overline{\text{UB}}$	I/O1 to I/O8	I/O9 to I/O16	Supply Current
Standby Precharge	H	X	X	X	X	X	Hi-Z	Hi-Z	Standby (I_{SB})
	X	L	X	X	X	X			
	X	X	H	H	X	X			
	X	X	X	X	H	H			
Read	↓	H	H	L	L	L	Data Output	Data Output	Operation (I_{CC})
					L	H	Data Output	Hi-Z	
					H	L	Hi-Z	Data Output	
	L	↑	H	L	L	L	Data Output	Data Output	
					L	H	Data Output	Hi-Z	
					H	L	Hi-Z	Data Output	
Read (Pseudo-SRAM, $\overline{\text{OE}}$ control*1)	L	H	H	↓	L	L	Data Output	Data Output	
					L	H	Data Output	Hi-Z	
					H	L	Hi-Z	Data Output	
Write	↓	H	L	H	L	L	Data Output	Data Output	
					L	H	Data Output	Hi-Z	
					H	L	Hi-Z	Data Output	
	L	↑	L	H	L	L	Data Output	Data Output	
					L	H	Data Output	Hi-Z	
					H	L	Hi-Z	Data Output	
Write (Pseudo-SRAM, $\overline{\text{WE}}$ control*2)	L	H	↓	H	L	L	Data Input	Data Input	
					L	H	Data Input	Hi-Z	
					H	L	Hi-Z	Data Input	

Note: L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, Hi-Z = High Impedance

↓ : Latch address and latch data at falling edge, ↑ : Latch address and latch data at rising edge

*1 : $\overline{\text{OE}}$ control of the Pseudo-SRAM means the valid address at the falling edge of $\overline{\text{OE}}$ to read.

*2 : $\overline{\text{WE}}$ control of the Pseudo-SRAM means the valid address and data at the falling edge of $\overline{\text{WE}}$ to write.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power Supply Voltage*	V_{CC}	–0.5	+4.0	V
Input Pin Voltage*	V_{IN}	–0.5	V_{CC} + 0.5 (≤ 4.0)	V
Output Pin Voltage*	V_{OUT}	–0.5	V_{CC} + 0.5 (≤ 4.0)	V
Operating Ambient Temperature	T_A	–40	+85	°C
Storage Temperature	T_{STG}	–40	+125	°C

* : All voltages are referenced to VSS (ground 0 V).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage*	V_{CC}	3.0	3.3	3.6	V
High Level Input Voltage*	V_{IH}	V_{CC} × 0.8	—	V_{CC} + 0.5 (≤ 4.0)	V
Low Level Input Voltage*	V_{IL}	–0.5	—	+0.6	V
Operating Ambient Temperature	T_A	– 40	—	+85	°C

* : All voltages are referenced to VSS (ground 0 V).

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Leakage Current*3	$\vert I_{LI} \vert$	V_{IN} = 0 V to V_{CC}	—	—	10	µA
Output Leakage Current	$\vert I_{LO} \vert$	V_{OUT} = 0 V to V_{CC}, $\overline{CE}1 = V_{IH}$ or $\overline{OE} = V_{IH}$	—	—	10	µA
Operating Power Supply Current	I_{CC}	$\overline{CE}1$ = 0.2 V, CE2 = V_{CC} – 0.2 V, I_{out} = 0 mA*1	—	15	20	mA
Standby Current	I_{SB}	$\overline{CE}1 \geq V_{CC}$ – 0.2 V	—	50	150	µA
		CE2 ≤ 0.2 V*2				
		$\overline{OE} \geq V_{CC}$ – 0.2 V, $\overline{WE} \geq V_{CC}$ – 0.2 V*2				
		$\overline{LB} \geq V_{CC}$ – 0.2 V, $\overline{UB} \geq V_{CC}$ – 0.2 V*2				
High Level Output Voltage	V_{OH}	I_{OH} = – 1.0 mA	$V_{CC} \times 0.8$	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = 2.0 mA	—	—	0.4	V

*1 : During the measurement of I_{CC} , the Address, Data In were taken to only change once per active cycle.
Iout : output current

*2 : All pins other than setting pins should be input at the CMOS level voltages such as H ≥ V_{CC} – 0.2 V, L ≤ 0.2 V.

*3 : This also applies to DNU pins.

2. AC Characteristics

- **AC Test Conditions**

Supply Voltage	: 3.0 V to 3.6 V
Operating Ambient Temperature	: –40 °C to +85 °C
Input Voltage Amplitude	: 0.3 V to 2.7 V
Input Rising Time	: 5 ns
Input Falling Time	: 5 ns
Input Evaluation Level	: 2.0 V / 0.8 V
Output Evaluation Level	: 2.0 V / 0.8 V
Output Impedance	: 50 pF

(1) Read Cycle

(within recommended operating conditions)

Parameter	Symbol	Value		Unit
		Min	Max	
Read Cycle time	t_{RC}	150	—	ns
$\overline{CE}$1 Active Time	t_{CA1}	120	—	ns
CE2 Active Time	t_{CA2}	120	—	ns
$\overline{OE}$ Active Time	t_{RP}	120	—	ns
$\overline{LB}$, $\overline{UB}$ Active Time	t_{BP}	120	—	ns
Precharge Time	t_{PC}	20	—	ns
Address Setup Time	t_{AS}	0	—	ns
Address Hold Time	t_{AH}	50	—	ns
$\overline{OE}$ Setup Time	t_{ES}	0	—	ns
$\overline{LB}$, $\overline{UB}$ Setup Time	t_{BS}	5	—	ns
Output Data Hold time	t_{OH}	0	—	ns
Output Set Time	t_{LZ}	30	—	ns
$\overline{CE}$1 Access Time	t_{CE1}	—	120	ns
CE2 Access Time	t_{CE2}	—	120	ns
$\overline{OE}$ Access Time	t_{OE}	—	120	ns
Output Floating Time	t_{OHZ}	—	20	ns

(2) Write Cycle

(within recommended operating conditions)

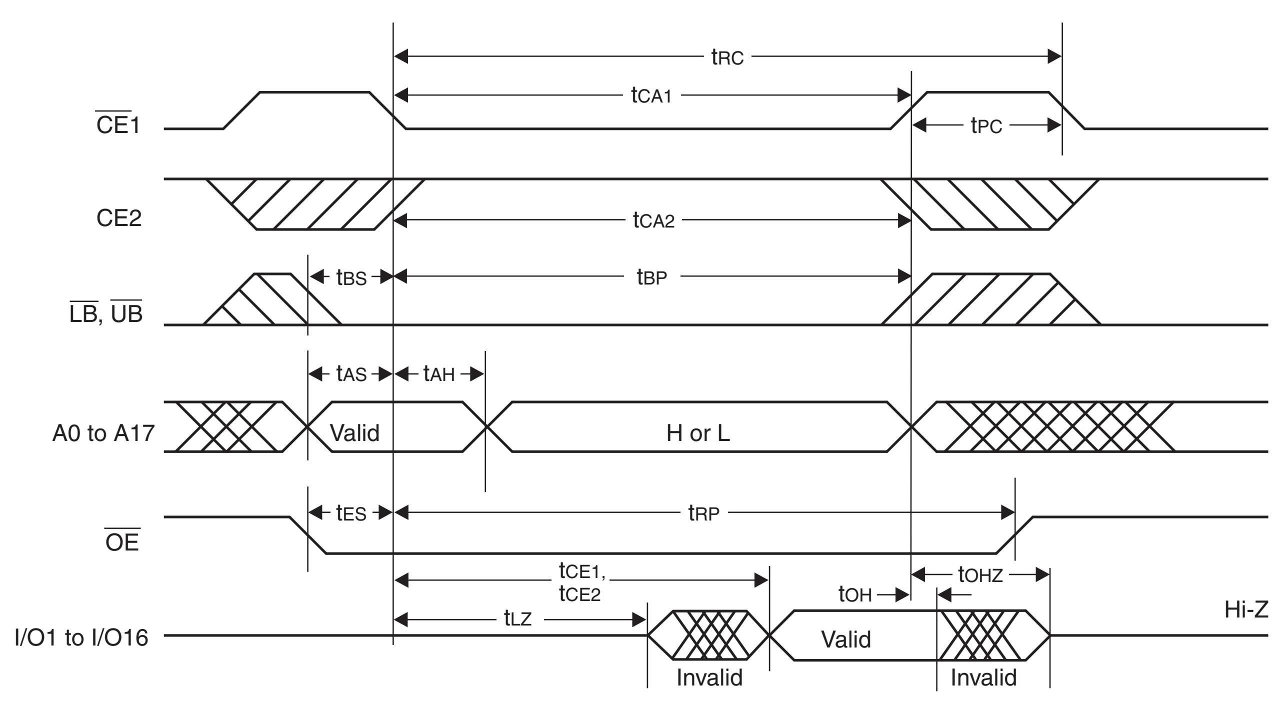
Parameter	Symbol	Value		Unit
		Min	Max	
Write Cycle Time	t_{WC}	150	—	ns
$\overline{CE}$1 Active Time	t_{CA1}	120	—	ns
CE2 Active Time	t_{CA2}	120	—	ns
$\overline{LB}$, $\overline{UB}$ Active Time	t_{BP}	120	—	ns
Precharge Time	t_{PC}	20	—	ns
Address Setup Time	t_{AS}	0	—	ns
Address Hold Time	t_{AH}	50	—	ns
$\overline{LB}$, $\overline{UB}$ Setup Time	t_{BS}	5	—	ns
Write Pulse Width	t_{WP}	120	—	ns
Data Setup Time	t_{DS}	0	—	ns
Data Hold Time	t_{DH}	50	—	ns
Write Setup Time	t_{WS}	0	—	ns

3. Pin Capacitance

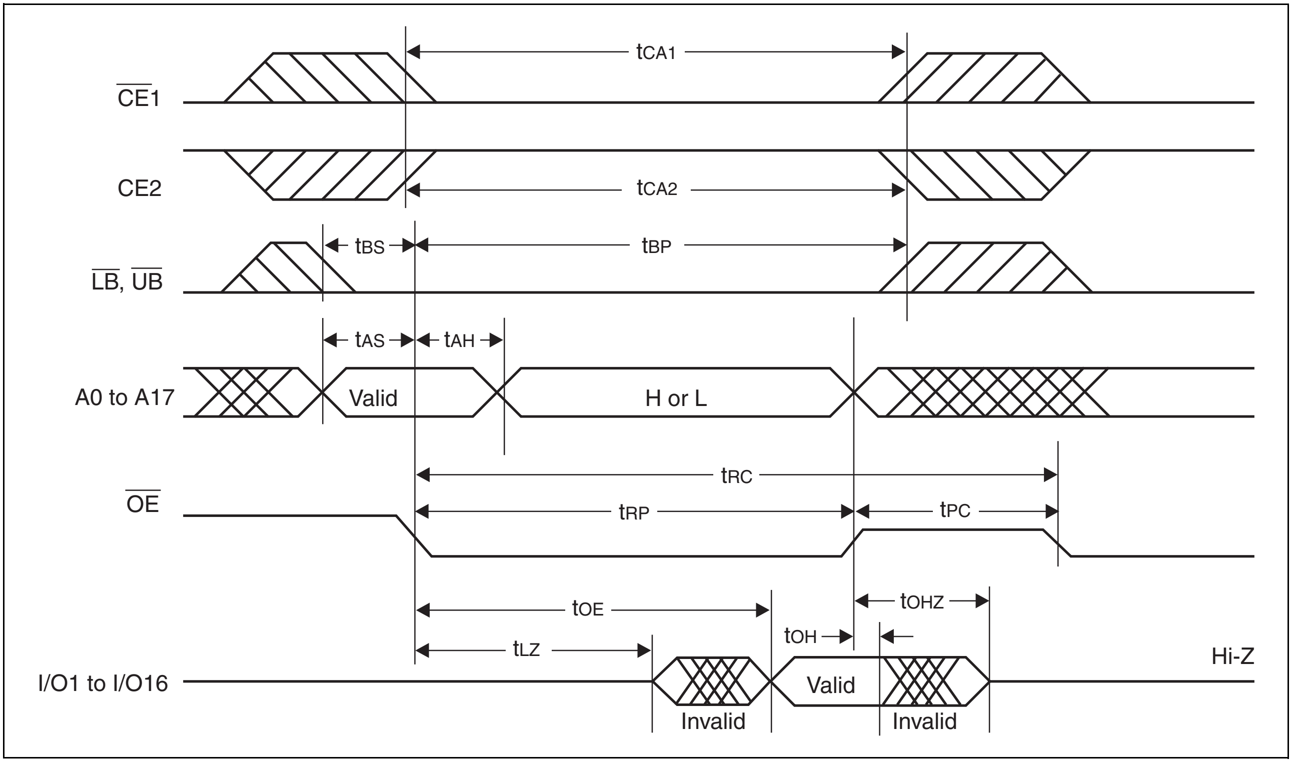
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Capacitance	C_{IN}	$V_{IN} = V_{OUT} = 0$ V, f = 1 MHz, $T_A = +25$ °C	—	—	10	pF
Output Capacitance	C_{OUT}		—	—	10	pF
DNU Pin Input Capacitance	C_{DNU}		—	—	10	pF

■ TIMING DIAGRAMS

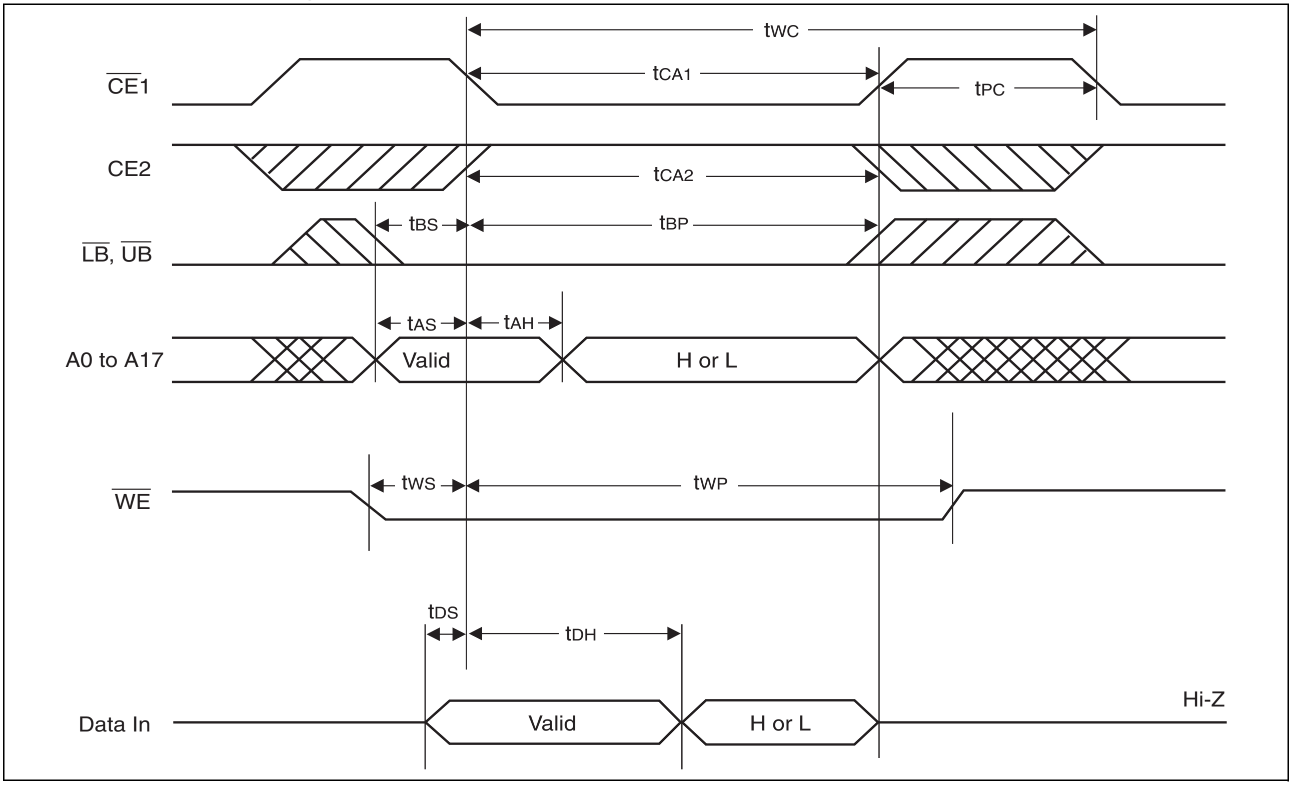
1. Read Cycle Timing ($\overline{\text{CE}}$1, CE2 Control)



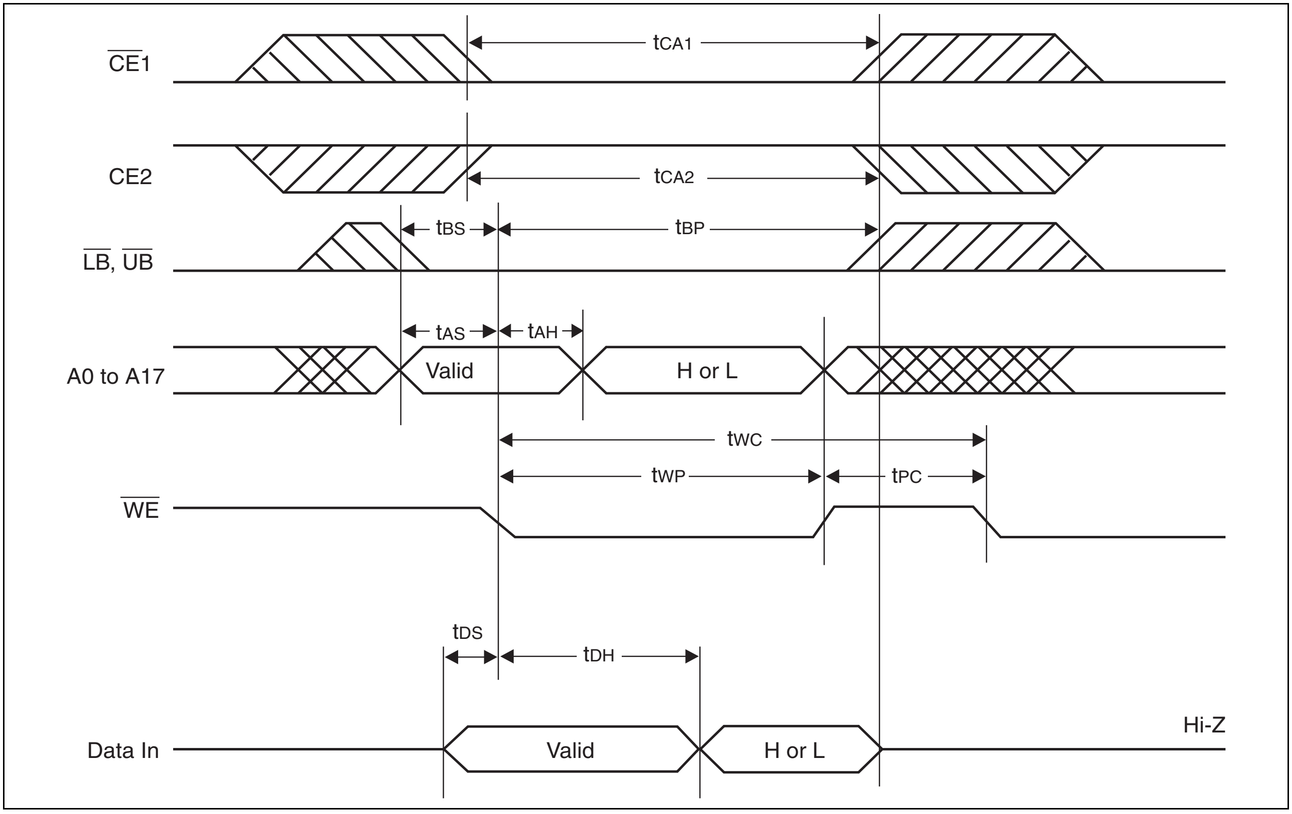
2. Read Cycle Timing ($\overline{\text{OE}}$ Control)



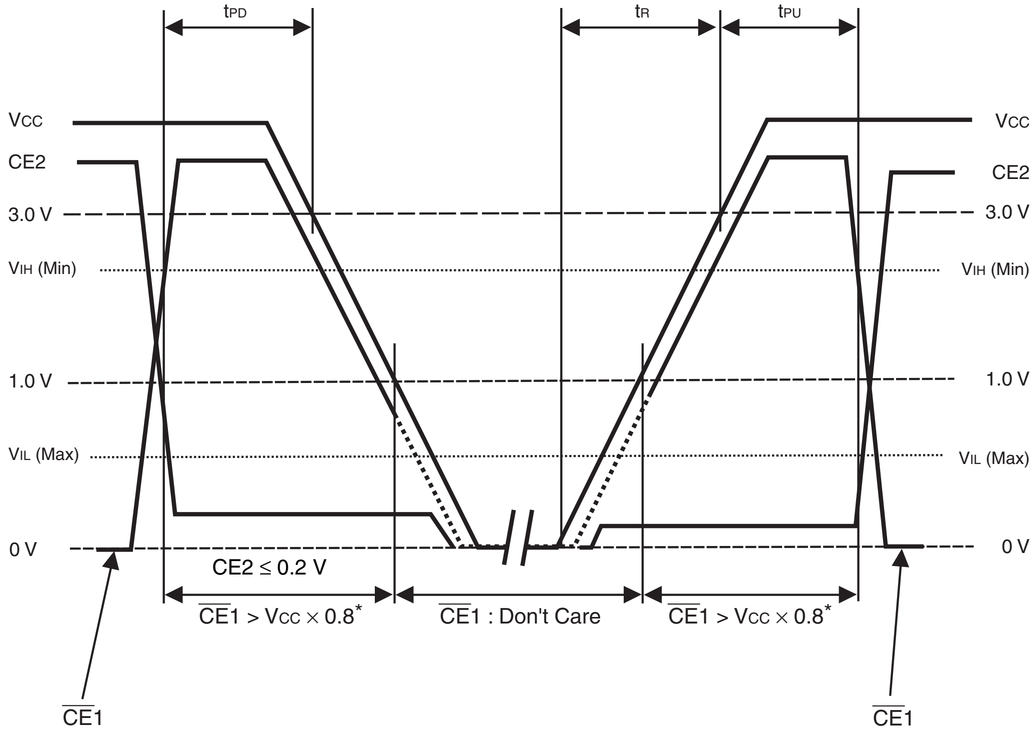
3. Write Cycle Timing ($\overline{\text{CE}}$1, CE2 Control)



4. Write Cycle Timing ($\overline{\text{WE}}$ Control)



■ POWER ON/OFF SEQUENCE



* : $\overline{\text{CE}}1$ (Max) < V_{CC} + 0.5 V

Notes:
- Use either of $\overline{\text{CE}}1$ or CE2, or both for disable control of the device.
- Because turning the power on from an intermediate level may cause malfunctions, when the power is turned on, V_{CC} is required to be started from 0 V.
- If the device does not operate within the specified conditions of read cycle, write cycle, power on/off sequence, memory data can not be guaranteed.
- When turning the power on or off, it is recommended that CE2 is connected to ground to prevent unexpected writing.

(within recommended operating conditions)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
$\overline{\text{CE}}1$ LEVEL hold time for Power OFF	t_{PD}	85	—	—	ns
$\overline{\text{CE}}1$ LEVEL hold time for Power ON	t_{PU}	85	—	—	ns
Power supply rising time	t_R	0.05	—	200	ms

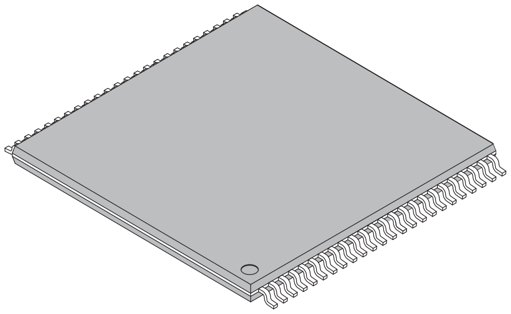
■ NOTES ON USE

After the IR reflow completed, it is not guaranteed to hold the data written prior to the IR reflow.

■ ORDERING INFOMATION

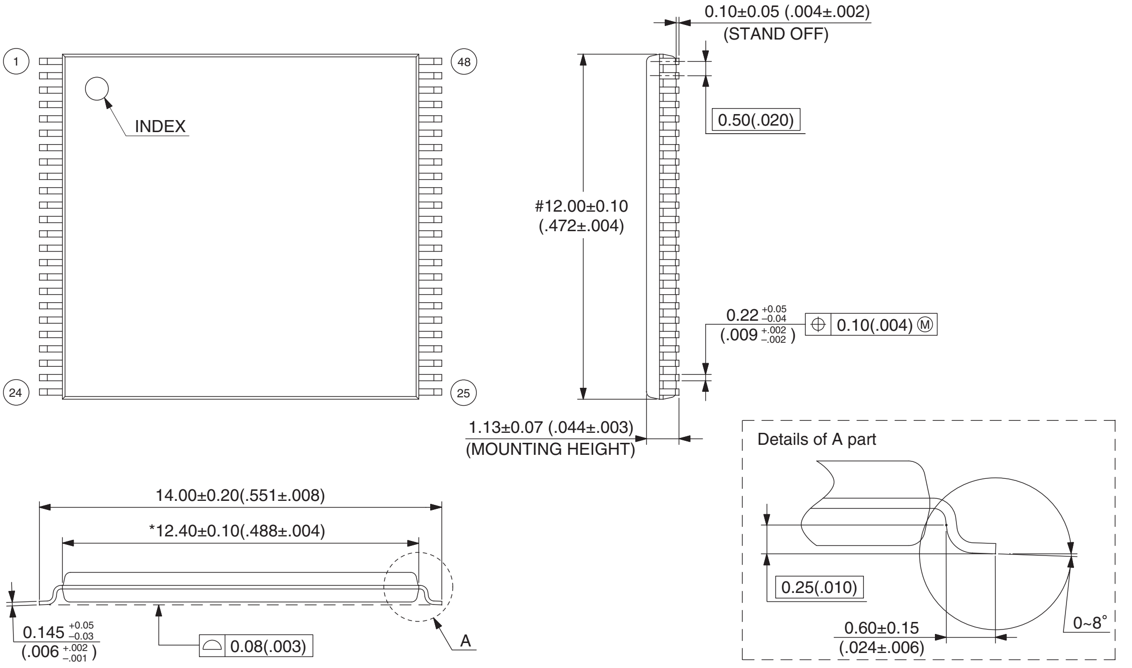
Part number	Package
MB85R4002ANC-GE1	48-pin plastic TSOP(1) (FPT-48P-M48)

■ PACKAGE DIMENSIONS

<table>
<tr><td rowspan="7">48-pin plastic TSOP

(FPT-48P-M48)</td><td>Lead pitch</td><td>0.50 mm</td></tr>
<tr><td>Package width × package length</td><td>12.00 mm × 12.40 mm</td></tr>
<tr><td>Lead shape</td><td>Gullwing</td></tr>
<tr><td>Sealing method</td><td>Plastic mold</td></tr>
<tr><td>Mounting height</td><td>1.20 mm MAX</td></tr>
<tr><td>Weight</td><td>0.36 g</td></tr>
<tr><td></td><td></td></tr>
</table>

48-pin plastic TSOP
(FPT-48P-M48)

Note 1) # : Resin protrusion. (Each side : +0.15 (.006) Max).
Note 2) * : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

MEMO

MEMO

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