Freescale Semiconductor
Advance Information

MR2A16A/D
Rev. 0.1, 7/2004

256K x 16-Bit 3.3-V Asynchronous Magnetoresistive RAM

Introduction

The MR2A16A is a 4,194,304-bit magnetoresistive random access memory (MRAM) device organized as 262,144 words of 16 bits. The MR2A16A is equipped with chip enable ($\overline{E}$), write enable ($\overline{W}$), and output enable ($\overline{G}$) pins, allowing for significant system design flexibility without bus contention. Because the MR2A16A has separate byte-enable controls ($\overline{LB}$ and $\overline{UB}$), individual bytes can be written and read.

MRAM is a nonvolatile memory technology that protects data in the event of power loss and does not require periodic refreshing. The MR2A16A is the ideal memory solution for applications that must permanently store and retrieve critical data quickly.

The MR2A16A is available in a 400-mil, 44-lead plastic small-outline TSOP type-II package with an industry-standard center power and ground SRAM pinout.

Features

- Single 3.3-V power supply
- Commercial temperature range (0°C to 70°C)
- Symmetrical high-speed read and write with fast access time (25 ns)
- Flexible data bus control — 8 bit or 16 bit access
- Equal address and chip-enable access times
- Automatic data protection with low-voltage inhibit circuitry to prevent writes on power loss
- All inputs and outputs are transistor-transistor logic (TTL) compatible
- Fully static operation
- Full nonvolatile operation with 10 years minimum data retention

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

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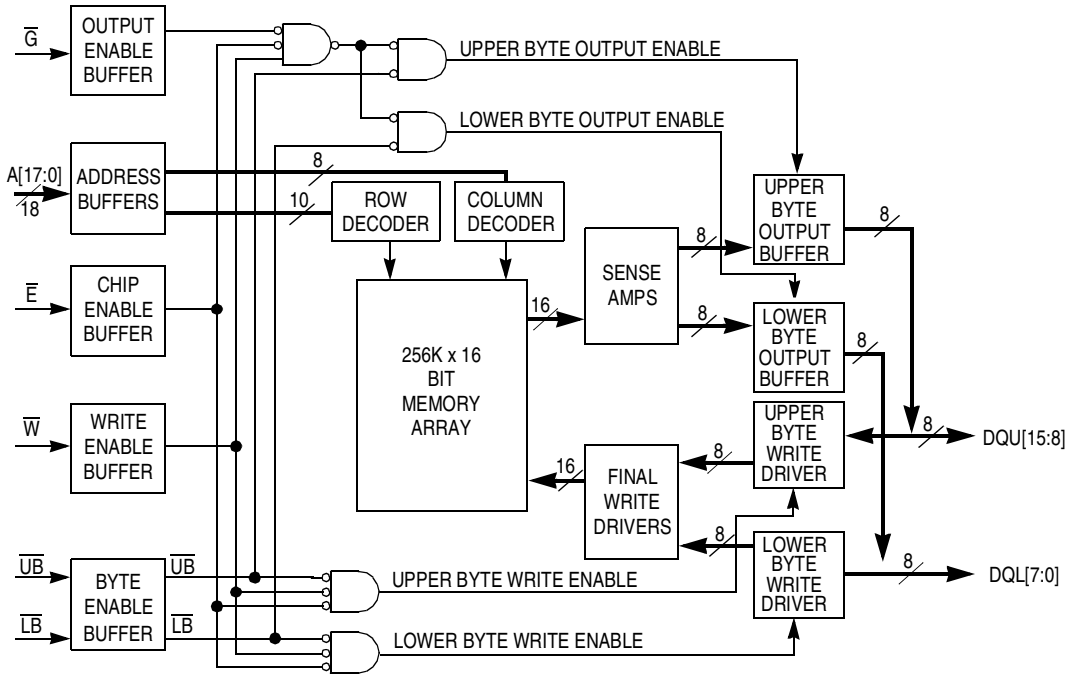


Figure 1. Block Diagram

Device Pin Assignment

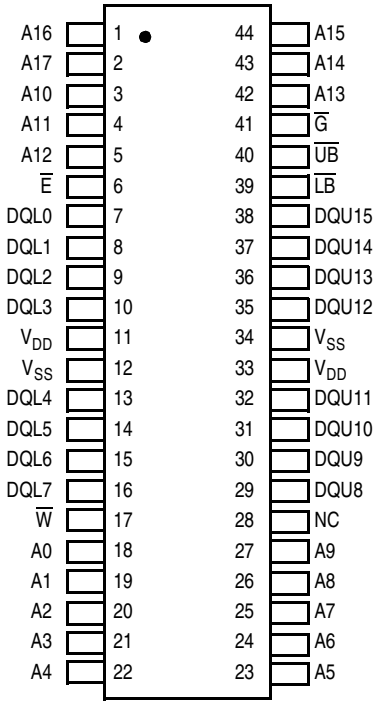


Table 1. Pin Functions

Signal Name	Function
A[17:0]	Address input
$\overline{E}$	Chip enable
$\overline{W}$	Write enable
$\overline{G}$	Output enable
$\overline{UB}$	Upper byte select
$\overline{LB}$	Lower byte select
DQL[7:0]	Data I/O, lower byte
DQU[15:8]	Data I/O, upper byte
V_{DD}	+3.3-V power supply
V_{SS}	Ground
NC	Do not connect this pin

Figure 2. MR2A16A in 44-Pin TSOP Type II Package

Table 2. Operating Modes

$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{LB}$	$\overline{UB}$	Mode	V_{DD} Current	DQL[7:0]	DQU[15:8]
H	X	X	X	X	Not selected	I_{SB1}, I_{SB2}	Hi-Z	Hi-Z
L	H	H	X	X	Output disabled	I_{DDA}	Hi-Z	Hi-Z
L	X	X	H	H	Output disabled	I_{DDA}	Hi-Z	Hi-Z
L	L	H	L	H	Lower byte read	I_{DDA}	D_{Out}	Hi-Z
L	L	H	H	L	Upper byte read	I_{DDA}	Hi-Z	D_{Out}
L	L	H	L	L	Word read	I_{DDA}	D_{Out}	D_{Out}
L	X	L	L	H	Lower byte write	I_{DDA}	D_{In}	Hi-Z
L	X	L	H	L	Upper byte write	I_{DDA}	Hi-Z	D_{In}
L	X	L	L	L	Word write	I_{DDA}	D_{In}	D_{In}

NOTES:
1. H = high, L = low, X = don't care
2. Hi-Z = high impedance

Electrical Specifications

Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.5 to 4.6	V
Voltage on any pin	V_{In}	–0.5 to V_{DD} + 0.5	V
Output current per pin	I_{Out}	±20	mA
Package power dissipation	P_D	TBD	W
Temperature under bias	T_{Bias}	–10 to 85	°C
Storage temperature	T_{stg}	–55 to 150	°C
Lead temperature during solder (3 minute max)	T_{Lead}	235	°C
Maximum magnetic field at package surface	H_{max}	20	oe

NOTES:
1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.
2. All voltages are referenced to V_{SS}.
3. Power dissipation capability depends on package characteristics and use environment.

Table 4. Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{DD}	3.0[1]	3.3	3.6	V
Write inhibit voltage	V_{WI}	2.5	2.7	3.0[1]	V
Input high voltage	V_{IH}	2.2	—	V_{DD} + 0.3[2]	V
Input low voltage	V_{IL}	–0.5[3]	—	0.8	V
Operating temperature	T_A	0		70	°C

NOTES:
1. After power up or if V_{DD} falls below V_{WI}, a waiting period of 1 μs must be observed.
   Memory is designed to prevent writing for all input pin conditions if V_{DD} falls below minimum V_{WI}.
2. V_{IH} (max) = V_{DD} + 0.3 Vdc; V_{IH} (max) = V_{DD} + 2.0 Vac (pulse width ≤ 10 ns) for I ≤ 20.0 mA.
3. V_{IL} (min) = –0.5 Vdc; V_{IL} (min) = –2.0 Vac (pulse width ≤ 10 ns) for I ≤ 20.0 mA.

Direct Current (dc)

Table 5. dc Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Input leakage current	$I_{lkg(I)}$	—	—	±1	μA
Output leakage current	$I_{lkg(O)}$	—	—	±1	μA
Output low voltage (I_{OL} = +4 mA) (I_{OL} = +100 μA)	V_{OL}	—	—	0.4 V_{SS} + 0.2	V
Output high voltage (I_{OH} = –4 mA) (I_{OH} = –100 mA)	V_{OH}	2.4 V_{DD} – 0.2	—	—	V

Table 6. Power Supply Characteristics

Parameter	Timing Set	Symbol	Typ	Max	Unit
ac active supply current — Read Modes (I_{Out} = 0 mA, V_{DD} = max)	20	I_{DDR}	TBD	TBD	mA
	25	I_{DDR}	TBD	TBD	mA
	35	I_{DDR}	TBD	TBD	mA
ac active supply current — Write Modes (V_{DD} = max)	20	I_{DDW}	TBD	TBD	mA
	25	I_{DDW}	TBD	TBD	mA
	35	I_{DDW}	TBD	TBD	mA
ac standby current (V_{DD} = max, $\overline{E}$ = V_{IH}) (no other restrictions on other inputs)	20	I_{SB1}	TBD	TBD	mA
	25	I_{SB1}	TBD	TBD	mA
	35	I_{SB1}	TBD	TBD	mA
CMOS standby current ($\overline{E}$ ≥ V_{DD} – 0.2 V and V_{In} ≤ V_{SS} + 0.2 V or ≥ V_{DD} – 0.2 V) (V_{DD} = max, f = 0 MHz)		I_{SB2}	TBD	TBD	mA

Table 7. Capacitance

Parameter	Symbol	Typ	Max	Unit
Address input capacitance	C_{In}	—	6	pF
Control input capacitance	C_{In}	—	6	pF
Input/Output capacitance	$C_{I/O}$	—	8	pF

NOTES:
1. (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, periodically sampled rather than 100% tested)

Table 8. ac Measurement Conditions

Parameter	Value
Logic input timing measurement reference level	1.5 V
Logic output timing measurement reference level	1.5 V
Logic input pulse levels	0 or 3.0 V
Input rise/fall time	2 ns
Output load for low and high impedance parameters	See Figure 3A
Output load for all other timing parameters	See Figure 3B

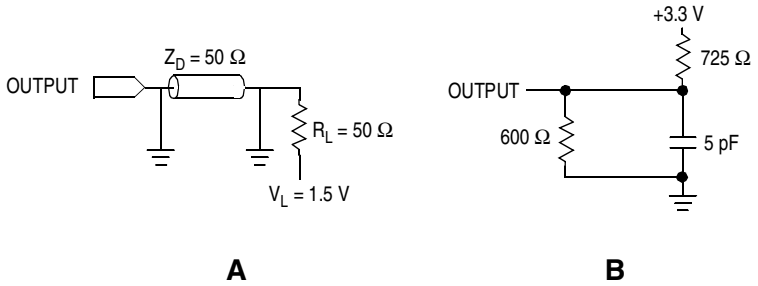


Figure 3. Output Load for ac Test

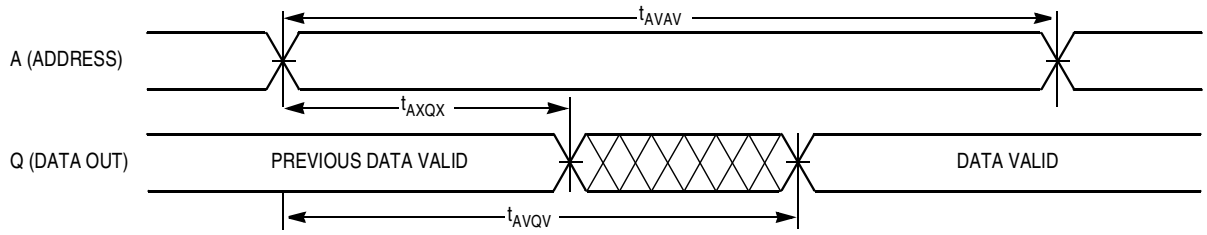
Timing Specifications

Read Mode

Table 9. Read Cycle Timing (See Notes 1 and 2)

Parameter	Symbol	Timing Set						Unit	Notes
		20		25		35			
		Min	Max	Min	Max	Min	Max		
Read cycle time	t_{AVAV}	20	—	25	—	35	—	ns	
Address access time	t_{AVQV}	—	20	—	25	—	35	ns	
Enable access time	t_{ELQV}	—	20	—	25	—	35	ns	3
Output enable access time	t_{GLQV}	—	10	—	11	—	15	ns	
Byte enable access time	t_{BLQV}	—	10	—	11	—	15	ns	
Output hold from address change	t_{AXQX}	3	—	3	—	3	—	ns	
Enable low to output active	t_{ELQX}	3	—	3	—	3	—	ns	4, 5
Output enable low to output active	t_{GLQX}	0	—	0	—	0	—	ns	4, 5
Byte enable low to output active	t_{BLQX}	0	—	0	—	0	—	ns	4, 5
Enable high to output Hi-Z	t_{EHQZ}	0	10	0	11	0	15	ns	4, 5
Output enable high to output Hi-Z	t_{GHQZ}	0	6	0	7	0	10	ns	4, 5
Byte high to output Hi-Z	t_{BHQZ}	0	6	0	7	0	10	ns	4, 5

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Due to product sensitivities to noise, power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles.
3. Addresses valid before or at the same time $\overline{E}$ goes low.
4. This parameter is sampled and not 100% tested.
5. Transition is measured ±200 mV from steady-state voltage.



NOTES:

1. Device is continuously selected ($\overline{E} \leq V_{IL}$, $\overline{G} \leq V_{IL}$).

Figure 4. Read Cycle 1

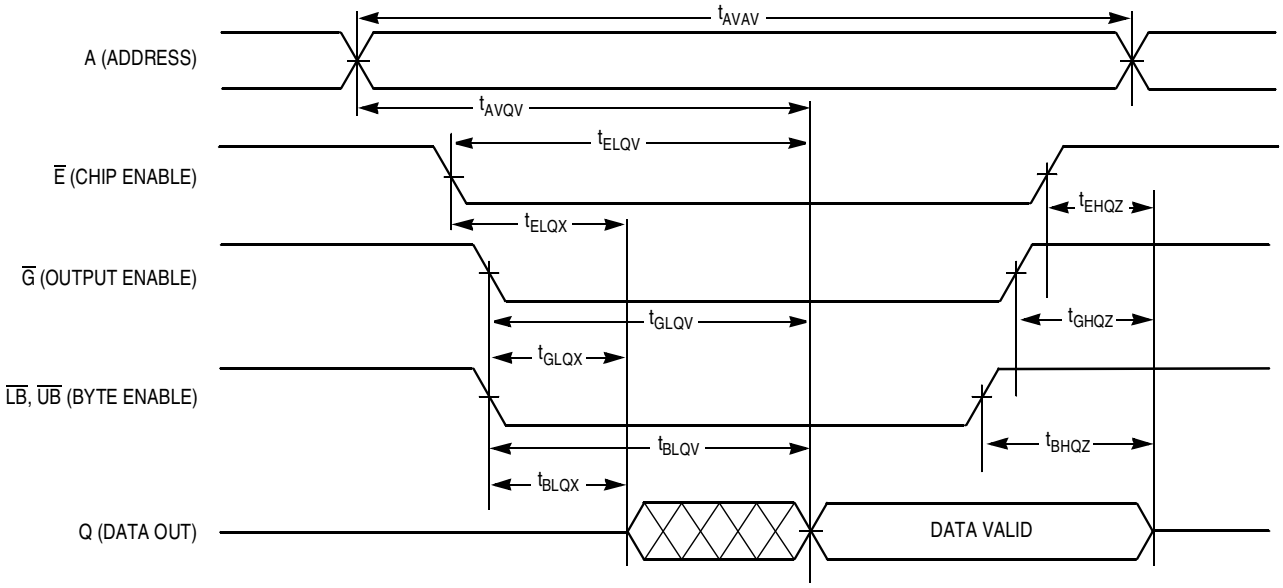


Figure 5. Read Cycle 2

Write Mode

Table 10. Write Cycle Timing 1 ($\overline{W}$ Controlled; See Notes 1, 2, 3, and 4)

Parameter	Symbol	Timing Set						Unit	Notes
		20		25		35			
		Min	Max	Min	Max	Min	Max		
Write cycle time	t_{AVAV}	20	—	25	—	35	—	ns	8
Address set-up time	t_{AVWL}	0	—	0	—	0	—	ns	
Address valid to end of write ($\overline{G}$ high)	t_{AVWH}	12	—	15	—	18	—	ns	
Address valid to end of write ($\overline{G}$ low)	t_{AVWH}	15	—	17	—	20	—	ns	
Write pulse width ($\overline{G}$ high)	t_{WLWH} t_{WLEH}	8	—	10	—	15	—	ns	
Write pulse width ($\overline{G}$ low)	t_{WLWH} t_{WLEH}	8	—	10	—	15	—	ns	
Data valid to end of write	t_{DVWH}	5	—	6	—	10	—	ns	
Data hold time	t_{WHDX}	0	—	0	—	0	—	ns	
Write low to data Hi-Z	t_{WLQZ}	0	7	0	9	0	12	ns	5, 6, 7
Write high to output active	t_{WHQX}	3	—	3	—	3	—	ns	5, 6, 7
Write recovery time	t_{WHAX}	8	—	10	—	12	—	ns	

NOTES:

1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Due to product sensitivities to noise, power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles.
3. If $\overline{G}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
4. After $\overline{W}$, $\overline{E}$, or $\overline{UB}/\overline{LB}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns.
5. This parameter is sampled and not 100% tested.
6. Transition is measured ±200 mV from steady-state voltage.
7. At any given voltage or temperature, t_{WLQZ} max < t_{WHQX} min.
8. All write cycle timings are referenced from the last valid address to the first transition address.

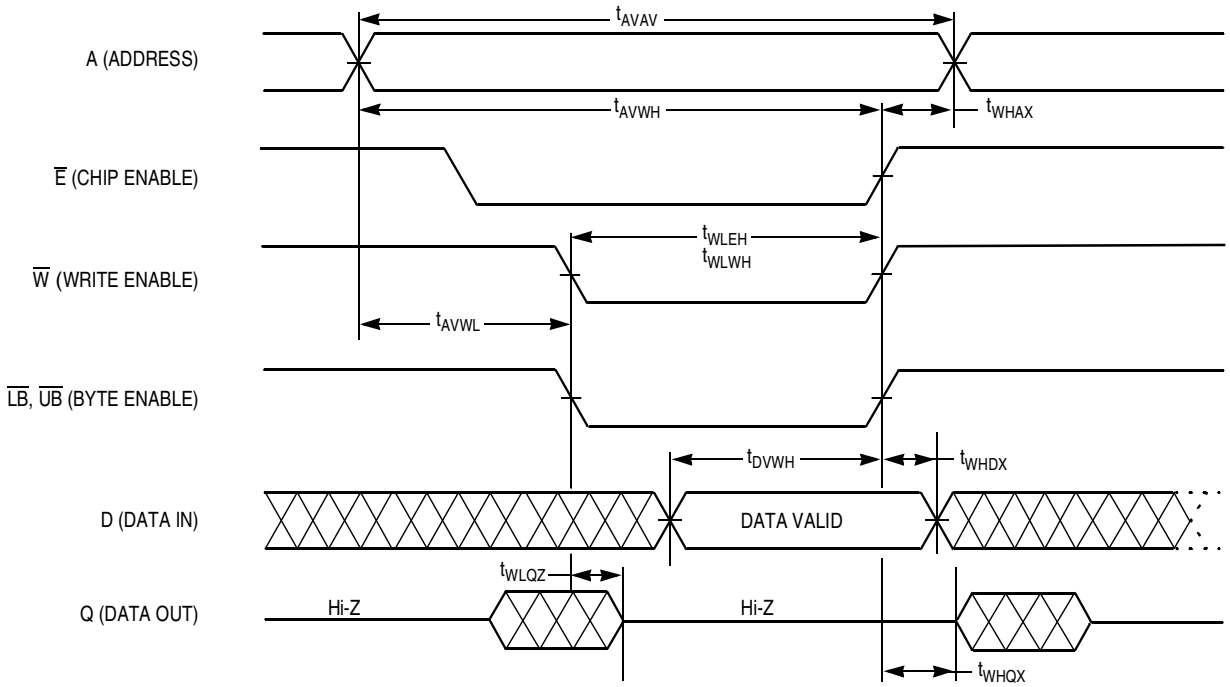


Figure 6. Write Cycle 1 ($\overline{W}$ Controlled)

Table 11. Write Cycle Timing 2 ($\overline{E}$ Controlled; See Notes 1,2,3, and 4)

Parameter	Symbol	Timing Set						Unit	Notes
		20		25		35			
		Min	Max	Min	Max	Min	Max		
Write cycle time	t_{AVAV}	20	—	25	—	35	—	ns	7
Address set-up time	t_{AVEL}	0	—	0	—	0	—	ns	
Address valid to end of write ($\overline{G}$ high)	t_{AVEH}	12	—	15	—	18	—	ns	
Address valid to end of write ($\overline{G}$ low)	t_{AVEH}	15	—	17	—	20	—	ns	
Enable to end of write ($\overline{G}$ high)	t_{ELEH} t_{ELWH}	8	—	10	—	15	—	ns	
Enable to end of write ($\overline{G}$ low)	t_{ELEH} t_{ELWH}	8	—	10	—	15	—	ns	5, 6
Data valid to end of write	t_{DVEH}	5	—	6	—	10	—	ns	
Data hold time	t_{EHDX}	0	—	0	—	0	—	ns	
Write recovery time	t_{EHAX}	8	—	10	—	12	—	ns	

NOTES:

1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Due to product sensitivities to noise, power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles.
3. If $\overline{G}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
4. After $\overline{W}$, $\overline{E}$, or $\overline{UB}/\overline{LB}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns.
5. If $\overline{E}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
6. If $\overline{E}$ goes high at the same time or before $\overline{W}$ goes high, the output will remain in a high-impedance state.
7. All write cycle timings are referenced from the last valid address to the first transition address.

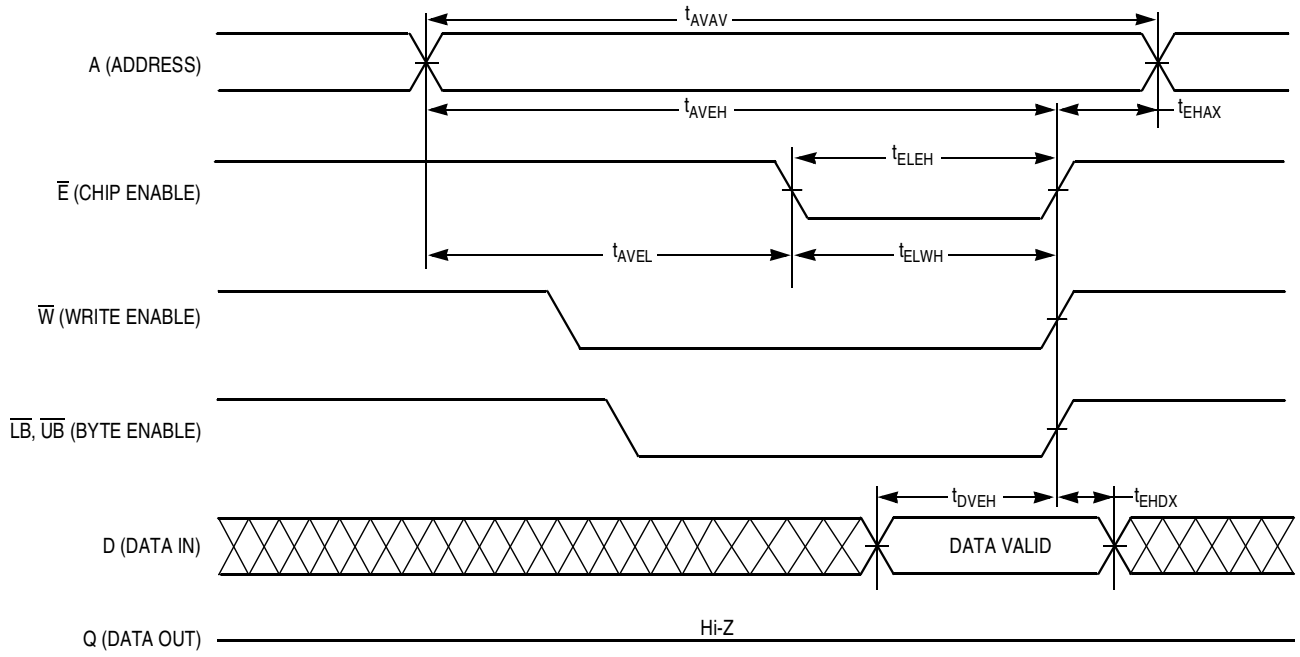


Figure 7. Write Cycle 2 ($\overline{E}$ Controlled)

Table 12. Write Cycle Timing 3 ($\overline{LB}$/$\overline{UB}$ Controlled; See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol	Timing Set						Unit	Notes
		20		25		35			
		Min	Max	Min	Max	Min	Max		
Write cycle time	t_{AVAV}	20	—	25	—	35	—	ns	6
Address set-up time	t_{AVBL}	0	—	0	—	0	—	ns	
Address valid to end of write ($\overline{G}$ high)	t_{AVBH}	12	—	15	—	18	—	ns	
Address valid to end of write ($\overline{G}$ low)	t_{AVBH}	15	—	17	—	20	—	ns	
Byte pulse width ($\overline{G}$ high)	t_{BLEH} t_{BLWH}	8	—	10	—	15	—	ns	
Byte pulse width ($\overline{G}$ low)	t_{BLEH} t_{BLWH}	8	—	10	—	15	—	ns	
Data valid to end of write	t_{DVBH}	5	—	6	—	10	—	ns	
Data hold time	t_{BHDX}	0	—	0	—	0	—	ns	
Write recovery time	t_{BHAX}	8	—	10	—	12	—	ns	

NOTES:

1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Due to product sensitivities to noise, power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles.
3. If $\overline{G}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
4. After $\overline{W}$, $\overline{E}$, or $\overline{UB}$/$\overline{LB}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns.
5. If both byte control signals are asserted, the two signals must have no more than 2 ns skew between them.
6. All write cycle timings are referenced from the last valid address to the first transition address.

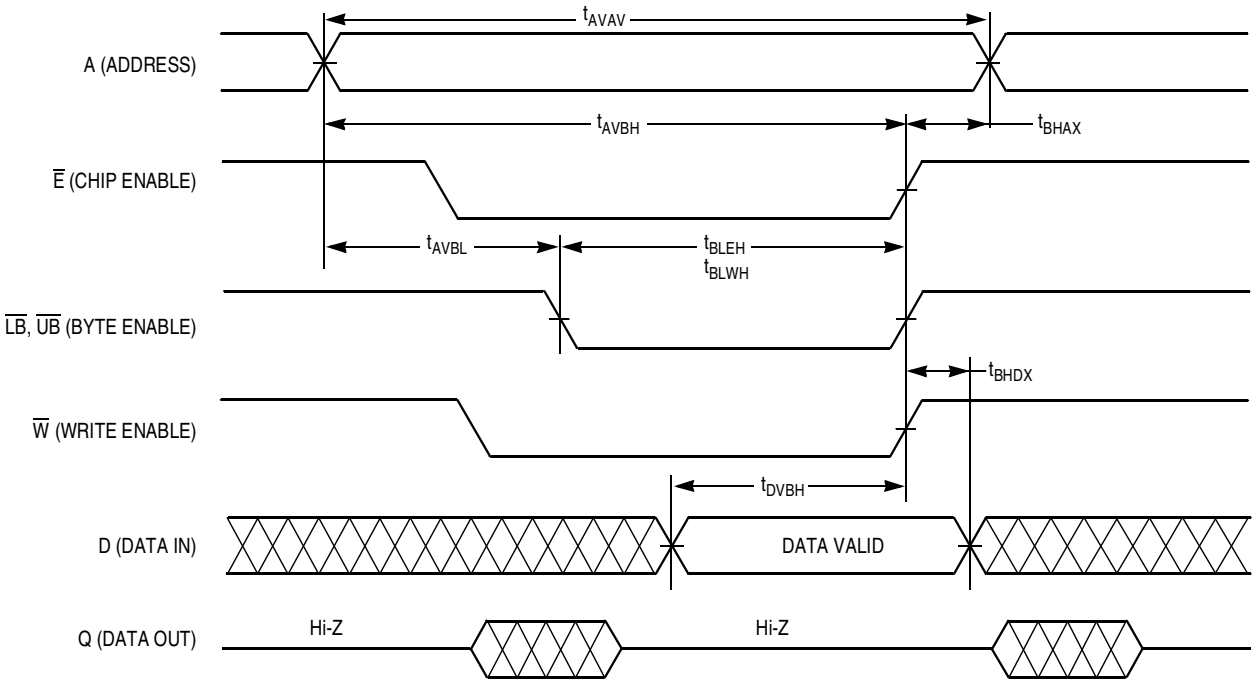


Figure 8. Write Cycle 3 ($\overline{LB}$/$\overline{UB}$ Controlled)

Ordering Information

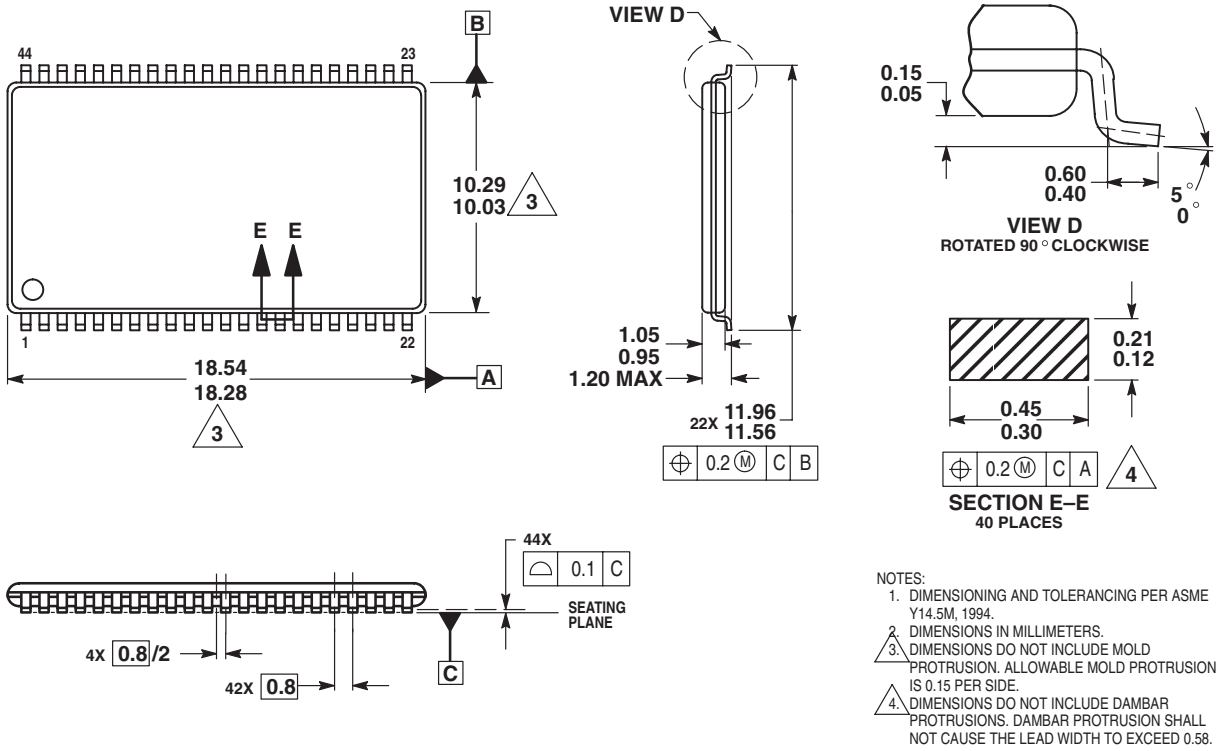
(Order by Full Part Number)

MR 2 A 16 A TS 25 C

- Freescale MRAM Memory Prefix — MR
- Density Code (2 = 4 Mb, 4 = 16 Mb) — 2
- Memory Type (A = Asynch, S = Sync) — A
- I/O Configuration (08 = 8 bits, 16 = 16 bits) — 16
- Revision (A = rev 1) — A
- Package Type (TS = TSOP) — TS
- Timing Set — 25
- Operating Temperature Range (C = 0° C to 70° C) — C

Commercial Device Numbers — MR2A16ATS25C
MR2A16ATS35C

TS Package (44-Lead, TSOP Type II, Case 924A-02)



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