



FSA2567 — Low-Power, Dual SIM Card Analog Switch

Features

- Low On Capacitance for Data Path: 10pF Typical
- Low On Resistance for Data Path: 6Ω Typical
- Low On Resistance for Supply Path: 0.4Ω Typical
- Wide V_{CC} Operating Range: 1.65V to 4.3V
- Low Power Consumption: 1μA Maximum
 - 15μA Maximum I_{CC}T Over Expanded Voltage Range (V_{IN}=1.8V, V_{CC}=4.3V)
- Wide -3db Bandwidth: > 160MHz
- Packaged in:
 - Pb-free 16-Lead MLP & 16-Lead UMLP
- 3kV ESD Rating, >12kV Power/GND ESD Rating

Applications

- Cell phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-Top Box

Description

The FSA2567 is a bi-directional, low-power, dual double-pole, double-throw (4PDT) analog switch targeted at dual SIM card multiplexing. It is optimized for switching the WLAN-SIM data and control signals and dedicates one channel as a supply-source switch.

The FSA2567 is compatible with the requirements of SIM cards and features a low on capacitance (C_{ON}) of 10pF to ensure high-speed data transfer. The V_{SIM} switch path has a low R_{ON} characteristic to ensure minimal voltage drop in the dual SIM card supply paths.

The FSA2567 contains special circuitry that minimizes current consumption when the control voltage applied to the SEL pin is lower than the supply voltage (V_{CC}). This feature is especially valuable in ultra-portable applications, such as cell phones; allowing direct interface with the general-purpose I/Os of the baseband processor. Other applications include switching and connector sharing in portable cell phones, PDAs, digital cameras, printers, and notebook computers.

IMPORTANT NOTE:

For additional information, please contact analogswitch@fairchildsemi.com.

Ordering Information

Part Number	Top Mark	Operating Temperature Range	Eco Status	Package
FSA2567MPX	FSA2567	-40 to +85°C	Green	16-Lead, Molded Leadless Package (MLP) Quad, JEDEC MO-220, 3mm Square
FSA2567UMX	GX	-40 to +85°C	Green	16-Lead, Quad, Ultrathin Molded Leadless Package (UMLP), 1.8 x 2.6mm

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

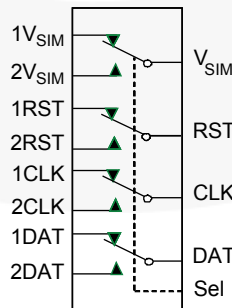


Figure 1. Analog Symbol

Pin Assignments

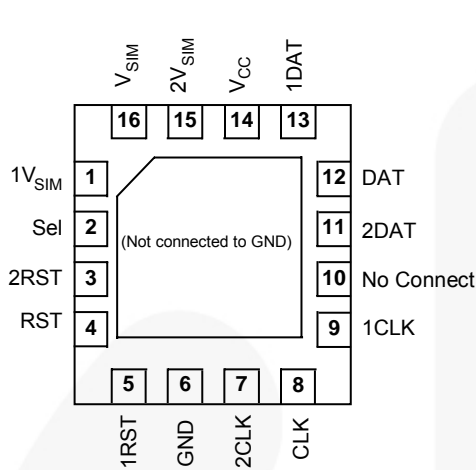


Figure 2. Pad Assignment MLP16 (Top Through View)

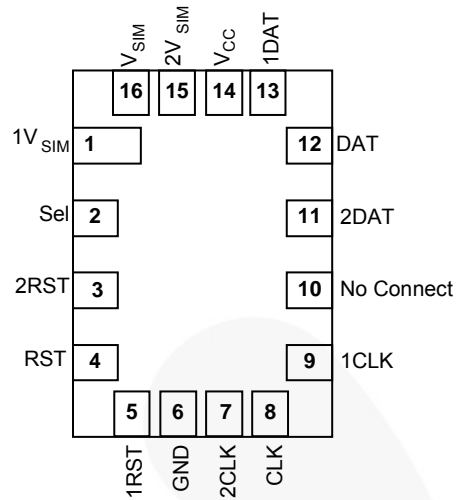


Figure 3. Pad Assignment UMLP16 (Top Through View)

Pin Definitions

Pin	Description
nDAT, nRST, nCLK	Multiplexed Data Source Inputs
nV _{SIM}	Multiplexed SIM Supply Inputs
V _{SIM} , DAT, RST, CLK	Common SIM Ports
Sel	Switch Select

Truth Table

Sel	Function
Logic LOW	1DAT = DAT, 1RST = RST, 1CLK = CLK, 1V _{SIM} = V _{SIM}
Logic HIGH	2DAT = DAT, 2RST = RST, 2CLK = CLK, 2V _{SIM} = V _{SIM}

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	-0.5	+5.5	V
V_{CNTRL}	DC Input Voltage (Sel) ⁽¹⁾	-0.5	V_{CC}	V
V_{SW}	DC Switch I/O Voltage ⁽¹⁾	-0.5	$V_{CC} + 0.3$	V
I_{IK}	DC Input Diode Current	-50		mA
I_{SIM}	DC Output Current - V_{SIM}		350	mA
I_{OUT}	DC Output Current – DAT, CLK, RST		35	mA
T_{STG}	Storage Temperature	-65	+150	°C
ESD	Human Body Model, JEDEC: JESD22-A114	All Pins	3	kV
		I/O to GND	12	
	Charged Device Model, JEDEC: JESD22-C101			

Note:

- The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	1.65	4.30	V
V_{CNTRL}	Control Input Voltage (Sel) ⁽²⁾	0	V_{CC}	V
V_{SW}	Switch I/O Voltage	-0.5	V_{CC}	V
I_{SIM}	DC Output Current - V_{SIM}		150	mA
I_{OUT}	DC Output Current – DAT, CLK, RST		25	mA
T_A	Operating Temperature	-40	+85	°C

Note:

- The control input must be held HIGH or LOW; it must not float.

DC Electrical Characteristics

All typical values are at 25°C, 3.3V V_{CC} unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$			Units
				Min.	Typ.	Max.	
V_{IK}	Clamp Diode Voltage	$I_{IN} = -18\text{mA}$	2.7			-1.2	V
V_{IH}	Input Voltage High		1.65 to 2.3	1.1			V
			2.7 to 3.6	1.3			
			4.3	1.7			
V_{IL}	Input Voltage Low		1.65 to 2.3			0.4	V
			2.7 to 3.6			0.5	
			4.3			0.7	
I_{IN}	Control Input Leakage	$V_{SW} = 0 \text{ to } V_{CC}$	4.3	-1		1	μA
$I_{nc(off)}$, $I_{no(off)}$	Off State Leakage	$nRST, nDAT, nCLK, nV_{SIM} = 0.3\text{V}$ or 3.6V Figure 10	4.3	-60		60	nA
R_{OND}	Data Path Switch On Resistance ⁽³⁾	$V_{SW} = 0, 1.8\text{V}, I_{ON} = -20\text{mA}$ Figure 9	1.8		7.0	12.0	Ω
		$V_{SW} = 0, 2.3\text{V}, I_{ON} = -20\text{mA}$ Figure 9	2.7		6.0	10.0	
R_{ONV}	V_{SIM} Switch On Resistance ⁽³⁾	$V_{SW} = 0, 1.8\text{V}, I_{ON} = -100\text{mA}$ Figure 9	1.8		0.5	0.7	Ω
		$V_{SW} = 0, 2.3\text{V}, I_{ON} = -100\text{mA}$ Figure 9	2.7		0.4	0.6	
ΔR_{OND}	Data Path Delta On Resistance ⁽⁴⁾	$V_{SW} = 0\text{V}, I_{ON} = -20\text{mA}$	2.7		0.2		Ω
I_{CC}	Quiescent Supply Current	$V_{CNTRL} = 0 \text{ or } V_{CC}, I_{OUT} = 0$	4.3			1.0	μA
I_{CCT}	Increase in I_{CC} Current Per Control Voltage and V_{CC}	$V_{CNTRL} = 2.6\text{V}, V_{CC} = 4.3\text{V}$	4.3		5.0	10.0	μA
		$V_{CNTRL} = 1.8\text{V}, V_{CC} = 4.3\text{V}$	4.3		7.0	15.0	μA

Notes:

3. Measured by the voltage drop between nDAT, nRST, nCLK and relative common port pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the relative ports.
4. Guaranteed by characterization.

AC Electrical Characteristics

All typical value are for $V_{CC}=3.3V$ at $25^{\circ}C$ unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A=-40^{\circ}C$ to $+85^{\circ}C$			Units
				Min.	Typ.	Max.	
t_{OND}	Turn-On Time Sel to Output (DAT,CLK,RST)	$R_L = 50\Omega, C_L = 35pF$ $V_{SW} = 1.5V$ Figure 11, Figure 12	$1.8^{(5)}$		65	95	ns
			2.7 to 3.6		42	60	ns
t_{OFFD}	Turn-Off Time Sel to Output (DAT,CLK,RST)	$R_L = 50\Omega, C_L = 35pF$ $V_{SW} = 1.5V$ Figure 11, Figure 12	$1.8^{(5)}$		30	50	ns
			2.7 to 3.6		20	40	ns
t_{ONV}	Turn-On Time Sel to Output (V_{SIM})	$R_L = 50\Omega, C_L = 35pF$ $V_{SW} = 1.5V$ Figure 11, Figure 12	$1.8^{(5)}$		55	80	ns
			2.7 to 3.6		35	55	ns
t_{OFFV}	Turn-Off Time Sel to Output (V_{SIM})	$R_L = 50\Omega, C_L = 35pF$ $V_{SW} = 1.5V$ Figure 11, Figure 12	$1.8^{(5)}$		35	50	
			2.7 to 3.6		22	40	ns
t_{PD}	Propagation Delay ⁽⁵⁾ (DAT,CLK,RST)	$C_L = 35 pF, R_L = 50\Omega$ Figure 11, Figure 13	3.3		0.25		ns
t_{BBMD}	Break-Before-Make ⁽⁵⁾ (DAT,CLK,RST)	$R_L = 50\Omega, C_L = 35pF$ $V_{SW1} = V_{SW2} = 1.5V$ Figure 15	2.7 to 3.6	3	18		ns
t_{BBMV}	Break-Before-Make ⁽⁵⁾ (V_{SIM})	$R_L = 50\Omega, C_L = 35pF$ $V_{SW1} = V_{SW2} = 1.5V$ Figure 15	2.7 to 3.6	3	12		ns
Q	Charge Injection (DAT,CLK,RST)	$C_L = 50pF, R_{GEN} = 0\Omega,$ $V_{GEN} = 0V$	2.7 to 3.6		10		pC
O_{IRR}	Off Isolation (DAT,CLK,RST)	$R_L = 50\Omega, f = 10MHz$ Figure 17	2.7 to 3.6		-60		dB
Xtalk	Non-Adjacent Channel Crosstalk (DAT,CLK,RST)	$R_L = 50\Omega, f = 10MHz$ Figure 18	2.7 to 3.6		-60		dB
BW	-3db Bandwidth (DAT,CLK,RST)	$R_L = 50\Omega, C_L = 5pF$ Figure 16	2.7 to 3.6		475		MHz

Note:

- Guaranteed by characterization.

Capacitance

Symbol	Parameter	Conditions	T _A = -40°C to +85°C			Units
			Min.	Typ.	Max.	
C _{IN}	Control Pin Input Capacitance	V _{CC} = 0V		1.5		pF
C _{OND}	RST, CLK, DAT On Capacitance ⁽⁶⁾	V _{CC} = 3.3V, f = 1MHz Figure 20		10	12	
C _{ONV}	V _{SIM} On Capacitance ⁽⁶⁾	V _{CC} = 3.3V, f = 1MHz Figure 20		110	150	
C _{OFFD}	RST, CLK, DAT Off Capacitance	V _{CC} = 3.3V Figure 19		3		
C _{OFFV}	V _{SIM} Off Capacitance	V _{CC} = 3.3V Figure 19		40		

Note:

6. Guaranteed by characterization.

Typical Performance Characteristics

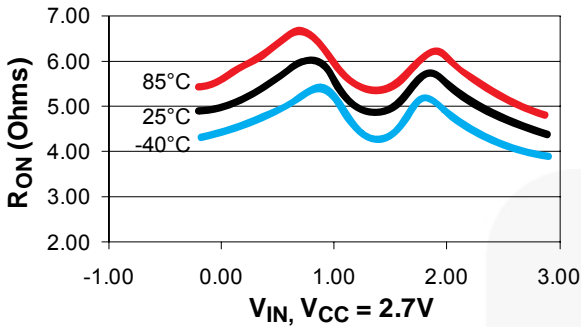


Figure 4. R_{ON} Data Path

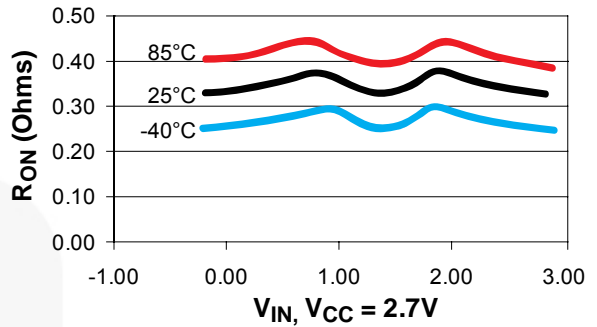


Figure 5. R_{ON} V_{SIM}

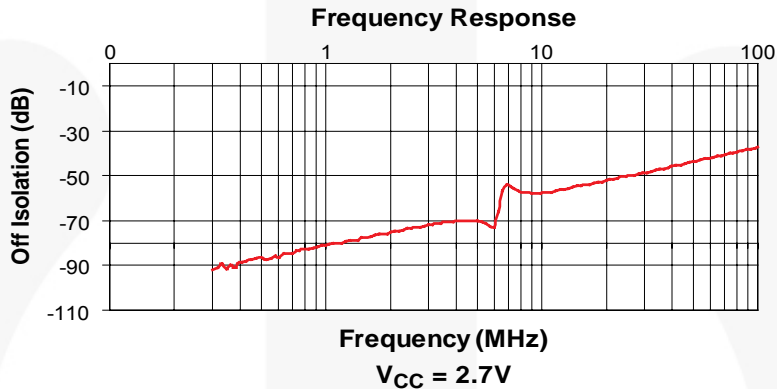


Figure 6. Off Isolation

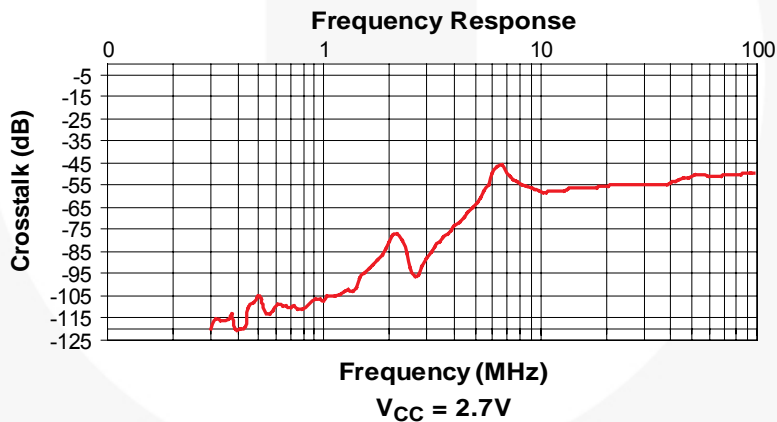


Figure 7. Crosstalk

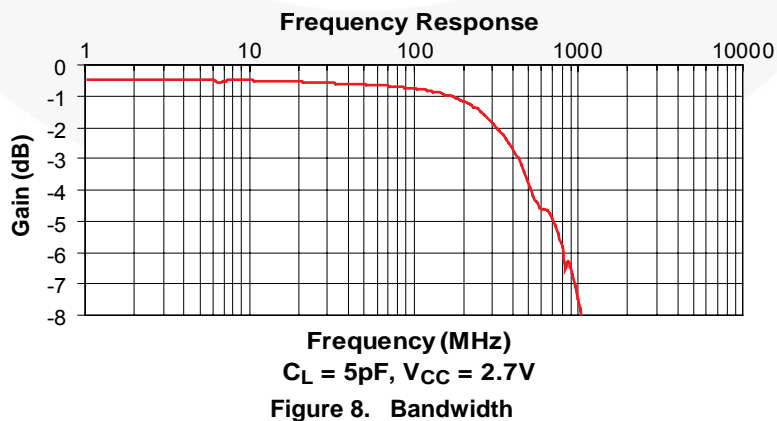


Figure 8. Bandwidth

Test Diagrams

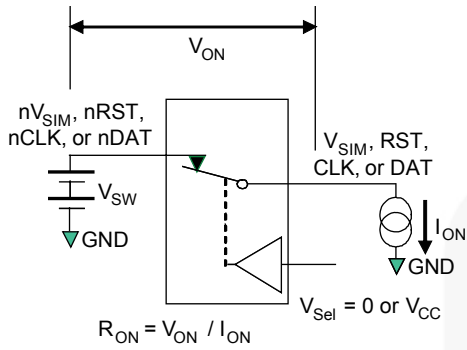


Figure 9. On Resistance

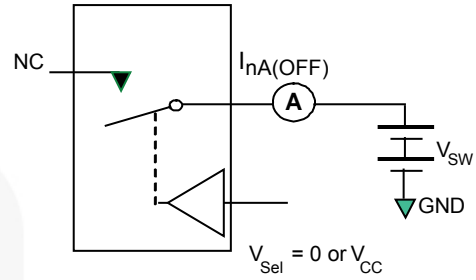
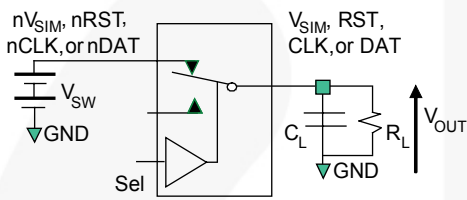


Figure 10. Off Leakage



R_L and C_L are functions of the application environment (see tables for specific values). C_L includes test fixture and stray capacitance.

Figure 11. AC Test Circuit Load

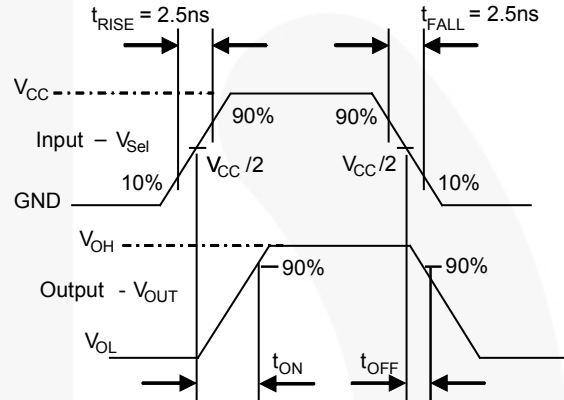


Figure 12. Turn-On / Turn-Off Waveforms

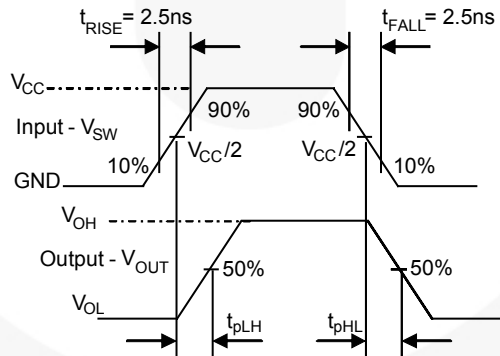


Figure 13. Propagation Delay

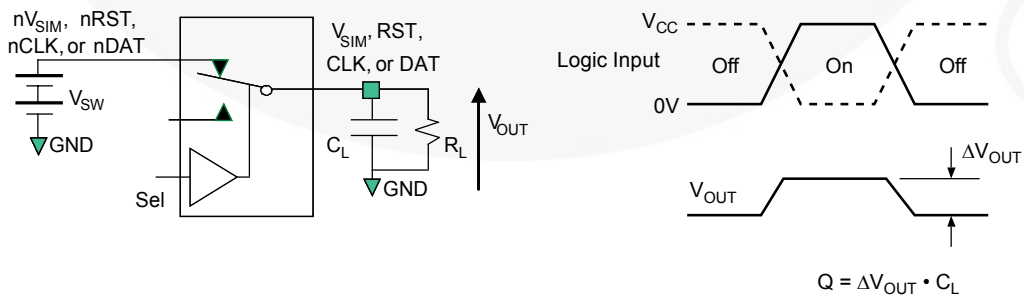
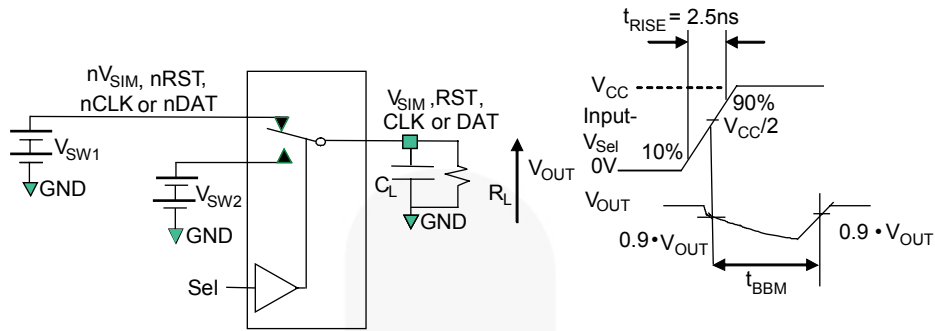


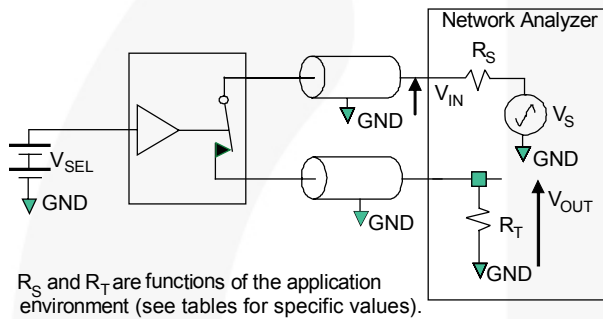
Figure 14. Charge Injection

Test Diagrams (Continued)



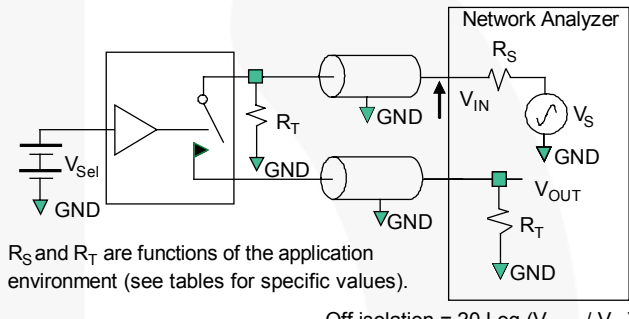
R_L and C_L are functions of the application environment (see tables for specific values).
 C_L includes test fixture and stray capacitance.

Figure 15. Break-Before-Make Interval Timing



R_S and R_T are functions of the application environment (see tables for specific values).

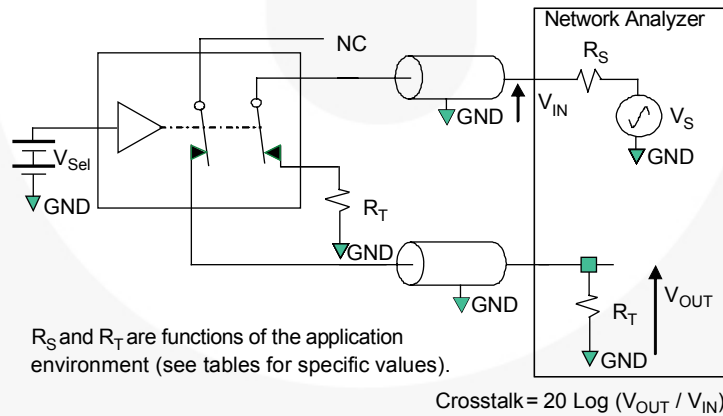
Figure 16. Bandwidth



R_S and R_T are functions of the application environment (see tables for specific values).

$$\text{Off isolation} = 20 \text{ Log } (V_{OUT} / V_{IN})$$

Figure 17. Channel Off Isolation



R_S and R_T are functions of the application environment (see tables for specific values).

$$\text{Crosstalk} = 20 \text{ Log } (V_{OUT} / V_{IN})$$

Figure 18. Non-Adjacent Channel-to-Channel Crosstalk

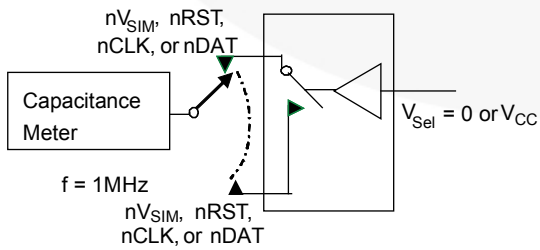


Figure 19. Channel Off Capacitance

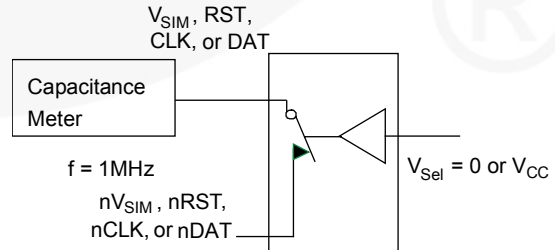
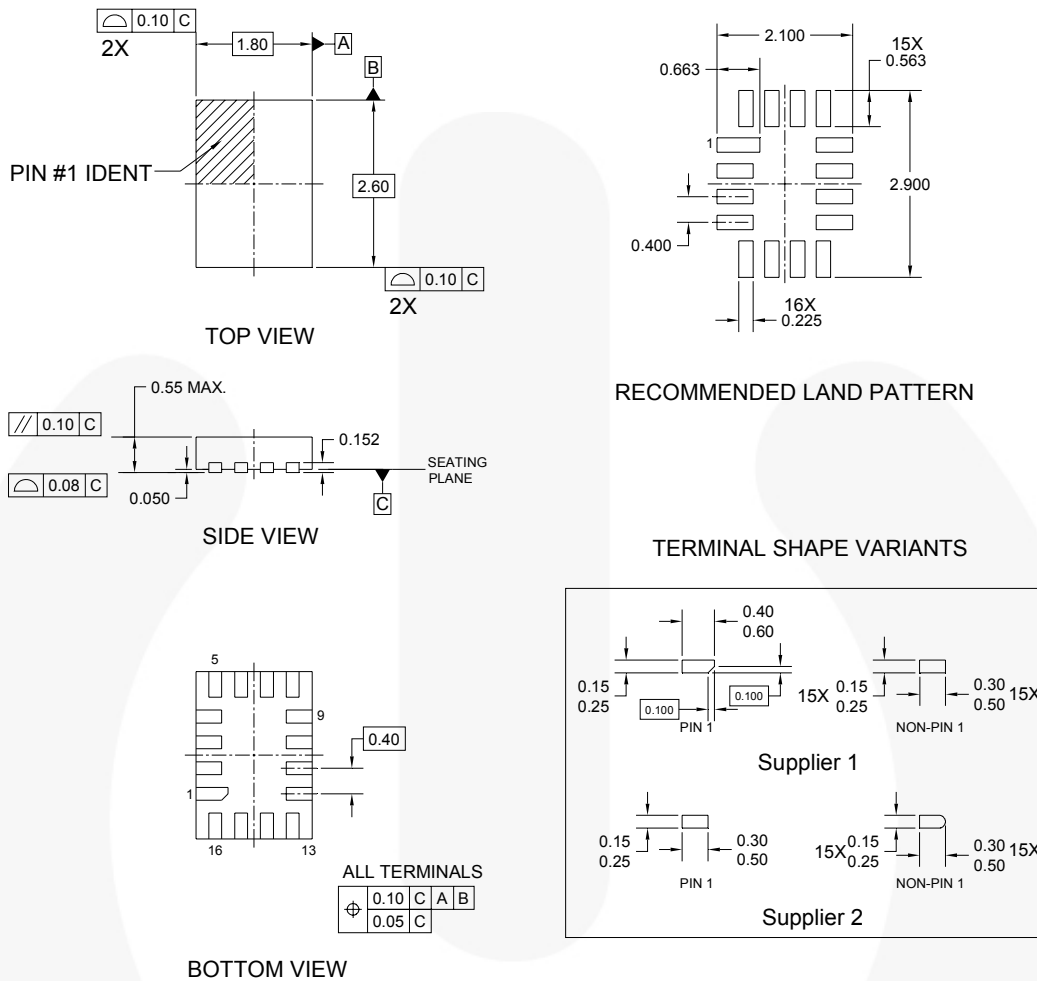


Figure 20. Channel On Capacitance

Physical Dimensions



NOTES:

- A. THIS PACKAGE IS NOT CURRENTLY REGISTERED WITH ANY STANDARDS COMMITTEE
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. TERMINAL SHAPE MAY VARY ACCORDING TO PACKAGE SUPPLIER, SEE TERMINAL SHAPE VARIANTS
- E. LAND PATTERN IS A MINIMAL TOE DESIGN
- F. DRAWING FILE NAME : UMLP16AREV3

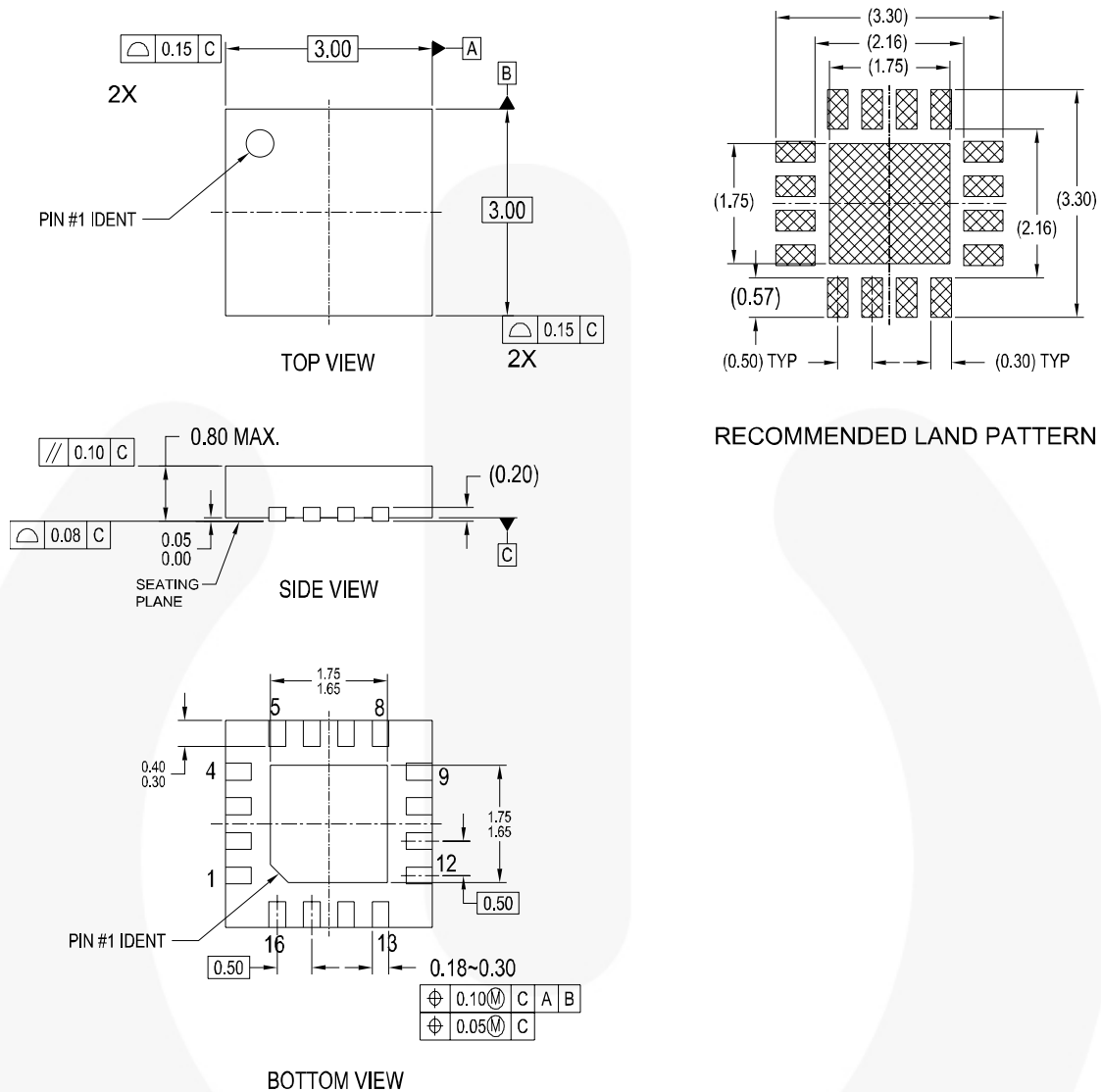
Figure 21. 16-Lead Ultrathin Molded Leadless Package (UMLP)

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Physical Dimensions



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WEED-Pending, DATED pending
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

MLP16BrevB

Figure 22. 16-Terminal Molded Leadless Package (MLP)






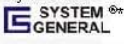
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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Rev. 142