FAIRCHILD SEMICONDUCTOR®

November 1988
Revised February 2005

74AC00 • 74ACT00
Quad 2-Input NAND Gate

General Description

The AC/ACT00 contains four 2-input NAND gates.

Features

- I_{CC} reduced by 50%
- Outputs source/sink 24 mA
- ACT00 has TTL-compatible inputs

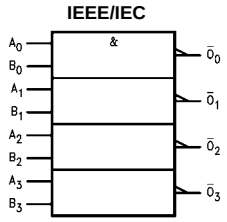
Ordering Code:

Order Number	Package Number	Package Description
74AC00SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74AC00SCX_NL	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74AC00SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC00MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC00PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74AC00PC_NL	N14A	Pb-Free 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT00SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ACT00SCX_NL	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ACT00SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT00MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT00PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

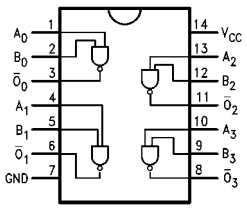
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering form. PC not available in Tape and Reel.
Pb-Free package per JEDEC J-STD-020B.

Note 1: "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Use this number to order device.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
A_n, B_n	Inputs
$\overline{O}_n$	Outputs

FACT™ is a trademark of Fairchild Semiconductor Corporation.

Absolute Maximum Ratings(Note 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source	
or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 2: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	T_A = +25°C Typ	T_A = −40°C to +85°C Guaranteed Limits		Units	Conditions
V_{IH}	Minimum HIGH Level	3.0	1.5	2.1	2.1		V_{OUT} = 0.1V
	Input Voltage	4.5	2.25	3.15	3.15	V	or V_{CC} − 0.1V
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum LOW Level	3.0	1.5	0.9	0.9		V_{OUT} = 0.1V
	Input Voltage	4.5	2.25	1.35	1.35	V	or V_{CC} − 0.1V
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum HIGH Level	3.0	2.99	2.9	2.9		
	Output Voltage	4.5	4.49	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4		
							V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.46		I_{OH} = −12 mA
		4.5		3.86	3.76	V	I_{OH} = −24 mA
		5.5		4.86	4.76		I_{OH} = −24 mA (Note 3)
V_{OL}	Maximum LOW Level	3.0	0.002	0.1	0.1		
	Output Voltage	4.5	0.001	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1		
							V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.44		I_{OL} = 12 mA
		4.5		0.36	0.44	V	I_{OL} = 24 mA
		5.5		0.36	0.44		I_{OL} = 24 mA (Note 3)
I_{IN} (Note 4)	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{OLD}	Minimum Dynamic	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current (Note 5)	5.5			−75	mA	V_{OHD} = 3.85V Min
I_{CC} (Note 4)	Maximum Quiescent Supply Current	5.5		2.0	20.0	μA	V_{IN} = V_{CC} or GND

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

Note 5: Maximum test duration 2.0 ms, one output loaded at a time.

DC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC}	$T_A = +25°C$	$T_A = -40°C$ to $+85°C$		Units	Conditions
		(V)	Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	2.0	2.0		
V_{IL}	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	0.8	0.8		
V_{OH}	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50\ \mu A$
		5.5	5.49	5.4	5.4		
		4.5		3.86	3.76	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24$ mA
		5.5		4.86	4.76		$I_{OH} = -24$ mA (Note 6)
V_{OL}	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		5.5	0.001	0.1	0.1		
		4.5		0.36	0.44	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 24$ mA
		5.5		0.36	0.44		$I_{OL} = 24$ mA (Note 6)
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	Minimum Dynamic Output Current (Note 7)	5.5			75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}		5.5			−75	mA	$V_{OHD} = 3.85V$ Min
I_{CC}	Maximum Quiescent Supply Current	5.5		2.0	20.0	μA	$V_{IN} = V_{CC}$ or GND

Note 6: All outputs loaded; thresholds on input associated with output under test.

Note 7: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V) (Note 8)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	3.3	2.0	7.0	9.5	2.0	10.0	ns
		5.0	1.5	6.0	8.0	1.5	8.5	
t_{PHL}	Propagation Delay	3.3	1.5	5.5	8.0	1.0	8.5	ns
		5.0	1.5	4.5	6.5	1.0	7.0	

Note 8: Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Electrical Characteristics for ACT

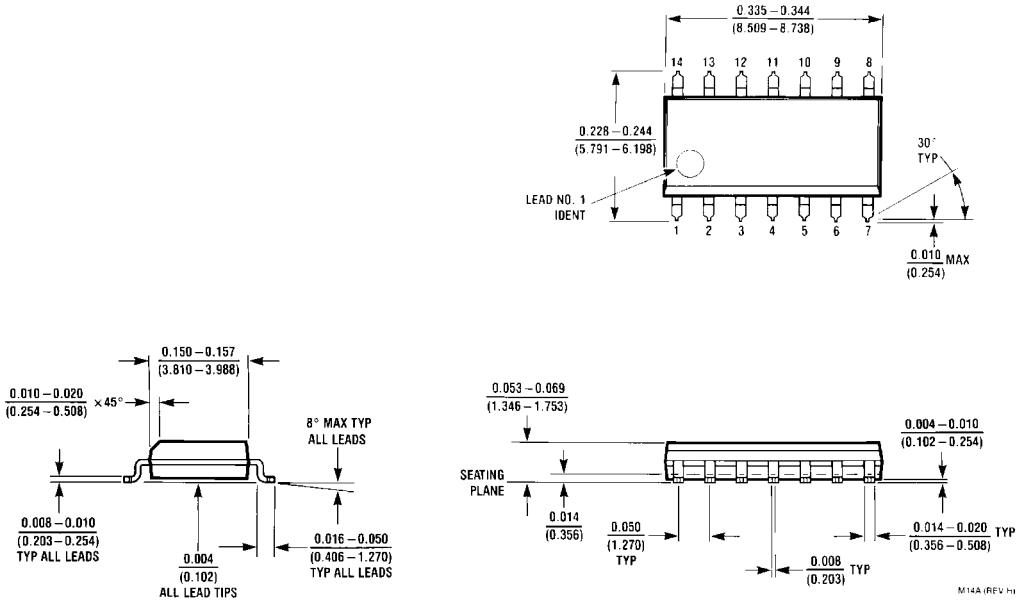
Symbol	Parameter	V_{CC} (V) (Note 9)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	5.0	1.5	5.5	9.0	1.0	9.5	ns
t_{PHL}	Propagation Delay	5.0	1.5	4.0	7.0	1.0	8.0	ns

Note 9: Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

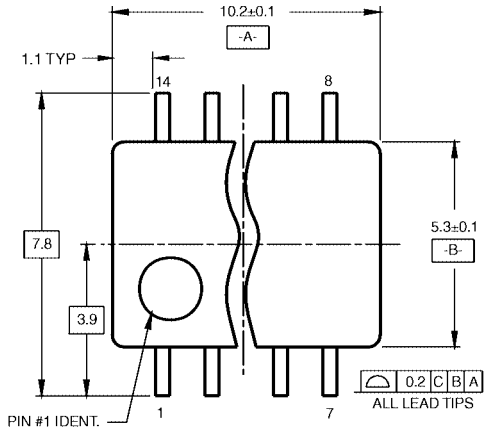
Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = Open
C_{PD}	Power Dissipation Capacitance	30.0	pF	$V_{CC} = 5.0V$

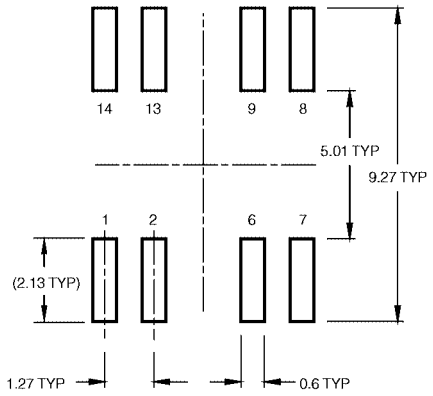
Physical Dimensions inches (millimeters) unless otherwise noted



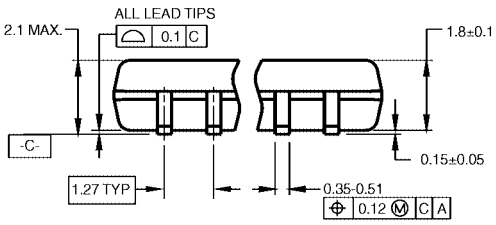
14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

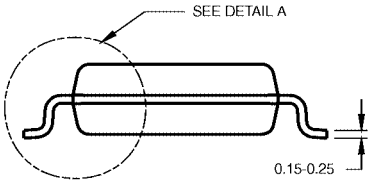
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



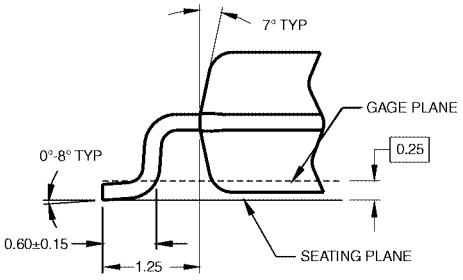


LAND PATTERN RECOMMENDATION





DIMENSIONS ARE IN MILLIMETERS



DETAIL A

NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

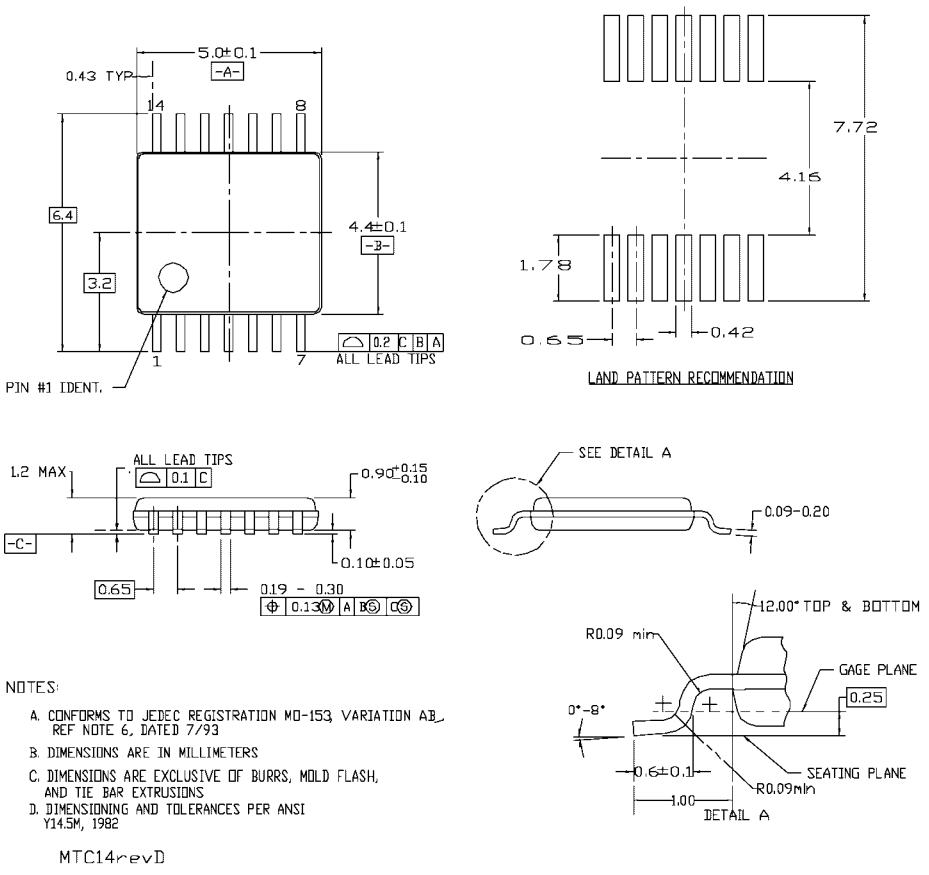
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93

B. DIMENSIONS ARE IN MILLIMETERS

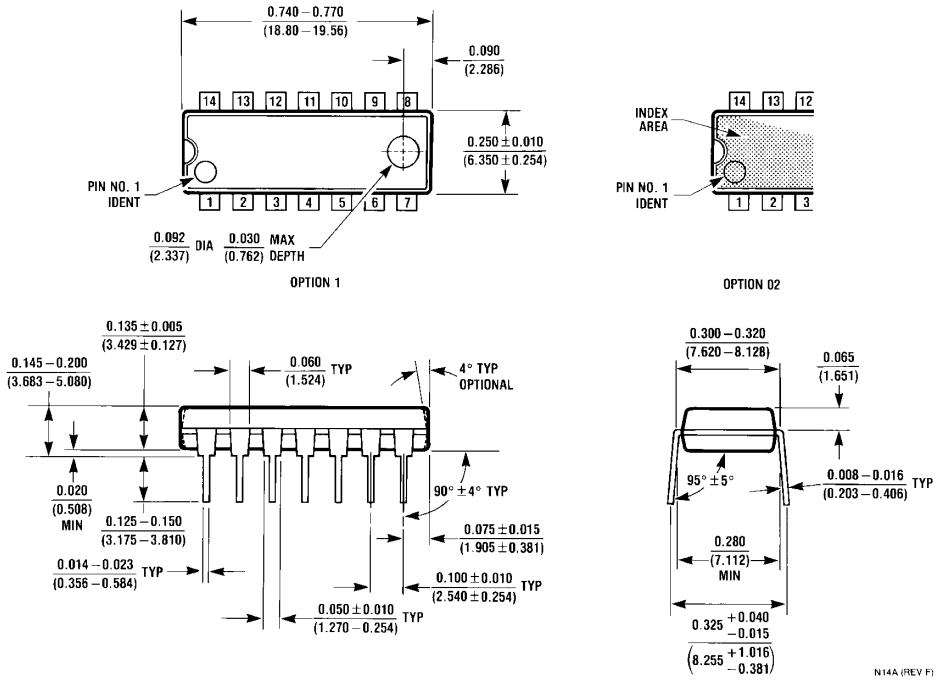
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14revD

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

LIFE SUPPORT POLICY

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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