

256K (32K x 8) Static RAM

Features

- Fast access time: 12 ns, 15 ns, 20 ns and 25 ns
- Wide voltage range: 5.0V $\pm$ 10% (4.5V to 5.5V)
- CMOS for optimum speed/power
- TTL-compatible Inputs and Outputs
- Available in 28 DIP, 28 SOJ, and 28 TSOP I packages
- Available in Pb-free packages
- 2.0V Data Retention
- Low CMOS standby power
- Automated Power-down when deselected

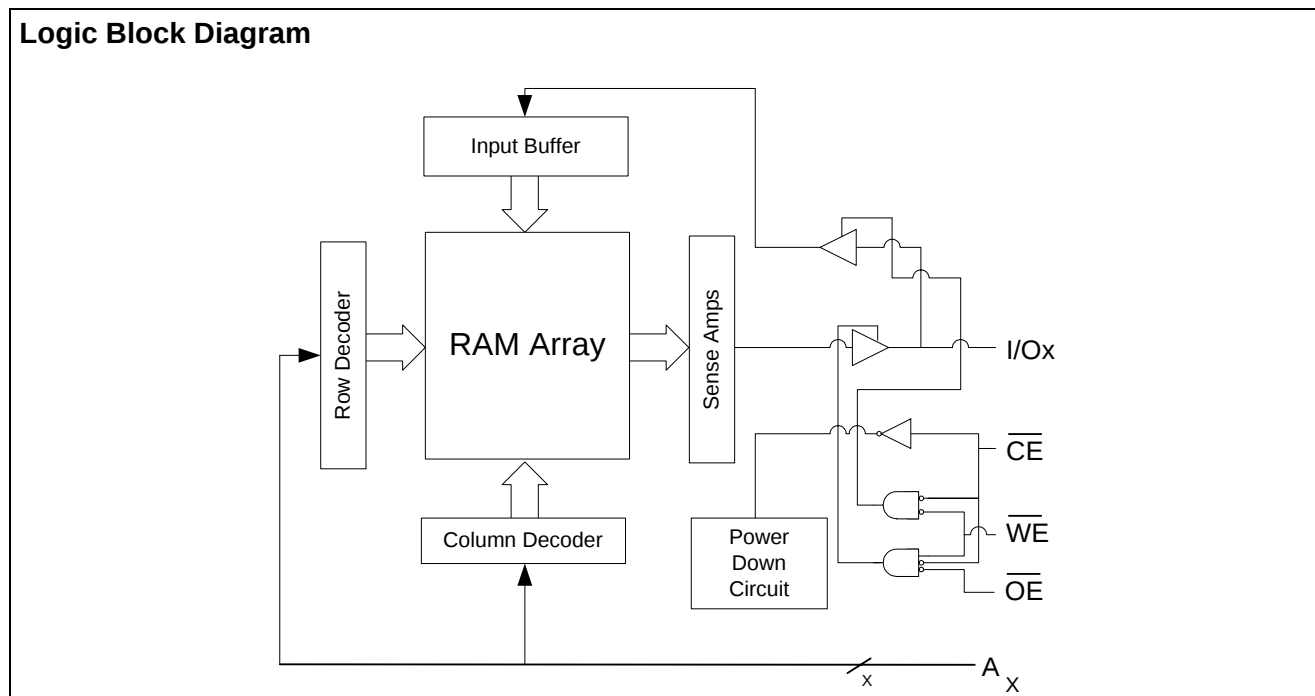
General Description

The CY7C199CN is a high-performance CMOS Asynchronous SRAM organized as 32K by 8 bits that supports an asynchronous memory interface. The device features an automatic power-down feature that significantly reduces power consumption when deselected.

See the Truth Table in this data sheet for a complete description of read and write modes.

The CY7C199CN is available in 28 DIP, 28 SOJ and 28 TSOP I package(s).

Logic Block Diagram



Product Portfolio

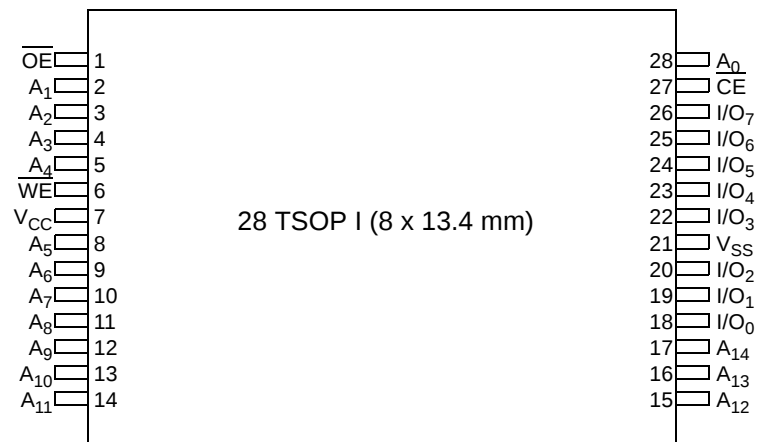
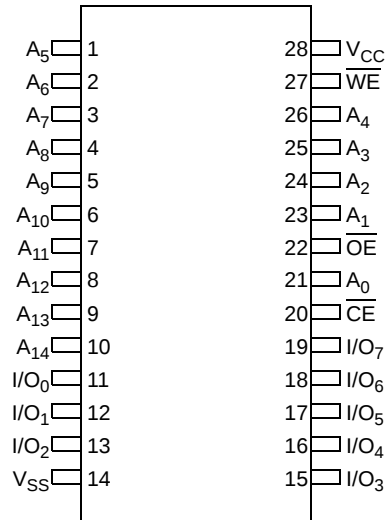
	-12	-15	-20	-25	Unit
Maximum Access Time	12	15	20	25	ns
Maximum Operating Current	85	80	75	75	mA
Maximum CMOS Standby Current (low power)	500	500	500	500	μ A

Note:

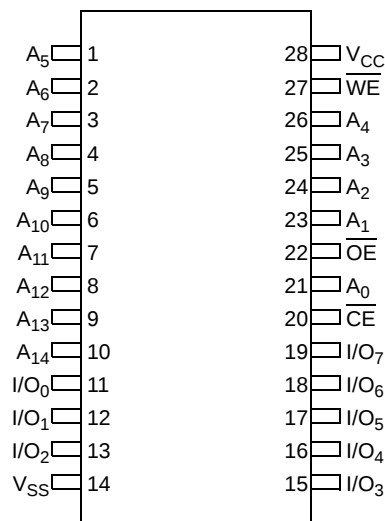
1. For best-practices recommendations, please refer to the Cypress application note *System Design Guidelines* on www.cypress.com.

Pin Layout and Specifications

28 DIP (6.9 x 35.6 x 3.5 mm)



28 SOJ



Pin Description

Pin	Type	Description	DIP	SOJ	TSOP I
A _X	Input	Address Inputs	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 21, 23, 24, 25, 26	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 21, 23, 24, 25, 26	2, 3, 4, 5, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 28
CE	Control	Chip Enable	20	20	27
I/O _X	Input or Output	Data Input/Outputs	11, 12, 13, 15, 16, 17, 18, 19	11, 12, 13, 15, 16, 17, 18, 19	18, 19, 20, 22, 23, 24, 25, 26
OE	Control	Output Enable	22	22	1
V _{CC}	Supply	Power (5.0V)	28	28	7
V _{SS}	Supply	Ground	14	14	21
WE	Control	Write Enable	27	27	6

Truth Table

CE	OE	WE	I/O _x	Mode	Power
H	X	X	High Z	Deselect / Power- Down	Stand by (I _{SB})
L	L	H	Data out	Read	Active (I _{CC})
L	X	L	Data In	Write	Active (I _{CC})
L	H	H	High Z	Selected, outputs disabled	Active (I _{CC})

Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested.)

Parameter	Description	Value	Unit
T _{STG}	Storage Temperature	-65 to +150	°C
T _{AMB}	Ambient Temperature with Power Applied (i.e., case temperature)	-55 to +125	°C
V _{CC}	Core Supply Voltage Relative to V _{SS}	-0.5 to +7.0	V
V _{IN} , V _{OUT}	DC Voltage Applied to any Pin Relative to V _{SS}	-0.5 to V _{CC} + 0.5	V
I _{OUT}	Output Short-Circuit Current	20	mA
V _{ESD}	Static Discharge Voltage (per MIL-STD-883, Method 3015)	> 2001	V
I _{LU}	Latch-up Current	> 200	mA

Operating Range

Range	Ambient Temperature (T _A)	Voltage Range (V _{CC})
Commercial	0°C to 70°C	5.0V ± 10%
Industrial	-40°C to 85°C	5.0V ± 10%

DC Electrical Characteristics Over the Operating Range (-12, -15)^[2]

Parameter	Description	Condition	Power	-12		-15		Unit
				Min.	Max.	Min.	Max.	
V _{IH}	Input HIGH Voltage		–	2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage		–	-0.5	0.8	-0.5	0.8	V
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	–	2.4	–	2.4	–	V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA	–	–	0.4	–	0.4	V
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = F _{MAX} = 1/t _{RC}	–	–	85	–	80	mA
I _{SB1}	Automatic $\overline{\text{CE}}$ Power-down Current TTL Inputs	Max. V _{CC} , $\overline{\text{CE}} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = F _{MAX}	–	–	30	–	30	mA
			L	–	10	–	10	mA
I _{SB2}	Automatic $\overline{\text{CE}}$ Power-down Current CMOS Inputs	Max. V _{CC} , $\overline{\text{CE}} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0	–	–	10	–	10	mA
			L	–	500	–	500	μA
I _{OZ}	Output Leakage Current	GND ≤ V _i ≤ V _{CC} , Output Disabled	–	-5	+5	-5	+5	μA
I _{IX}	Input Load Current	GND ≤ V _i ≤ V _{CC}	–	-5	+5	-5	+5	μA

DC Electrical Characteristics Over the Operating Range (-20, -25)^[2]

Parameter	Description	Condition	Power	-20 ns		-25 ns		Unit
				Min.	Max.	Min.	Max.	
V _{IH}	Input HIGH Voltage		–	2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage		–	-0.5	0.8	-0.5	0.8	V
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	–	2.4	–	2.4	–	V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA	–	–	0.4	–	0.4	V
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = F _{MAX} = 1/t _{RC}	–	–	75	–	75	mA
I _{SB1}	Automatic $\overline{\text{CE}}$ Power-down Current TTL Inputs	Max. V _{CC} , $\overline{\text{CE}} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = F _{MAX}	–	–	30	–	30	mA
			L	–	10	–	10	mA
I _{SB2}	Automatic $\overline{\text{CE}}$ Power-down Current CMOS Inputs	Max. V _{CC} , $\overline{\text{CE}} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0	–	–	10	–	10	mA
			L	–	500	–	500	μA

Note:

2. V_{IL} (min) = -2.0V for pulse durations of less than 20 ns.

DC Electrical Characteristics Over the Operating Range $(-20, -25)^{[2]}$ (continued)

Parameter	Description	Condition	Power	-20 ns		-25 ns		Unit
				Min.	Max.	Min.	Max.	
I_{OZ}	Output Leakage Current	$GND \leq V_i \leq V_{CC}$, Output Disabled	—	-5	+5	-5	+5	μA
I_{IX}	Input Load Current	$GND \leq V_i \leq V_{CC}$	—	-5	+5	-5	+5	μA

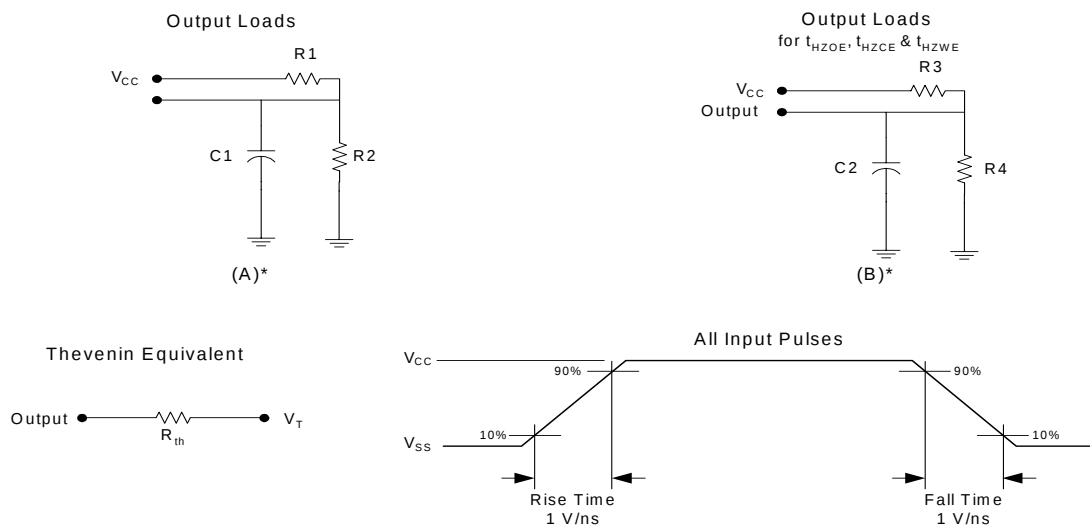
Capacitance^[3]

Parameter	Description	Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ C$, $f = 1 \text{ MHz}$, $V_{CC} = 5.0V$	8	pF
C_{OUT}	Output Capacitance		8	

Thermal Resistance^[4]

Parameter	Description	Conditions	TSOP I	SOJ	DIP	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 square inch, two-layer printed circuit board	88.6	79	69.33	$^\circ C/W$
Θ_{JC}	Thermal Resistance (Junction to Case)		21.94	41.42	31.62	

AC Test Loads



* including scope and jig capacitance

AC Test Conditions

Parameter	Description	Nom.	Unit
C1	Capacitor 1	30	pF
C2	Capacitor 2	5	
R1	Resistor 1	480	Ω
R2	Resistor 2	255	
R3	Resistor 3	480	
R4	Resistor 4	255	
R_{TH}	Resistor Thevenin	167	
V_{TH}	Voltage Thevenin	1.73	V

Note:

3. Tested initially and after any design or process change that may affect these parameters.

AC Electrical Characteristics^[5, 6, 7]

Parameter	Description	-12		-15		-20		-25		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	12	–	15	–	20	–	25	–	ns
t_{AA}	Address to Data Valid	–	12	–	15	–	20	–	25	ns
t_{OHA}	Data Hold from Address Change	3	–	3	–	3	–	3	–	ns
t_{ACE}	$\overline{CE}$ to Data Valid	–	12	–	15	–	20	–	25	ns
t_{DOE}	$\overline{OE}$ to Data Valid	–	5	–	7	–	9	–	9	ns
t_{LZOE}	$\overline{OE}$ to Low Z	0	–	0	–	0	–	0	–	ns
t_{HZOE}	$\overline{OE}$ to High Z	–	5	–	7	–	9	–	9	ns
t_{LZCE}	$\overline{CE}$ to Low Z	3	–	3	–	3	–	3	–	ns
t_{HZCE}	$\overline{CE}$ to High Z	–	5	–	7	–	9	–	9	ns
t_{PU}	$\overline{CE}$ to Power-up	0	–	0	–	0	–	0	–	ns
t_{PD}	$\overline{CE}$ to Power-down	–	12	–	15	–	20	–	20	ns
t_{WC}	Write Cycle Time	12	–	15	–	20	–	25	–	ns
t_{SCE}	$\overline{CE}$ to Write End	9	–	10	–	15	–	15	–	ns
t_{AW}	Address Set-up to Write End	9	–	10	–	15	–	15	–	ns
t_{HA}	Address Hold from Write End	0	–	0	–	0	–	0	–	ns
t_{SA}	Address Set-up to Write Start	0	–	0	–	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ Pulse Width	8	–	9	–	15	–	15	–	ns
t_{SD}	Data Set-up to Write End	8	–	9	–	10	–	10	–	ns
t_{HD}	Data Hold from Write End	0	–	0	–	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z	–	7	–	7	–	10	–	10	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3	–	3	–	3	–	3	–	ns

Data Retention Characteristics^[8]

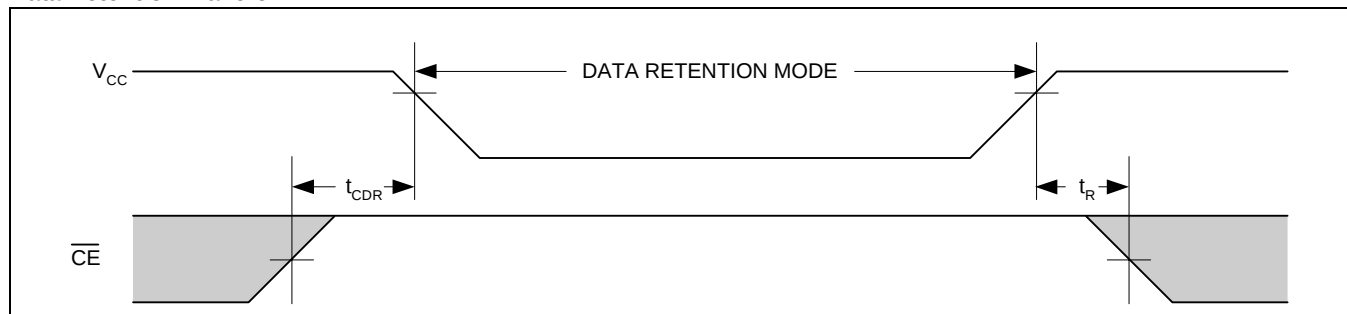
Parameter	Description	Condition	Min	Max	Unit
V_{DR}	V_{CC} for Data Retention		2.0	–	V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V, \overline{CE} \geq V_{CC} - 0.3V,$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	–	150	μA
t_{CDR}	Chip Deselect to Data Retention Time		0	–	ns
t_R	Operation Recovery Time		200	–	μs

Notes:

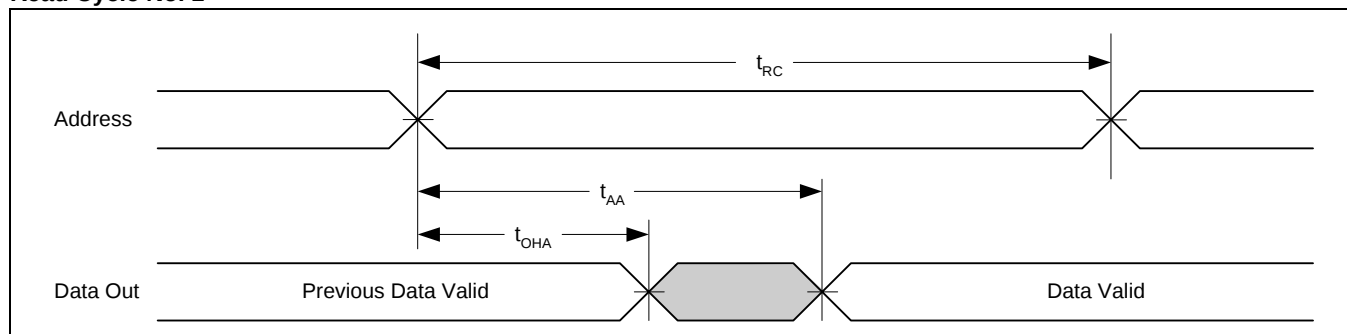
- Test Conditions assume a transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- t_{HZOE} , t_{HZCE} , t_{HZWE} are specified as in part (b) of the A/C Test Loads. Transitions are measured ± 200 mV from steady state voltage.
- L-version only.

Timing Waveforms

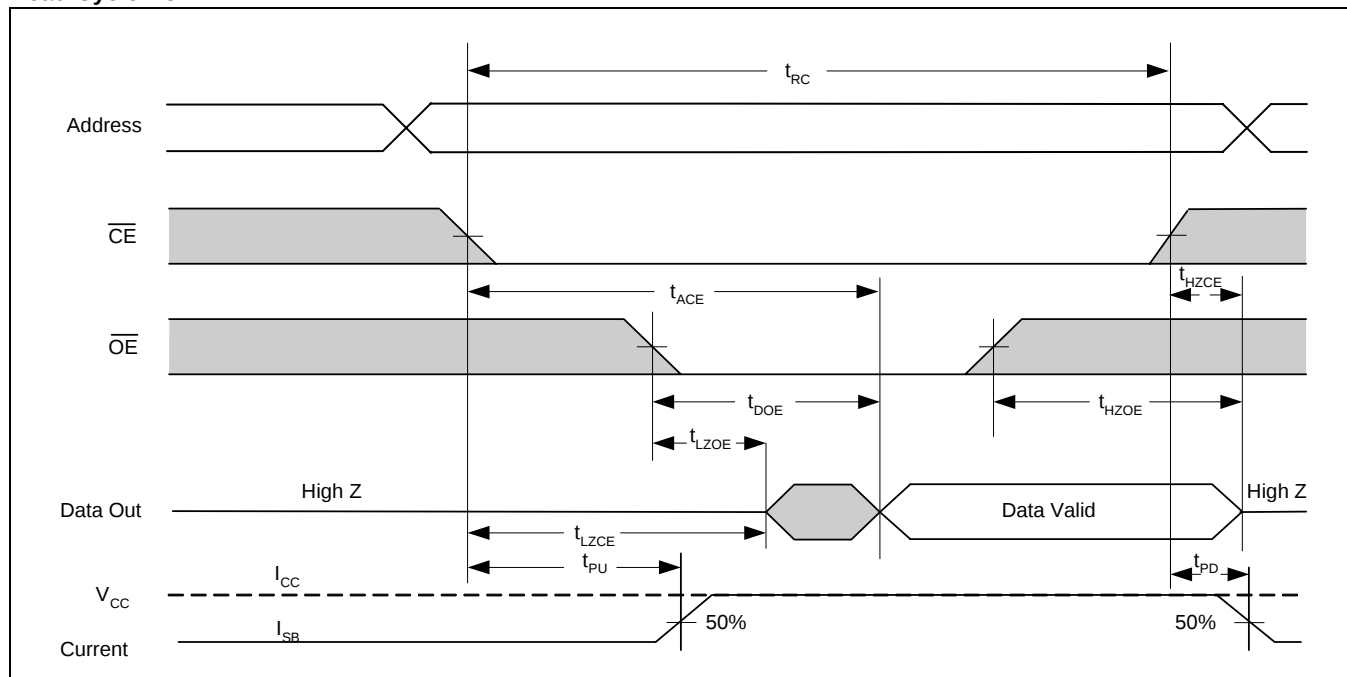
Data Retention Waveform



Read Cycle No. 1^[9, 10]



Read Cycle No. 2^[11, 12]

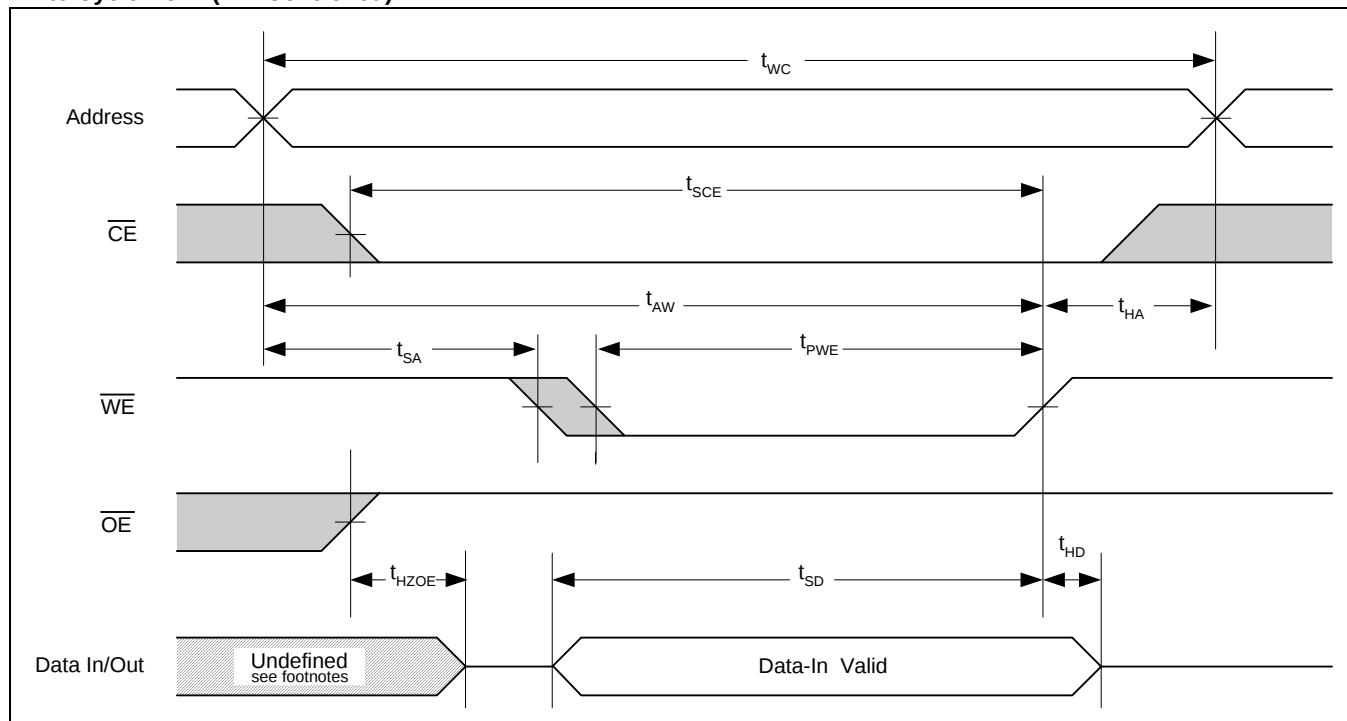


Notes:

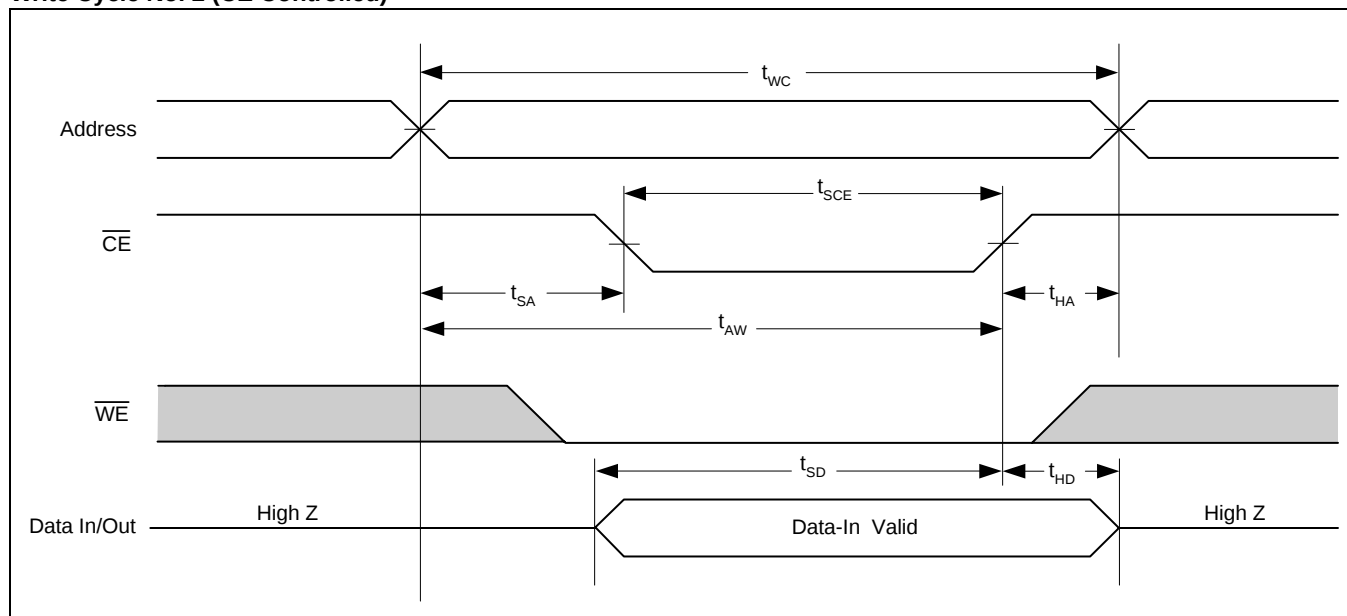
9. Device is continuously selected. $\overline{OE} = V_{IL} = \overline{CE}$.
10. $\overline{WE}$ is HIGH for Read Cycle.
11. This cycle is $\overline{OE}$ Controlled and $\overline{WE}$ is HIGH read cycle.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Timing Waveforms (continued)

Write Cycle No. 1 ($\overline{WE}$ Controlled)^[13, 14, 15]



Write Cycle No. 2 ($\overline{CE}$ Controlled)^[14, 16, 17]

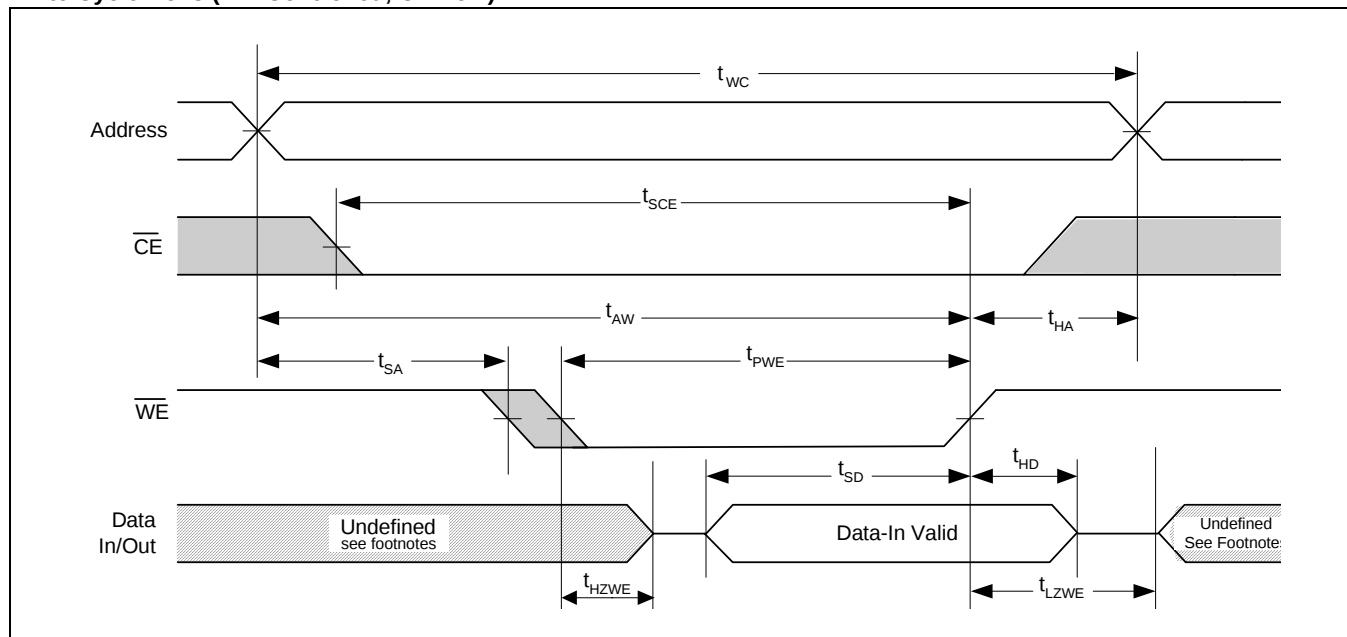


Notes:

13. This cycle is $\overline{WE}$ controlled, $\overline{OE}$ is HIGH during write.
14. Data In/Out is high impedance if $\overline{OE} = V_{IH}$.
15. During this period the I/Os are in output state and input signals should not be applied.
16. This cycle is $\overline{CE}$ controlled.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Timing Waveforms (continued)

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ Low)^[18]



Note:

18. The cycle is $\overline{WE}$ controlled, $\overline{OE}$ LOW. The minimum write cycle time is the sum of t_{HZWE} and t_{SD} .

Ordering Information

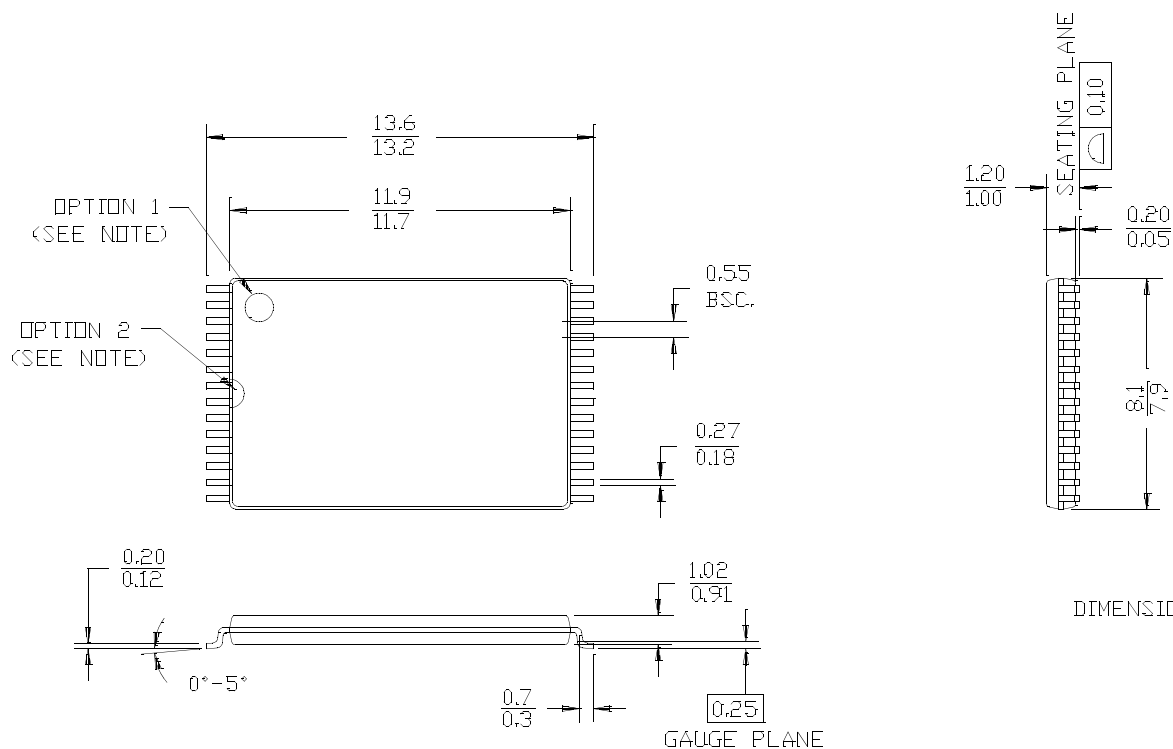
Speed (ns)	Ordering Code	Package Diagram	Package Type	Power Option	Operating Range
12	CY7C199CN-12VC	51-85031	28-Lead (300-Mil) Molded SOJ	Standard	Commercial
	CY7C199CN-12ZC	51-85071	28 TSOP I (8 x 13.4 mm)	Standard	Commercial
	CY7C199CN-12ZX	51-85071	28 TSOP I (8 x 13.4 mm) (Pb-free)	Standard	Commercial
	CY7C199CN-12VI	51-85031	28-Lead (300-Mil) Molded SOJ	Standard	Industrial
	CY7C199CN-12VXI	51-85031	28-Lead (300-Mil) Molded SOJ (Pb-free)	Standard	Industrial
15	CY7C199CN-15PC	51-85014	28 DIP (6.9 x 35.6 x 3.5 mm)	Standard	Commercial
	CY7C199CN-15PXC	51-85014	28 DIP (6.9 x 35.6 x 3.5 mm) (Pb-free)	Standard	Commercial
	CY7C199CN-15VC	51-85031	28-Lead (300-Mil) Molded SOJ	Standard	Commercial
	CY7C199CN-15VXC	51-85031	28-Lead (300-Mil) Molded SOJ (Pb-free)	Standard	Commercial
	CY7C199CN-15ZC	51-85071	28 TSOP I (8 x 13.4 mm) (Pb-free)	Standard	Commercial
	CY7C199CN-15ZX	51-85071	28 TSOP I (8 x 13.4 mm) (Pb-free)	Standard	Commercial
	CY7C199CN-15VI	51-85031	28-Lead (300-Mil) Molded SOJ	Standard	Industrial
	CY7C199CN-15VNC	51-85031	28-Lead (300-Mil) Molded SOJ	Low Power	Commercial
	CY7C199CN-15VXC	51-85031	28-Lead (300-Mil) Molded SOJ (Pb-free)	Low Power	Commercial
	CY7C199CN-15ZX	51-85071	28 TSOP I (8 x 13.4 mm) Lead Free	Low Power	Commercial
	CY7C199CN-15VXI	51-85031	28-Lead (300-Mil) Molded SOJ (Pb-free)	Low Power	Industrial
20	CY7C199CN-20VC	51-85031	28-Lead (300-Mil) Molded SOJ	Standard	Commercial
	CY7C199CN-20ZI	51-85071	28 TSOP I (8 x 13.4 mm)	Standard	Industrial
	CY7C199CN-20ZXI	51-85071	28 TSOP I (8 x 13.4 mm) (Pb-free)	Standard	Industrial
25	CY7C199CN-25PC	51-85014	28 DIP (6.9 x 35.6 x 3.5 mm)	Standard	Commercial
	CY7C199CN-25PXC	51-85014	28 DIP (6.9 x 35.6 x 3.5 mm) (Pb-free)	Standard	Commercial

Please contact local sales representative regarding availability of these parts.

Package Diagram

28-Lead TSOP I (8 x 13.4 mm) (51-85071)

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER
AS SHOWN IN OPTION 1 OR OPTION 2



DIMENSION IN MM
MAX.
MIN.

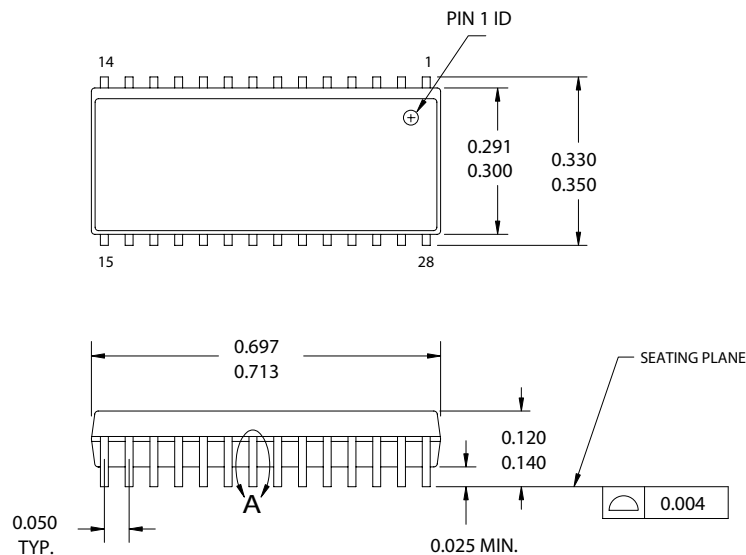
51-85071-G

Package Diagram (continued)

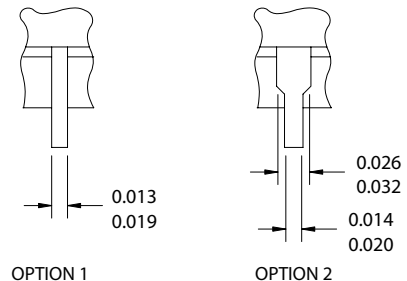
28-Lead (300-Mil) Molded SOJ (51-85031)

NOTE:

1. JEDEC STD REF MO088
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.006 in (0.152 mm) PER SIDE
3. DIMENSIONS IN INCHES MIN. MAX.

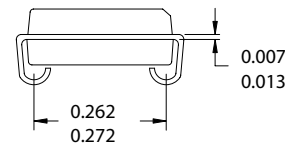


DETAIL A
EXTERNAL LEAD DESIGN



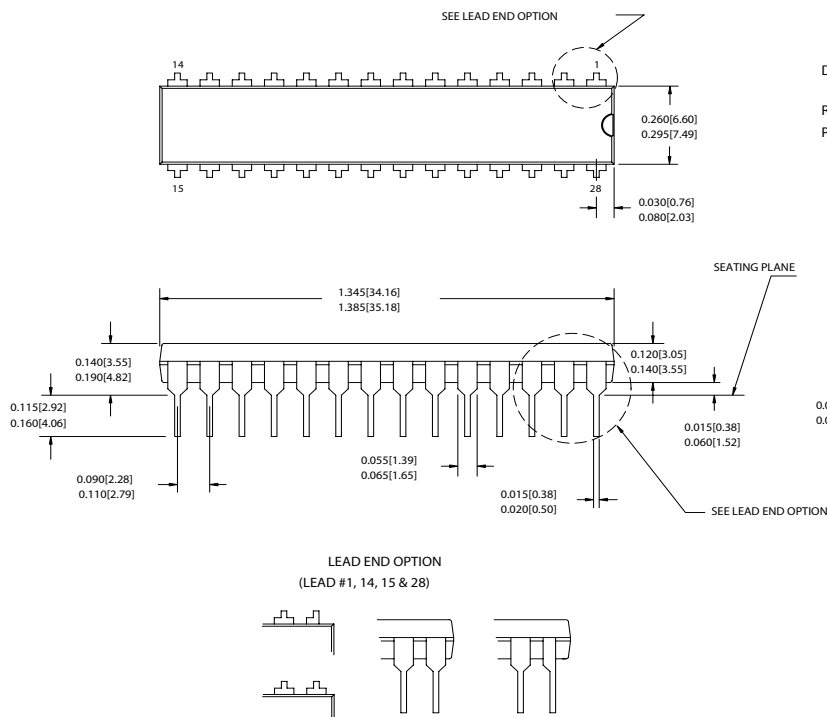
OPTION 1

OPTION 2



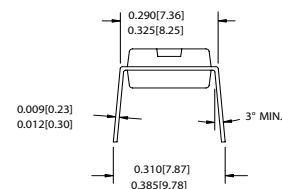
51-85031-*C

28-Lead (300-Mil) PDIP (51-85014)



DIMENSIONS IN INCHES [MM] MIN. MAX.

REFERENCE JEDEC MO-095
PACKAGE WEIGHT: 2.15 gms



51-85014-*D

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Document History Page

Document Title: CY7C199CN 256K (32K x 8) Static RAM Document Number: 001-06435				
REV.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	430363	See ECN	NXR	New Data Sheet