



PRELIMINARY

CY7C1071AV33

32-Mbit (2M x 16) Static RAM

Features

- High density 32-Mbit SRAM
- High speed
 - $t_{AA} = 10 \text{ ns}$
- Low active power
 - $I_{CC} = 450 \text{ mA}$
- Operating voltages of $3.3 \pm 0.3\text{V}$
- 2.0V data retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Available in standard 119-ball FBGA

Functional Description

The CY7C1071AV33 is a 3.3V high-performance 32-Megabit static RAM organized as a 2,097,152 words by 16 bits.

Writing to the device is accomplished by enabling the chip (CE HIGH) while forcing the Write Enable (WE) input LOW. If Byte

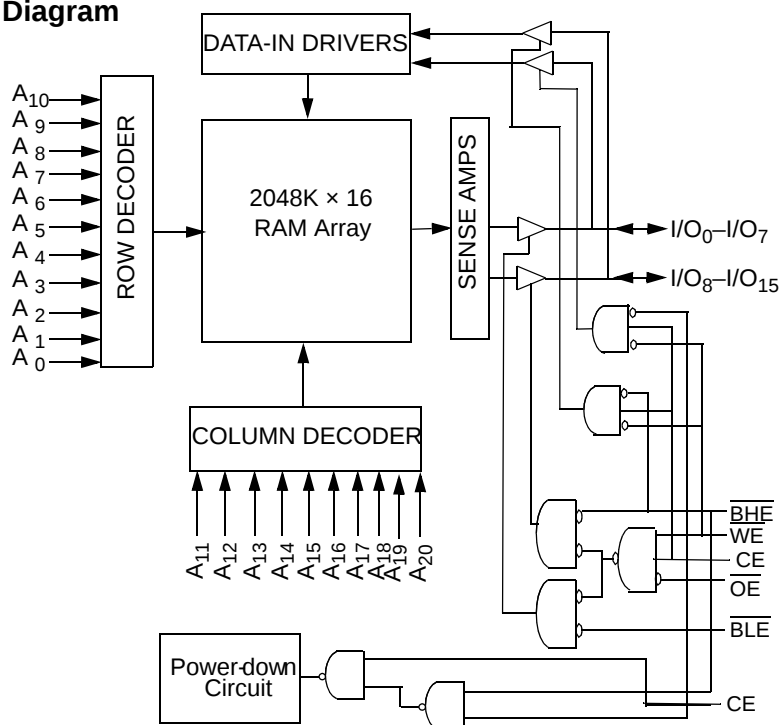
Low Enable ($\overline{\text{BLE}}$) is LOW, then data from the I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{20}). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{20}).

Reading from the device is accomplished by enabling the chip by taking CE HIGH while forcing the Output Enable ($\overline{\text{OE}}$) LOW and the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7 . If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O_8 to I/O_{15} . See the truth table at the back of this data sheet for a complete description of Read and Write modes.

The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected (CE LOW), the outputs are disabled ($\overline{\text{OE}}$ HIGH), the BHE and BLE are disabled ($\overline{\text{BHE}}$, $\overline{\text{BLE}}$ HIGH), or during a Write operation (CE HIGH, and WE LOW).

The CY7C1071AV33 is available in a 119-ball grid array (FBGA) package.

Logic Block Diagram



Selection Guide

		CY7C1071AV33-10	CY7C1071AV33-12	Unit
Maximum Access Time		10	12	ns
Maximum Operating Current	Com'I / Ind'I	450	400	mA
Maximum CMOS Standby Current	Com'I / Ind'I	100	100	mA

Pin Configurations
119 BGA
(Top View)

	1	2	3	4	5	6	7
A	NC	A	A	A	A	A	NC
B	NC	A	A	NC	A	A	NC
C	NC	$\overline{\text{BHE}}$	CE	A	NC	$\overline{\text{BLE}}$	NC
D	NC	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	NC
E	I/O ₈	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₀
F	I/O ₉	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₁
G	I/O ₁₀	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₂
H	I/O ₁₁	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₃
J	NC	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	DNU
K	I/O ₁₂	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₄
L	I/O ₁₃	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₅
M	I/O ₁₄	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O ₆
N	I/O ₁₅	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O ₇
P	NC	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	NC
R	NC	A	NC	A	NC	A	NC
T	NC	A	A	$\overline{\text{WE}}$	A	A	NC
U	NC	A	A	$\overline{\text{OE}}$	A	A	NC

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with
Power Applied -55°C to +125°C

Supply Voltage on V_{CC} to Relative GND^[1] -0.5V to +4.6V

DC Voltage Applied to Outputs
in High-Z State^[1] -0.3V to $V_{CC} + 0.3V$

DC Input Voltage^[1] -0.3V to $V_{CC} + 0.3V$

Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	-40°C to +85°C	

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-10		-12		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage ^[1]		-0.3	0.8	-0.3	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-2	+2	-2	+2	μA
I_{OZ}	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$, Output Disabled	-2	+2	-2	+2	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}, f = f_{MAX} = 1/t_{RC}$ Com'l / Ind'l		450		400	mA
I_{SB1}	Automatic CE Power-down Current — TTL Inputs	$CE \leq V_{IL}$, Max. $V_{CC}, V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}, f = f_{MAX}$		140		140	mA
I_{SB2}	Automatic CE Power-down Current — CMOS Inputs	$CE \leq 0.3V$, Max. $V_{CC}, V_{IN} \geq V_{CC} - 0.3V$, or $V_{IN} \leq 0.3V, f = 0$ Com'l / Ind'l		100		100	mA

Capacitance^[2]

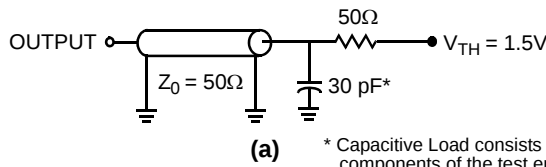
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz}, V_{CC} = 3.3V$	12	pF
C_{OUT}	I/O Capacitance		15	pF

Thermal Resistance^[2]

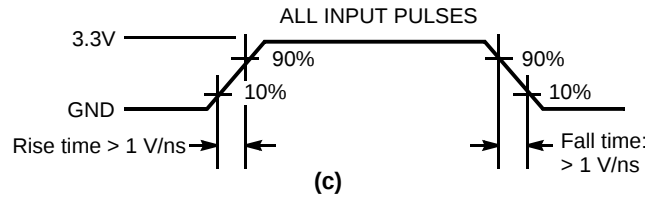
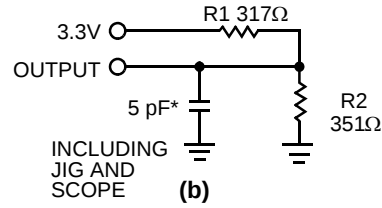
Parameter	Description	Test Conditions	All-Packages	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient) ^[2]	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	TBD	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case) ^[2]		TBD	°C/W

Notes:

- $V_{IL} (\text{min.}) = -2.0V$ and $V_{IH} (\text{max.}) = V_{CC} + 0.5V$ for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms^[3]


* Capacitive Load consists of all components of the test environment.


AC Switching Characteristics Over the Operating Range^[4]

Parameter	Description	-10		-12		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t _{power}	V _{CC} (typical) to the first access ^[5]	1		1		ms
t _{RC}	Read Cycle Time	10		12		ns
t _{AA}	Address to Data Valid		10		12	ns
t _{OHA}	Data Hold from Address Change	3		3		ns
t _{ACE}	CE HIGH to Data Valid		10		12	ns
t _{DOE}	OE LOW to Data Valid		5		6	ns
t _{LZOE}	OE LOW to Low-Z	1		1		ns
t _{HZOE}	OE HIGH to High-Z ^[6]		5		6	ns
t _{LZCE}	CE HIGH to Low-Z ^[6]	3		3		ns
t _{HZCE}	CE LOW to High-Z ^[6]		5		6	ns
t _{PU}	CE HIGH to Power-Up ^[7]	0		0		ns
t _{PD}	CE LOW to Power-Down ^[7]		10		12	ns
t _{DBE}	Byte Enable to Data Valid		10		12	ns
t _{LZBE}	Byte Enable to Low-Z	1		1		ns
t _{HZBE}	Byte Disable to High-Z		5		6	ns
Write Cycle ^[8, 9]						
t _{WC}	Write Cycle Time	10		12		ns
t _{SCE}	CE HIGH to Write End	7		8		ns

Notes:

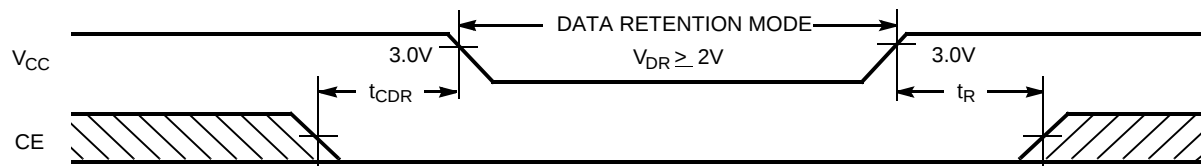
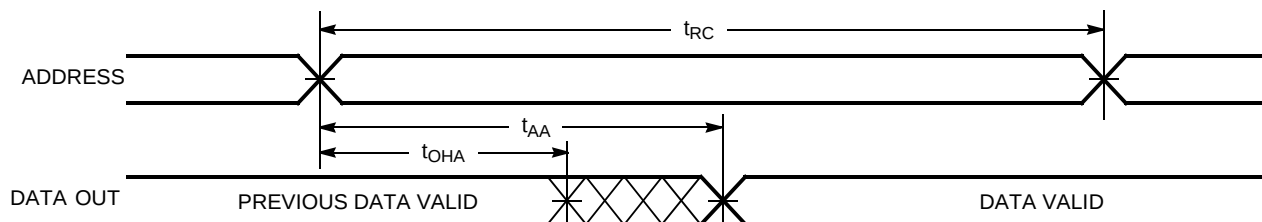
- Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (3.0V). As soon as 1 ms (T_{power}) after reaching the minimum operating V_{DD} , normal SRAM operation can begin including reduction in V_{DD} to the data retention (V_{CCDR} , 2.0V) voltage.
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and specified transmission line loads. Test conditions for the Read cycle use output loading shown in part a) of the AC test loads, unless specified otherwise.
- t_{power} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
- t_{HZOE} , t_{HZCE} , t_{HZWE} , t_{HZBE} and t_{LZOE} , t_{LZCE} , t_{LZWE} , t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal Write time of the memory is defined by the overlap of CE HIGH and $\overline{WE}$ LOW. Chip enables must be active and $\overline{WE}$ and byte enables must be LOW to initiate a Write, and the transition of any of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- The minimum Write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD} .

AC Switching Characteristics Over the Operating Range (continued)^[4]

Parameter	Description	-10		-12		Unit
		Min.	Max.	Min.	Max.	
t_{AW}	Address Set-up to Write End	7		8		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		ns
t_{PWE}	WE Pulse Width	7		8		ns
t_{SD}	Data Set-up to Write End	5.5		6		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	WE HIGH to Low-Z ^[6]	3		3		ns
t_{HZWE}	WE LOW to High-Z ^[6]		5		6	ns
t_{BW}	Byte Enable to End of Write	7		8		ns

Data Retention Characteristics Over the Operating Range

Parameter	Description	Conditions ^[11]	Min.	Max	Unit
V_{DR}	V_{CC} for Data Retention		2.0		V
I_{CCDR}	Data Retention Current Com'l / Ind'l	$V_{CC} = V_{DR} = 2.0V$, $CE \leq 0.3V$		100	mA
$t_{CDR}^{[2]}$	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	0		ns
$t_R^{[10]}$	Operation Recovery Time				μs

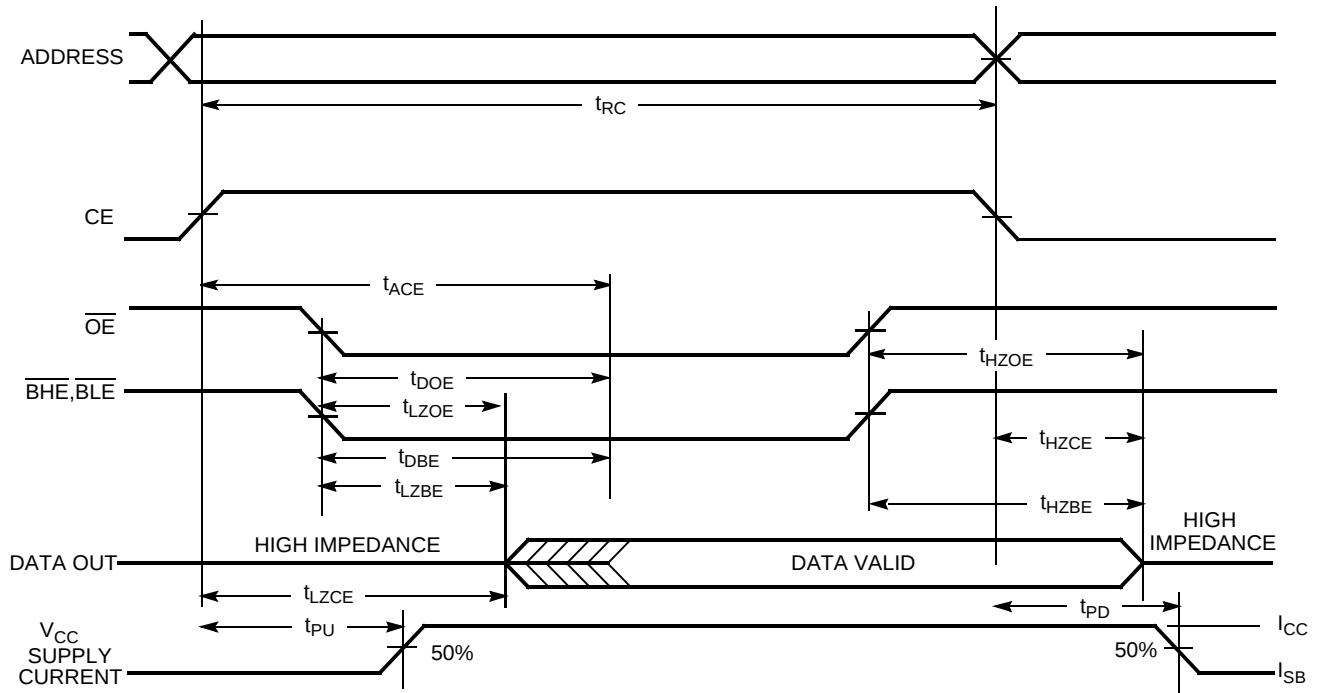
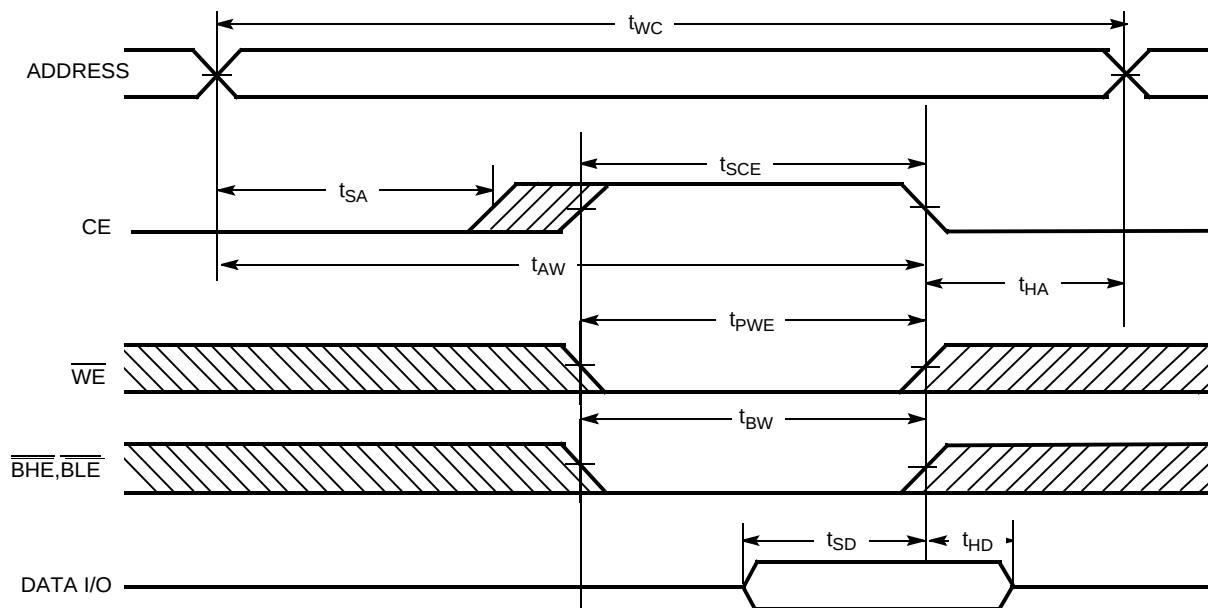
Data Retention Waveform

Switching Waveforms
Read Cycle No. 1^[11, 13]

Notes:

10. Test conditions assume $t_f \leq 3$ ns.

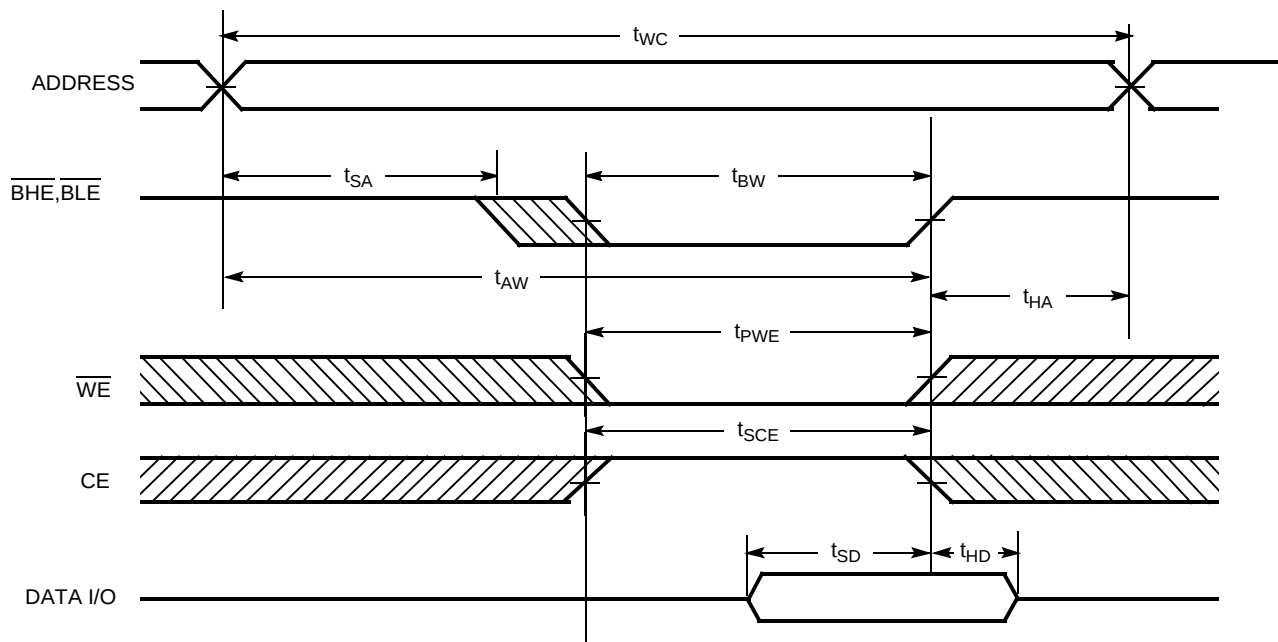
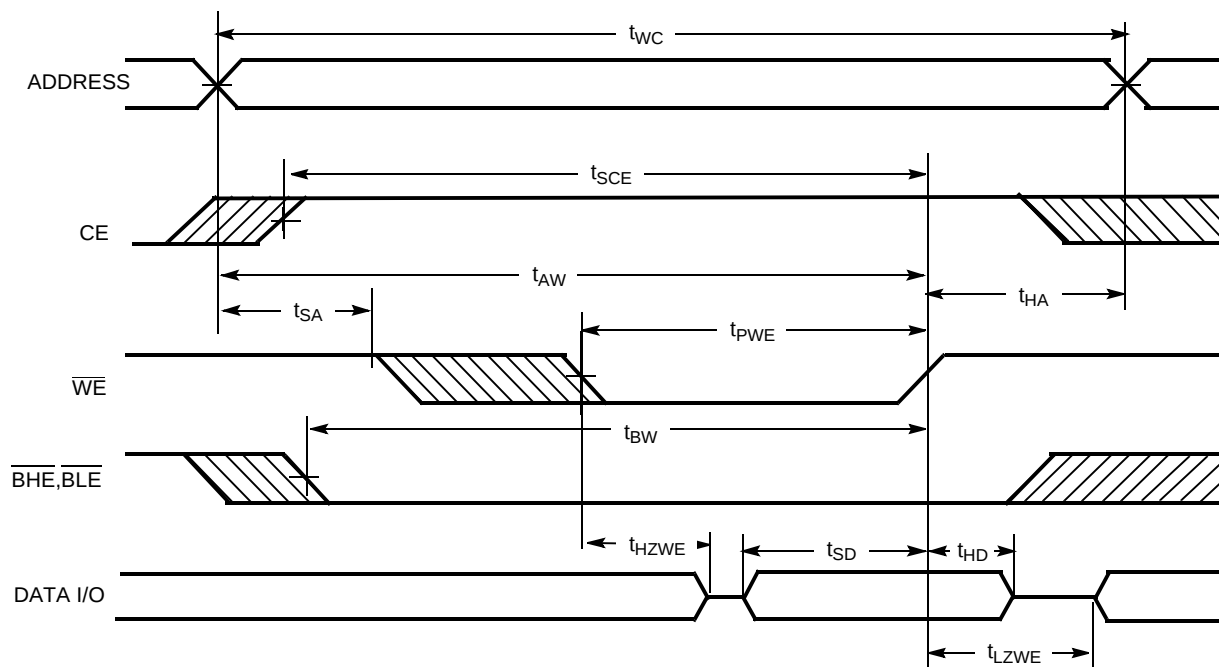
11. No input may exceed $V_{CC} + 0.3V$.

12. Device is continuously selected. $\overline{OE}$, $\overline{BHE}$ and/or $\overline{BWE} = V_{IL}$. $CE = V_{IH}$.

13. WE is HIGH for Read cycle.

Switching Waveforms (continued)
Read Cycle No. 2 ($\overline{OE}$ Controlled)^[13, 14]

Write Cycle No. 1 (CE Controlled)^[15, 16]

Notes:

14. Address valid prior to or coincident with CE transition HIGH.
15. Data I/O is high-impedance if OE or BHE and/or BLE = V_{IH} .
16. If CE goes LOW simultaneously with WE going HIGH, the output remains in a high-impedance state.

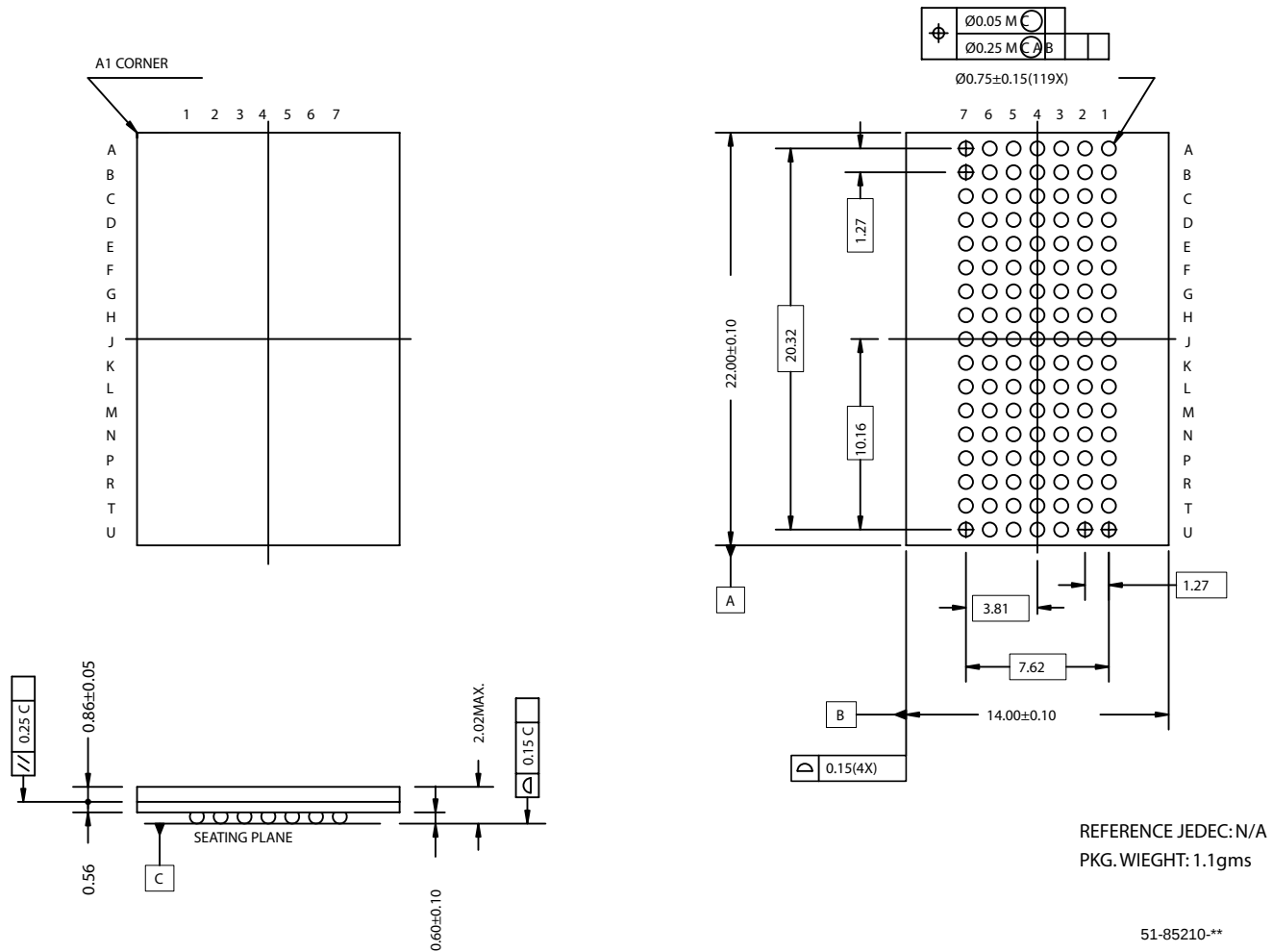
Switching Waveforms (continued)
Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)^[15, 16]

Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[15, 16]


Truth Table

CE	OE	WE	BLE	BHE	I/O ₀ –I/O ₇	I/O ₈ –I/O ₁₅	Mode	Power
L	X	X	X	X	High-Z	High-Z	Power-down	Standby (I _{SB})
H	L	H	L	L	Data Out	Data Out	Read All Bits	Active (I _{CC})
H	L	H	L	H	Data Out	High-Z	Read Lower Bits Only	Active (I _{CC})
H	L	H	H	L	High-Z	Data Out	Read Upper Bits Only	Active (I _{CC})
H	X	L	L	L	Data In	Data In	Write All Bits	Active (I _{CC})
H	X	L	L	H	Data In	High-Z	Write Lower Bits Only	Active (I _{CC})
H	X	L	H	L	High-Z	Data In	Write Upper Bits Only	Active (I _{CC})
H	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active (I _{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1071AV33-10 BBC	BB119	119-Ball (14 x 22 x 2.02 mm) FBGA	Commercial
	CY7C1071AV33-10 BBI			Industrial
12	CY7C1071AV33-12 BBC	BB119	119-Ball (14 x 22 x 2.02 mm) FBGA	Commercial
	CY7C1071AV33-12 BBI			Industrial

Package Diagram
119 FBGA (14 x 22 x 2.02 mm) BB119B


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Document History Page

Document Title: CY7C1071AV33 32-Mbit (2M x 16) Static RAM Document Number: 38-05634				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	278072	See ECN	RKF	New Datasheet
*A	397695	See ECN	SYT	Converted from "Advance Information" to "Preliminary" Changed the MPN from CYM1071AV33 to CY7C1071AV33 Changed Title from "CY7C1071AV33 32-Mbit (2M x 16) Static RAM Module" to "CY7C1071AV33 32-Mbit (2M x 16) Static RAM" Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Removed redundant information from the "Features" and "Functional Description" sections Edited typo 'A ₁₉ ' to 'A ₂₀ ' in the Functional Description on Page # 1 Changed Package offering from 119 PBGA (BG119) to 119 FBGA (BB119) Removed the Package Column from the Capacitance table on Page # 3 Changed the DC Voltage Applied to Outputs in High-Z State and DC Input Voltage from "-0.5V to V _{CC} + 0.5V" to "-0.3V to V _{CC} + 0.3V" in the Maximum Ratings on Page # 3 Changed t _{DBE} from 5 ns to 10 ns and 6 ns to 12 ns for -10 and -12 speed bins respectively on Page # 4 Included spec for I _{CCDR} = 100 mA in the Data Retention Characteristics table on Page# 5 Edited footnote # 11 from "V _{CC} + 0.5V" to "V _{CC} + 0.3V" Referenced footnotes # 15 and 16 on to Write Cycle No.2 Page # 7 Updated the Ordering Information to include the BB119 Package