

# 2-Mbit (128 K × 16) F-RAM Memory

## Features

- 2-Mbit ferroelectric random access memory (F-RAM) logically organized as 128 K × 16
  - Configurable as 256 K × 8 using  $\overline{UB}$  and  $\overline{LB}$
  - High-endurance 100 trillion ( $10^{14}$ ) read/writes
  - 145-year data retention (See the [Data Retention and Endurance](#) table)
  - NoDelay™ writes
  - Page mode operation to 30 ns cycle time
  - Advanced high-reliability ferroelectric process
- SRAM compatible
  - Industry-standard 128 K × 16 SRAM pinout
  - 60 ns access time, 90 ns cycle time
  - Software block protection for 1/4, 1/2, or entire array
- Advanced features
  - Software programmable block write-protect
- Superior to battery-backed SRAM modules
  - No battery concerns
  - Monolithic reliability
  - True surface mount solution, no rework steps
  - Superior for moisture, shock, and vibration
- Low power consumption
  - Active current 7 mA (Typ)
  - Standby current 120 μA (Typ)

- Low-voltage operation:  $V_{DD} = 2.0\text{ V to }3.6\text{ V}$
- Industrial temperature  $-40\text{ °C to }+85\text{ °C}$
- 44-pin thin small outline package (TSOP) Type II
- Restriction of hazardous substances (RoHS) compliant

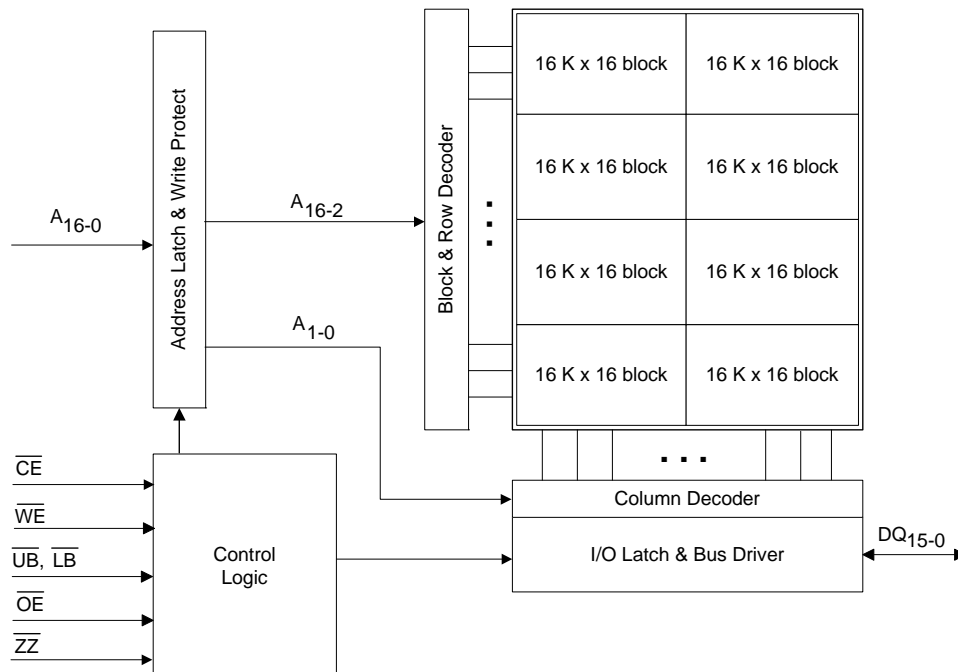
## Functional Overview

The FM28V202 is a 128 K × 16 nonvolatile memory that reads and writes similar to a standard SRAM. A ferroelectric random access memory or F-RAM is nonvolatile, which means that data is retained after power is removed. It provides data retention for over 145 years while eliminating the reliability concerns, functional disadvantages, and system design complexities of battery-backed SRAM (BBSRAM). Fast write timing and high write endurance make the F-RAM superior to other types of memory.

The FM28V202 operation is similar to that of other RAM devices and hence it can be used as a drop-in replacement for a standard SRAM in a system. Read and write cycles may be triggered by  $\overline{CE}$  or simply by changing the address. The F-RAM memory is nonvolatile due to its unique ferroelectric memory process. These features make the FM28V202 ideal for nonvolatile memory applications requiring frequent or rapid writes.

The device is available in a 400 mil 44-pin TSOP-II surface mount package. Device specifications are guaranteed over the industrial temperature range  $-40\text{ °C to }+85\text{ °C}$ .

## Logic Block Diagram

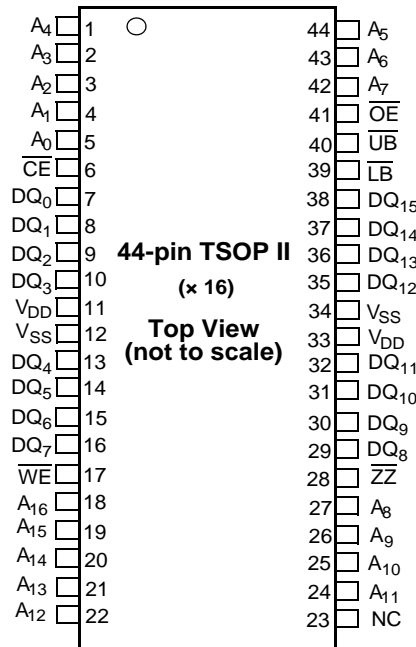


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**Pinout**

**Figure 1. 44-pin TSOP II pinout**



**Pin Definitions**

Pin Name	I/O Type	Description
A <sub>0</sub> -A <sub>16</sub>	Input	<b>Address inputs:</b> The 17 address lines select one of 128K words in the F-RAM array. The lowest two address lines A <sub>1</sub> -A <sub>0</sub> may be used for page mode read and write operations.
DQ <sub>0</sub> -DQ <sub>15</sub>	Input/Output	<b>Data I/O Lines:</b> 16-bit bi-directional data bus for accessing the F-RAM array.
$\overline{WE}$	Input	<b>Write Enable:</b> A write cycle begins when $\overline{WE}$ is asserted. The rising edge causes the FM28V202 to write the data on the DQ bus to the F-RAM array. The falling edge of WE latches a new column address for page mode write cycles.
$\overline{CE}$	Input	<b>Chip Enable:</b> The device is selected and a new memory access begins on the falling edge of $\overline{CE}$ . The entire address is latched internally at this point. Subsequent changes to the A <sub>1</sub> -A <sub>0</sub> address inputs allow page mode operation.
$\overline{OE}$	Input	<b>Output Enable:</b> When $\overline{OE}$ is low, the FM28V202 drives the data bus when valid read data is available. Deasserting $\overline{OE}$ high tristates the DQ pins.
$\overline{UB}$	Input	<b>Upper Byte Select:</b> Enables DQ <sub>15</sub> -DQ <sub>8</sub> pins during reads and writes. These pins are HI-Z if $\overline{UB}$ is high. If the user does not perform byte writes and the device is not configured as a 256K x 8, the $\overline{UB}$ and $\overline{LB}$ pins may be tied to ground.
$\overline{LB}$	Input	<b>Lower Byte Select:</b> Enables DQ <sub>7</sub> -DQ <sub>0</sub> pins during reads and writes. These pins are HI-Z if $\overline{LB}$ is high. If the user does not perform byte writes and the device is not configured as a 256 K x 8, the $\overline{UB}$ and $\overline{LB}$ pins may be tied to ground.
$\overline{ZZ}$	Input	<b>Sleep:</b> When $\overline{ZZ}$ is low, the device enters a low power sleep mode for the lowest supply current condition. $\overline{ZZ}$ must be high for normal read/write operation. The $\overline{ZZ}$ pin is internally pulled up.
V <sub>SS</sub>	Ground	Ground for the device. Must be connected to the ground of the system.
V <sub>DD</sub>	Power supply	Power supply inputs to the device.
NC	No connect	No connect. This pin is not connected to the die.

## Device Operation

The FM28V202 is a worldwide F-RAM memory logically organized as 131,072 × 16 and accessed using an industry-standard parallel interface. All data written to the part is immediately nonvolatile with no delay. The device offers page mode operation, which provides high-speed access to addresses within a page (row). Access to a different page requires that either CE transitions low or the upper address (A<sub>16</sub>–A<sub>2</sub>) changes. See the [Functional Truth Table on page 17](#) for a complete description of read and write modes.

## Memory Operation

Users access 131,072 memory locations, each with 16 data bits through a parallel interface. The F-RAM array is organized as eight blocks, each having 4096 rows. Each row has four column locations, which allow fast access in page mode operation. When an initial address is latched by the falling edge of CE, subsequent column locations may be accessed without the need to toggle CE. When CE is deasserted high, a pre-charge operation begins. Writes occur immediately at the end of the access with no delay. The WE pin must be toggled for each write operation. The write data is stored in the nonvolatile memory array immediately, which is a feature unique to F-RAM called NoDelay writes.

## Read Operation

A read operation begins on the falling edge of CE. The falling edge of CE causes the address to be latched and starts a memory read cycle if WE is high. Data becomes available on the bus after the access time is met. When the address is latched and the access completed, a new access to a random location (different row) may begin while CE is still low. The minimum cycle time for random addresses is t<sub>RC</sub>. Note that unlike SRAMs, the FM28V202's CE-initiated access time is faster than the address access time.

The FM28V202 will drive the data bus when OE and at least one of the byte enables (UB, LB) is asserted low. The upper data byte is driven when UB is low, and the lower data byte is driven when LB is low. If OE is asserted after the memory access time is met, the data bus will be driven with valid data. If OE is asserted before completing the memory access, the data bus will not be driven until valid data is available. This feature minimizes supply current in the system by eliminating transients caused by invalid data being driven onto the bus. When OE is deasserted high, the data bus will remain in a HI-Z state.

## Write Operation

In the FM28V202, writes occur in the same interval as reads. The FM28V202 supports both CE- and WE-controlled write cycles. In both cases, the address A<sub>16</sub>–A<sub>2</sub> is latched on the falling edge of CE.

In a CE-controlled write, the WE signal is asserted before beginning the memory cycle. That is, WE is low when CE falls. In this case, the device begins the memory cycle as a write. The FM28V202 will not drive the data bus regardless of the state of OE as long as WE is low. Input data must be valid when CE is deasserted high. In a WE-controlled write, the memory cycle

begins on the falling edge of CE. The WE signal falls some time later. Therefore, the memory cycle begins as a read. The data bus will be driven if OE is low; however, it will be HI-Z when WE is asserted low. The CE- and WE-controlled write timing cases are shown in the [Switching Waveforms on page 13](#).

Write access to the array begins on the falling edge of WE after the memory cycle is initiated. The write access terminates on the rising edge of WE or CE, whichever comes first. A valid write operation requires the user to meet the access time specification before deasserting WE or CE. Data setup time indicates the interval during which data cannot change before the end of the write access (rising edge of WE or CE).

Unlike other nonvolatile memory technologies, there is no write delay with F-RAM. Because the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory operation occurs in a single bus cycle. Data polling, a technique used with EEPROMs to determine if a write is complete, is unnecessary.

## Page Mode Operation

The F-RAM array is organized as eight blocks, each having 4096 rows. Each row has four column address locations. Address inputs A<sub>1</sub>–A<sub>0</sub> define the column address to be accessed. An access can start on any column address, and other column locations may be accessed without the need to toggle the CE pin. For fast access reads, after the first data byte is driven onto the bus, the column address inputs A<sub>1</sub>–A<sub>0</sub> may be changed to a new value. A new data byte is then driven to the DQ pins no later than t<sub>AAP</sub>, which is less than half the initial read access time. For fast access writes, the first write pulse defines the first write access. While CE is low, a subsequent write pulse along with a new column address provides a page mode write access.

## Pre-charge Operation

The pre-charge operation is an internal condition in which the memory state is prepared for a new access. Pre-charge is user-initiated by driving the CE signal high. It must remain high for at least the minimum pre-charge time t<sub>PC</sub>.

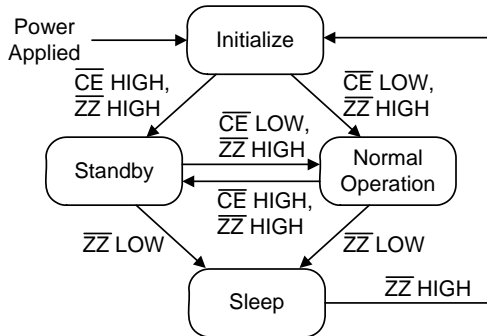
Pre-charge is also activated by changing the upper address A<sub>16</sub>–A<sub>2</sub>. The current row is first closed before accessing the new row. The device automatically detects an upper order address change, which starts a pre-charge operation. The new address is latched and the new read data is valid within the t<sub>AA</sub> address access time; see [Figure 8 on page 13](#). A similar sequence occurs for write cycles; see [Figure 13 on page 14](#). The rate at which random addresses can be issued is t<sub>RC</sub> and t<sub>WC</sub>, respectively.

## Sleep Mode

The device incorporates a sleep mode of operation, which allows the user to achieve the lowest power supply current condition. It enters a low-power sleep mode by asserting the ZZ pin low. Read and write operations must complete before the ZZ pin going low. When ZZ is low, all pins are ignored except the ZZ pin. When ZZ is deasserted high, there is some time delay (t<sub>ZZEX</sub>) before the user can access the device.

If sleep mode is not used, the ZZ pin may be floated (internal pull-up) or tied to V<sub>DD</sub>.

**Figure 2. Sleep/Standby State Diagram**



**Software Write Protect**

The 128 K × 16 address space is divided into eight sectors (blocks) of 16 K × 16 each. Each sector can be individually software write-protected and the settings are nonvolatile. A unique address and command sequence invokes the write-protect mode.

To modify write protection, the system host must issue six read commands, three write commands, and a final read command. The specific sequence of read addresses must be provided to access the write-protect mode. Following the read address sequence, the host must write a data byte that specifies the desired protection state of each sector. For confirmation, the system must then write the complement of the protection byte immediately after the protection byte. Any error that occurs including read addresses in the wrong order, issuing a seventh read address, or failing to complement the protection value will leave the write protection unchanged.

The write-protect state machine monitors all addresses, taking no action until this particular read/write sequence occurs. During the address sequence, each read will occur as a valid operation and data from the corresponding addresses will be driven onto the data bus. Any address that occurs out of sequence will cause the software protection state machine to start over. After the address sequence is completed, the next operation must be a write cycle. The lower data byte contains the write-protect settings. This value will not be written to the memory array, so the address is a don't-care. Rather it will be held pending the next cycle, which must be a write of the data complement to the protection settings. If the complement is correct, the write-protect settings will be adjusted. Otherwise, the process is aborted and the address sequence starts over. The data value written after the correct six addresses will not be entered into memory.

The protection data byte consists of eight bits, each associated with the write-protect state of a sector. The data byte must be driven to the lower eight bits of the data bus, DQ<sub>7</sub> - DQ<sub>0</sub>. Setting a bit to '1' write-protects the corresponding sector; a 0 enables writes for that sector. The following table shows the write-protect sectors with the corresponding bit that controls the write-protect setting.

**Table 1. Write Protect Sectors - 16K x 16 Blocks**

Sectors	Blocks
Sector 7	1FFFFh–1C000h
Sector 6	1BFFFh–18000h
Sector 5	17FFFh–14000h
Sector 4	13FFFh–10000h
Sector 3	0FFFFh–0C000h
Sector 2	0BFFFh–08000h
Sector 1	07FFFh–04000h
Sector 0	03FFFh–00000h

The write-protect address sequence follows:

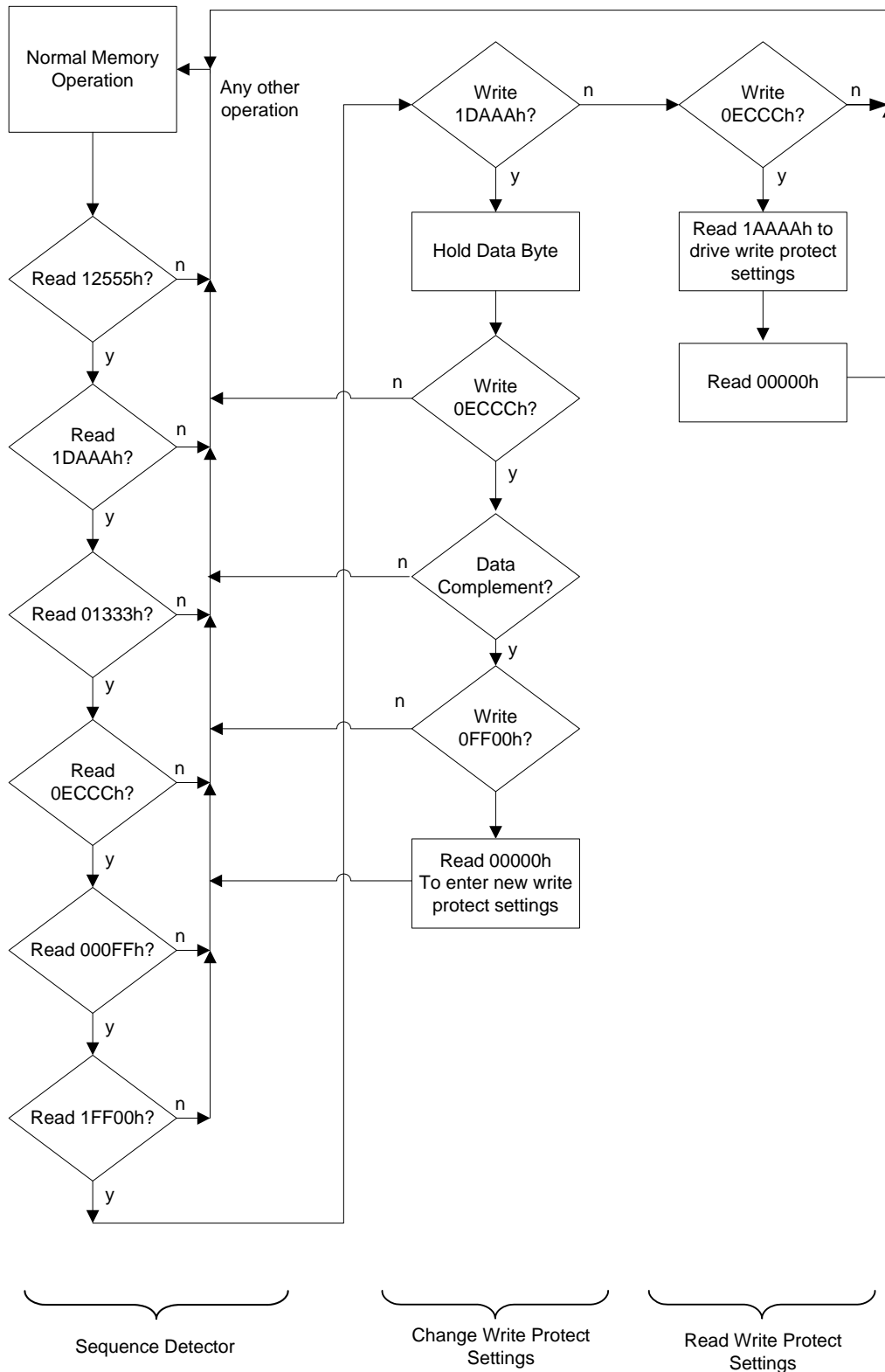
1. Read address 12555h
2. Read address 1DAAAh
3. Read address 01333h
4. Read address 0ECCCh
5. Read address 000FFh
6. Read address 1FF00h
7. Write address 1DAAAh
8. Write address 0ECCCh
9. Write address 0FF00h
10. Read address 00000h

The address sequence provides a secure way of modifying the protection. The write-protect sequence has a one in 3 × 10<sup>32</sup> chance of randomly accessing exactly the first six addresses. The odds are further reduced by requiring three more write cycles, one that requires an exact inversion of the data byte. [Figure 3 on page 6](#) shows a flow chart of the entire write-protect operation. The write-protect settings are nonvolatile. The factory default: all blocks are unprotected.

For example, the following sequence write-protects addresses from 0C000h to 13FFFh (sectors 3 and 4):

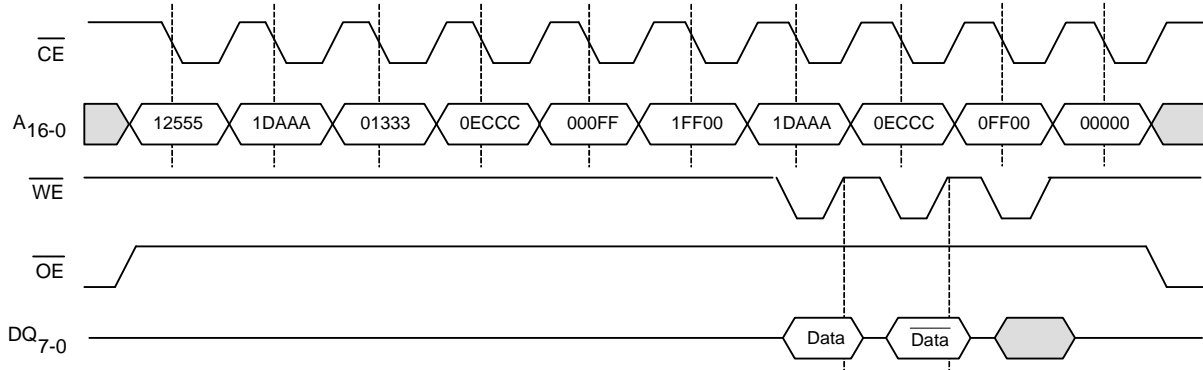
	Address	Data
Read	12555h	-
Read	1DAAAh	-
Read	01333h	-
Read	0ECCCh	-
Read	000FFh	-
Read	1FF00h	-
Write	1DAAAh	18h; bits 3 and 4 = 1
Write	0ECCCh	E7h; complement of 18h
Write	0FF00h	Don't care
Read	00000h	

Figure 3. Write-Protect State Machine

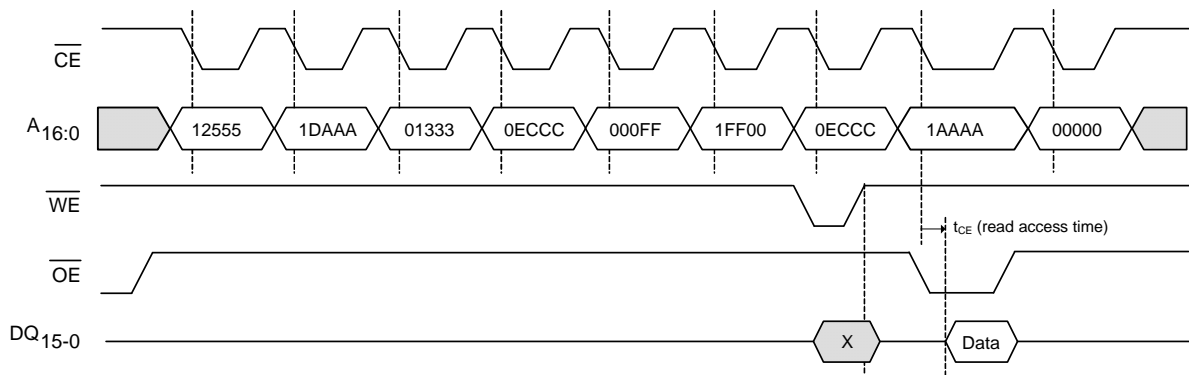


**Software Write-Protect Timing**

**Figure 4. Sequence to Set Write-Protect Blocks [1]**



**Figure 5. Sequence to Read Write-Protect Settings [1]**



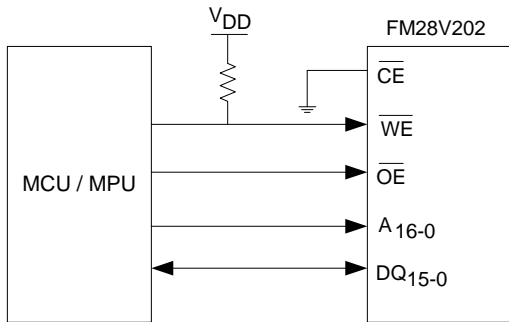
**Note**

1. This sequence requires  $t_{AS} \geq 10$  ns and address must be stable while  $\overline{CE}$  is low.

### SRAM Drop-In Replacement

The FM28V202 is designed to be a drop-in replacement for standard asynchronous SRAMs. The device does not require  $\overline{CE}$  to toggle for each new address.  $\overline{CE}$  may remain low indefinitely. While  $\overline{CE}$  is low, the device automatically detects address changes and a new access is begun. This functionality allows  $\overline{CE}$  to be grounded, similar to an SRAM. It also allows page mode operation at speeds up to 33 MHz. Note that if  $\overline{CE}$  is tied to ground, the user must be sure  $\overline{WE}$  is not low at power-up or power-down events. If  $\overline{CE}$  and  $\overline{WE}$  are both low during power cycles, data will be corrupted. Figure 6 shows a pull-up resistor on  $\overline{WE}$ , which will keep the pin high during power cycles assuming the MCU/MPU pin tristates during the reset condition. The pull-up resistor value should be chosen to ensure the  $\overline{WE}$  pin tracks  $V_{DD}$  yet a high enough value that the current drawn when  $\overline{WE}$  is low is not an issue. A 10-k $\Omega$  resistor draws 330  $\mu$ A when  $\overline{WE}$  is low and  $V_{DD} = 3.3$  V. Note that software write-protect is not available if the chip enable pin is hard-wired.

Figure 6. Use of Pullup Resistor on  $\overline{WE}$



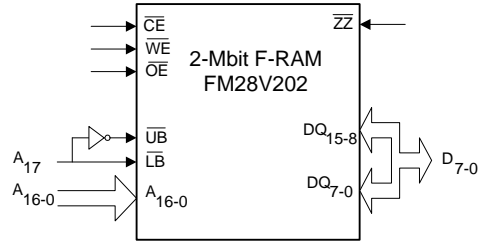
For applications that require the lowest power consumption, the  $\overline{CE}$  signal should be active (low) only during memory accesses. The FM28V202 draws supply current while  $\overline{CE}$  is low, even if addresses and control signals are static. While  $\overline{CE}$  is high, the device draws no more than the maximum standby current  $I_{SB}$ .

The FM28V202 is backward compatible with the 2-Mbit FM21L16 device. There are some differences in the timing specifications. Refer to the FM21L16 datasheet.

The  $\overline{UB}$  and  $\overline{LB}$  byte select pins are active for both read and write cycles. They may be used to allow the device to be wired as a 256K x 8 memory. The upper and lower data bytes can be tied together and controlled with the byte selects. Individual byte

enables or the next higher address line  $A_{17}$  may be available from the system processor.

Figure 7. FM28V202 Wired as 256 K x 8



### Endurance

The FM28V202 is capable of being accessed at least  $10^{14}$  times - reads or writes. An F-RAM memory operates with a read and restore mechanism. Therefore, an endurance cycle is applied on a row basis. The F-RAM architecture is based on an array of rows and columns. Rows are defined by  $A_{16-2}$  and column addresses by  $A_{1-0}$ . The array is organized as 32K rows of four words each. The entire row is internally accessed once whether a single 16-bit word or all four words are read or written. Each word in the row is counted only once in an endurance calculation.

The user may choose to write CPU instructions and run them from a certain address space. Table 2 shows endurance calculations for 256-byte repeating loop, which includes a starting address, three-page mode accesses, and a  $\overline{CE}$  pre-charge. The number of bus clock cycles needed to complete a four-word transaction is 4 + 1 at lower bus speeds, but 5 + 2 at 33 MHz due to initial read latency and an extra clock cycle to satisfy the device's pre-charge timing constraint  $t_{PC}$ . The entire loop causes each byte to experience only one endurance cycle. F-RAM read and write endurance is virtually unlimited even at 33 MHz system bus clock rate.

Table 2. Time to Reach 100 Trillion Cycles for Repeating 256-byte Loop

Bus Freq (MHz)	Bus Cycle Time (ns)	256-byte Transaction Time ( $\mu$ s)	Endurance Cycles/sec.	Endurance Cycles/year	Years to Reach $10^{14}$ Cycles
33	30	10.56	94,690	$2.98 \times 10^{12}$	33.5
25	40	12.8	78,125	$2.46 \times 10^{12}$	40.6
10	100	28.8	34,720	$1.09 \times 10^{12}$	91.7
5	200	57.6	17,360	$5.47 \times 10^{11}$	182.8

**Maximum Ratings**

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

- Storage temperature ..... -55 °C to +125 °C
- Maximum junction temperature ..... 95 °C
- Supply voltage on V<sub>DD</sub> relative to V<sub>SS</sub> ..... -1.0 V to + 4.5 V
- Voltage applied to outputs in High Z state ..... -0.5 V to V<sub>DD</sub>+ 0.5 V
- Input voltage ..... -1.0 V to + 4.5 V and V<sub>IN</sub> < V<sub>DD</sub> + 1.0 V
- Transient voltage (< 20 ns) on any pin to ground potential ..... -2.0 V to V<sub>CC</sub> + 2.0 V
- Package power dissipation capability (T<sub>A</sub> = 25 °C) ..... 1.0 W

- Surface mount Pb soldering temperature (3 seconds) ..... +260 °C
- DC output current (1 output at a time, 1s duration) .... 15 mA
- Static discharge voltage
  - Human Body Model (AEC-Q100-002 Rev. E) ..... 4 kV
  - Charged Device Model (AEC-Q100-011 Rev. B) .. 1.25 kV
  - Machine Model (AEC-Q100-003 Rev. E) ..... 250 V
- Latch-up current ..... > 140 mA

**Operating Range**

Range	Ambient Temperature	V <sub>DD</sub>
Industrial	-40 °C to +85 °C	2.0 V to 3.6 V

**DC Electrical Characteristics**

Over the [Operating Range](#)

Parameter	Description	Test Conditions	Min	Typ	Max	Unit	
V <sub>DD</sub>	Power supply voltage		2.0	3.3	3.6	V	
I <sub>DD</sub>	V <sub>DD</sub> supply current	V <sub>DD</sub> = 3.6 V, $\overline{CE}$ cycling at min. cycle time. All inputs toggling at CMOS levels (0.2 V or V <sub>DD</sub> - 0.2 V), all DQ pins unloaded.	-	7	12	mA	
I <sub>SB</sub>	Sleep mode current	V <sub>DD</sub> = 3.6 V, $\overline{CE}$ at V <sub>DD</sub> . All other pins are static and at CMOS levels (0.2 V or V <sub>DD</sub> - 0.2 V), $\overline{ZZ}$ is high	At T <sub>A</sub> = 25 °C	-	120	150	μA
			At T <sub>A</sub> = 85 °C	-	-	250	μA
I <sub>ZZ</sub>	Standby current	V <sub>DD</sub> = 3.6 V, $\overline{ZZ}$ is low, all other inputs at CMOS levels (0.2 V or V <sub>DD</sub> - 0.2 V).	At T <sub>A</sub> = 25 °C	-	3	5	μA
			At T <sub>A</sub> = 85 °C	-	-	8	μA
I <sub>LI</sub>	Input leakage current	V <sub>IN</sub> , V <sub>OUT</sub> between V <sub>DD</sub> and V <sub>SS</sub>	-	-	±1	μA	
I <sub>LO</sub>	Output leakage current	V <sub>IN</sub> , V <sub>OUT</sub> between V <sub>DD</sub> and V <sub>SS</sub> .	-	-	±1	μA	
V <sub>IH1</sub>	Input high voltage	V <sub>DD</sub> = 2.7 V to 3.6 V	2.2	-	V <sub>DD</sub> + 0.3	V	
V <sub>IH2</sub>	Input high voltage	V <sub>DD</sub> = 2.0 V to 2.7 V	0.7 x V <sub>DD</sub>	-	-	V	
V <sub>IL1</sub>	Input low voltage	V <sub>DD</sub> = 2.7 V to 3.6 V	- 0.3	-	0.8	V	
V <sub>IL2</sub>	Input low voltage	V <sub>DD</sub> = 2.0 V to 2.7 V	- 0.3	-	0.3 x V <sub>DD</sub>	V	
V <sub>OH1</sub>	Output high voltage	I <sub>OH</sub> = -1 mA, V <sub>DD</sub> > 2.7 V	2.4	-	-	V	
V <sub>OH2</sub>	Output high voltage	I <sub>OH</sub> = -100 μA	V <sub>DD</sub> - 0.2	-	-	V	
V <sub>OL1</sub>	Output low voltage	I <sub>OL</sub> = 2 mA, V <sub>DD</sub> > 2.7 V	-	-	0.4	V	
V <sub>OL2</sub>	Output low voltage	I <sub>OL</sub> = 150 μA	-	-	0.2	V	
R <sub>IN</sub> <sup>[2]</sup>	Input resistance ( $\overline{ZZ}$ pin)	For V <sub>IN</sub> = V <sub>IH</sub> (min)	40	-	-	kΩ	
		For V <sub>IN</sub> = V <sub>IL</sub> (max)	1	-	-	MΩ	

**Note**

2. The input pull-up circuit is strong (> 40 kΩ) when the input voltage is above V<sub>IH</sub> and weak (>1 MΩ) when the input voltage is below V<sub>IL</sub>.

**Data Retention and Endurance**

Parameter	Description	Test condition	Min	Max	Unit
T <sub>DR</sub>	Data retention	At +85 °C	10	–	Years
		At +75 °C	37	–	
		At +65 °C	145	–	
N <sub>VC</sub>	Endurance	Over operating temperature	10 <sup>14</sup>	–	Cycles

**Capacitance**

Parameter	Description	Test Conditions	Max	Unit
C <sub>I/O</sub>	Input/Output capacitance (DQ)	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>DD</sub> = V <sub>DD(Typ)</sub>	8	pF
C <sub>IN</sub>	Input capacitance		6	pF
C <sub>ZZ</sub>	Input capacitance of $\overline{ZZ}$ pin		8	pF

**Thermal Resistance**

Parameter	Description	Test Conditions	44-pin TSOP II	Unit
⊖ <sub>JA</sub>	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	107	°C/W
⊖ <sub>JC</sub>	Thermal resistance (junction to case)		25	°C/W

**AC Test Conditions**

Input pulse levels .....0 V to 3 V  
 Input rise and fall times (10%–90%) ..... ≤ 3 ns  
 Input and output timing reference levels ..... 1.5 V  
 Output load capacitance ..... 30 pF

## AC Switching Characteristics

 Over the [Operating Range](#)

Parameters <sup>[3]</sup>		Description	V <sub>DD</sub> = 2.0 V to 2.7 V		V <sub>DD</sub> = 2.7 V to 3.6 V		Unit
Cypress Parameter	Alt Parameter		Min	Max	Min	Max	
<b>SRAM Read Cycle</b>							
t <sub>CE</sub>	t <sub>ACE</sub>	Chip enable access time	–	70	–	60	ns
t <sub>RC</sub>	–	Read cycle time	105	–	90	–	ns
t <sub>AA</sub>	–	Address access time	–	105	–	90	ns
t <sub>OH</sub>	t <sub>OHA</sub>	Output hold time	20	–	20	–	ns
t <sub>AAP</sub>	–	Page mode address access time	–	40	–	30	ns
t <sub>OHP</sub>	–	Page mode output hold time	3	–	3	–	ns
t <sub>CA</sub>	–	Chip enable active time	70	–	60	–	ns
t <sub>PC</sub>	–	Pre-charge time	35	–	30	–	ns
t <sub>BA</sub>	t <sub>BW</sub>	$\overline{UB}$ , $\overline{LB}$ access time	–	25	–	15	ns
t <sub>AS</sub>	t <sub>SA</sub>	Address setup time (to $\overline{CE}$ low)	0	–	0	–	ns
t <sub>AH</sub>	t <sub>HA</sub>	Address hold time ( $\overline{CE}$ Controlled)	70	–	60	–	ns
t <sub>OE</sub>	t <sub>DOE</sub>	Output enable access time	–	25	–	15	ns
t <sub>HZ</sub> <sup>[4, 5]</sup>	t <sub>HZCE</sub>	Chip Enable to output HI-Z	–	15	–	10	ns
t <sub>OHZ</sub> <sup>[4, 5]</sup>	t <sub>HZOE</sub>	Output enable high to output HI-Z	–	15	–	10	ns
t <sub>BHZ</sub> <sup>[4, 5]</sup>	t <sub>HZBE</sub>	$\overline{UB}$ , $\overline{LB}$ high to output HI-Z	–	15	–	10	ns

### Notes

- Test conditions assume a signal transition time of 3 ns or less, timing reference levels of  $0.5 \times V_{DD}$ , input pulse levels of 0 to 3V, output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance shown in [AC Test Conditions on page 10](#).
- t<sub>HZ</sub>, t<sub>OHZ</sub> and t<sub>BHZ</sub> are specified with a load capacitance of 5 pF. Transition is measured when the outputs enter a high impedance state.
- This parameter is characterized but not 100% tested.

**AC Switching Characteristics** (continued)

 Over the [Operating Range](#)

Parameters <sup>[3]</sup>		Description	V <sub>DD</sub> = 2.0 V to 2.7 V		V <sub>DD</sub> = 2.7 V to 3.6 V		Unit
Cypress Parameter	Alt Parameter		Min	Max	Min	Max	
<b>SRAM Write Cycle</b>							
t <sub>WC</sub>	t <sub>WC</sub>	Write cycle time	105	–	90	–	ns
t <sub>CA</sub>	–	Chip enable active time	70	–	60	–	ns
t <sub>CW</sub>	t <sub>SCE</sub>	Chip enable to write enable high	70	–	60	–	ns
t <sub>PC</sub>	–	Pre-charge time	35	–	30	–	ns
t <sub>PWC</sub>	–	Page mode write enable cycle time	40	–	30	–	ns
t <sub>WP</sub>	t <sub>PWE</sub>	Write enable pulse width	22	–	18	–	ns
t <sub>WP2</sub>	t <sub>BW</sub>	$\overline{UB}$ , $\overline{LB}$ pulse width	22	–	18	–	ns
t <sub>WP3</sub>	t <sub>PWE</sub>	$\overline{WE}$ low to $\overline{UB}$ , $\overline{LB}$ high	22	–	18	–	ns
t <sub>AS</sub>	t <sub>SA</sub>	Address setup time (to $\overline{CE}$ low)	0	–	0	–	ns
t <sub>AH</sub>	t <sub>HA</sub>	Address hold time ( $\overline{CE}$ Controlled)	70	–	60	–	ns
t <sub>ASP</sub>	–	Page mode address setup time (to $\overline{WE}$ low)	8	–	5	–	ns
t <sub>AHP</sub>	–	Page mode address hold time (to $\overline{WE}$ low)	20	–	15	–	ns
t <sub>WLC</sub>	t <sub>PWE</sub>	Write enable low to chip disabled	30	–	25	–	ns
t <sub>BLC</sub>	t <sub>BW</sub>	$\overline{UB}$ , $\overline{LB}$ low to chip disabled	30	–	25	–	ns
t <sub>WLA</sub>	–	Write enable low to A <sub>16-2</sub> change	30	–	25	–	ns
t <sub>AWH</sub>	–	A <sub>16-2</sub> change to write enable high	105	–	90	–	ns
t <sub>DS</sub>	t <sub>SD</sub>	Data input setup time	20	–	15	–	ns
t <sub>DH</sub>	t <sub>HD</sub>	Data input hold time	0	–	0	–	ns
t <sub>WZ</sub> <sup>[6, 7]</sup>	t <sub>HZWE</sub>	Write enable low to output HI-Z	–	10	–	10	ns
t <sub>WX</sub> <sup>[7]</sup>	–	Write enable high to output driven	8	–	5	–	ns
t <sub>BDS</sub>	–	Byte disable setup time (to $\overline{WE}$ low)	8	–	5	–	ns
t <sub>BDH</sub>	–	Byte disable hold time (to $\overline{WE}$ high)	8	–	5	–	ns

**Notes**

6. t<sub>WZ</sub> is specified with a load capacitance of 5 pF. Transition is measured when the outputs enter a high impedance state.
7. This parameter is characterized but not 100% tested.

Switching Waveforms

Figure 8. Read Cycle Timing 1 ( $\overline{CE}$  low,  $\overline{OE}$  low)

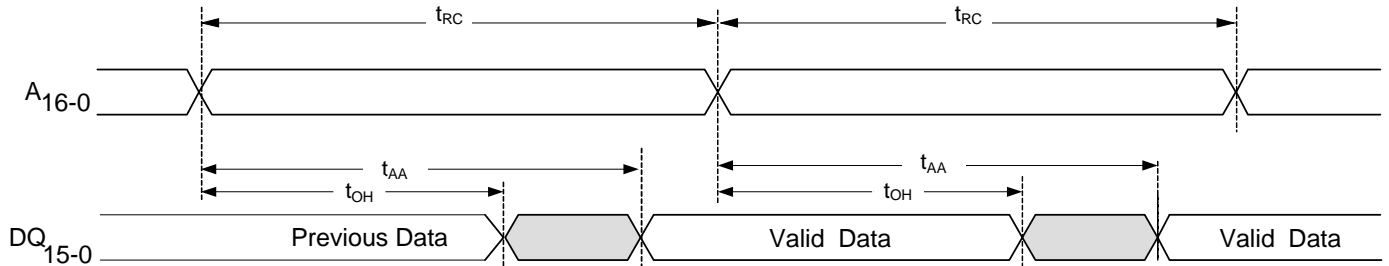


Figure 9. Read Cycle Timing 2 ( $\overline{CE}$  Controlled)

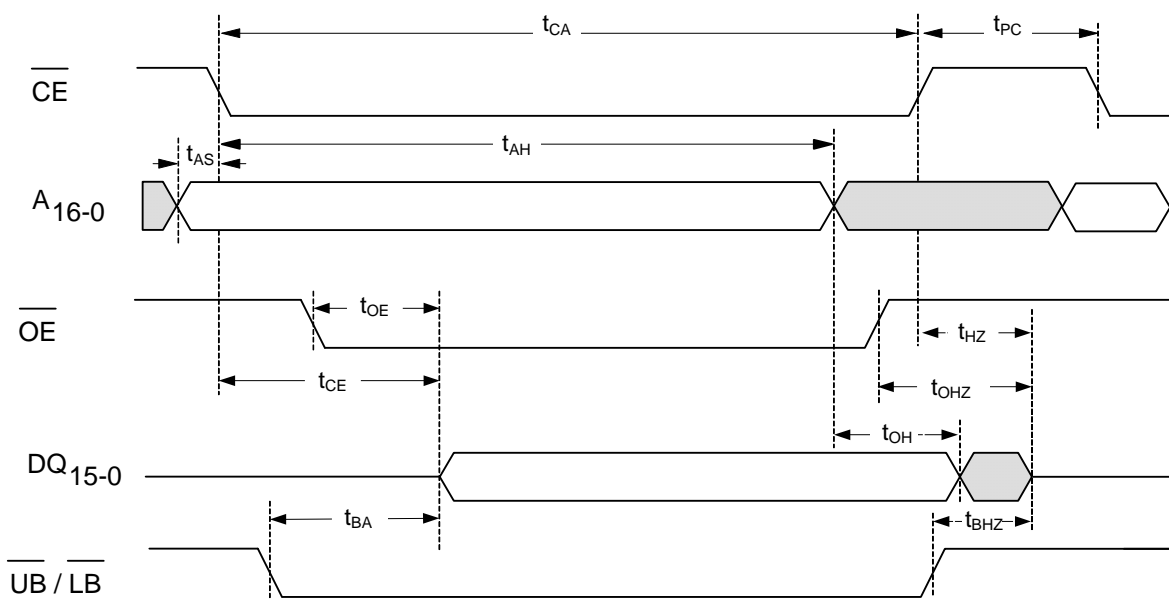
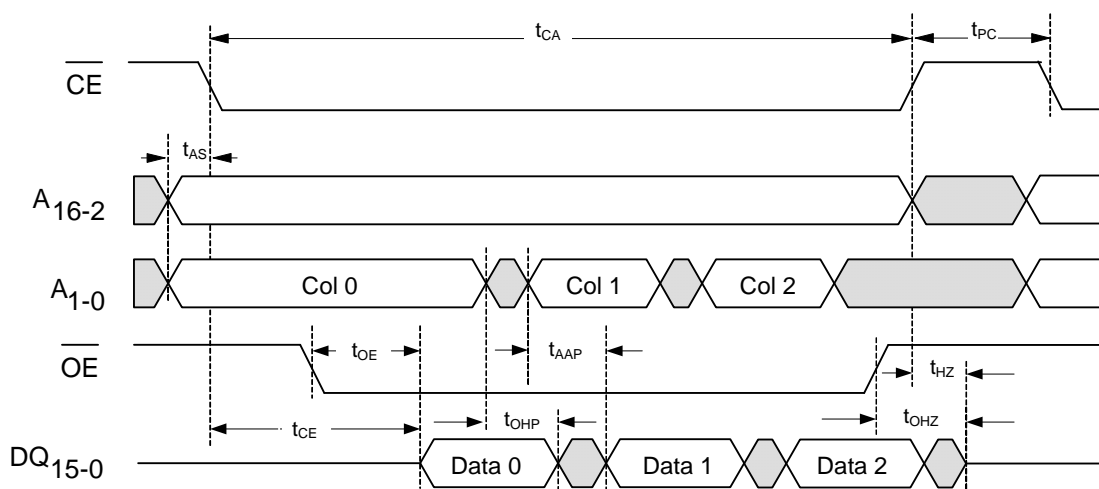


Figure 10. Page Mode Read Cycle Timing [8]



Note

8. Although sequential column addressing is shown, it is not required

Switching Waveforms (continued)

Figure 11. Write Cycle Timing 1 ( $\overline{\text{WE}}$  Controlled) [9]

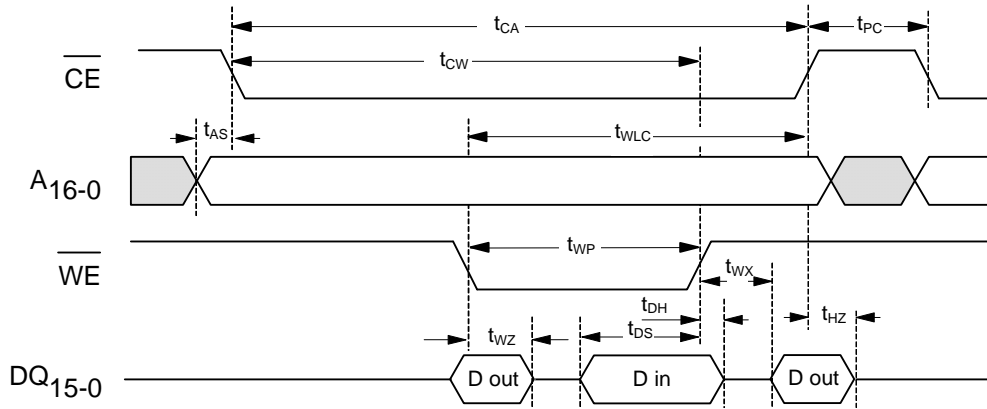


Figure 12. Write Cycle Timing 2 ( $\overline{\text{CE}}$  Controlled)

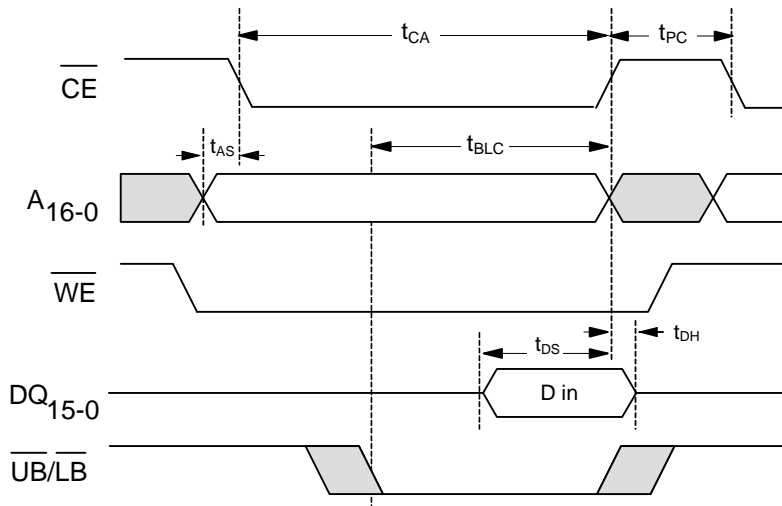
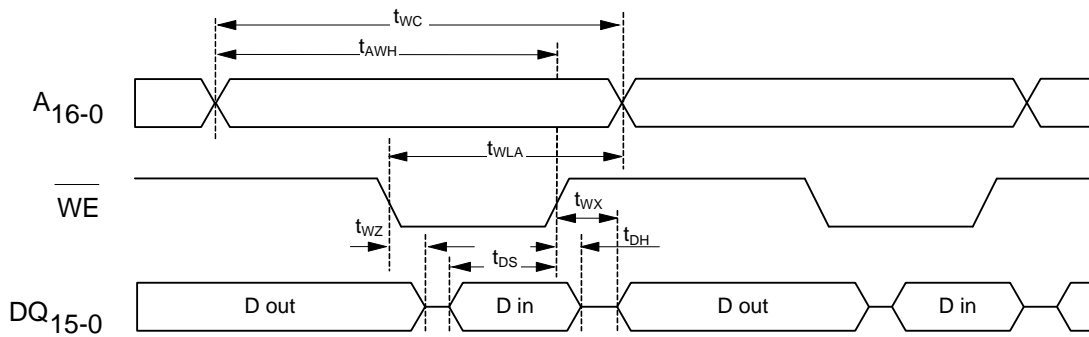


Figure 13. Write Cycle Timing 3 ( $\overline{\text{CE}}$  Low) [9]



Note

9.  $\overline{\text{OE}}$  (not shown) is low only to show effect of  $\overline{\text{WE}}$  on DQ pins.

Switching Waveforms (continued)

Figure 14. Write Cycle Timing 4 ( $\overline{\text{CE}}$  Low) <sup>[10]</sup>

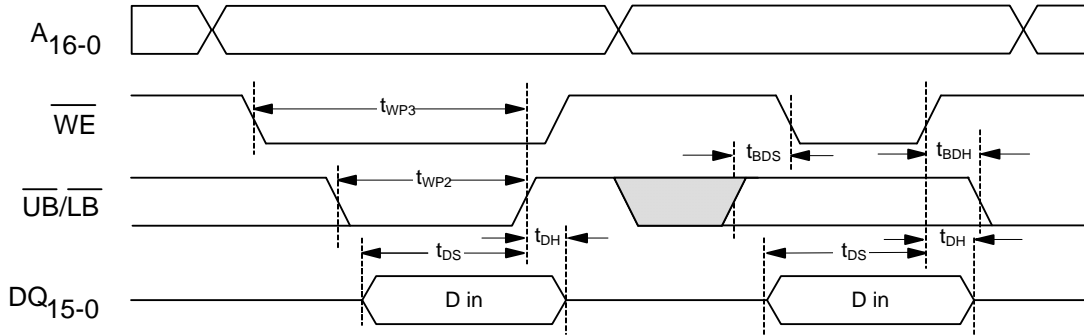
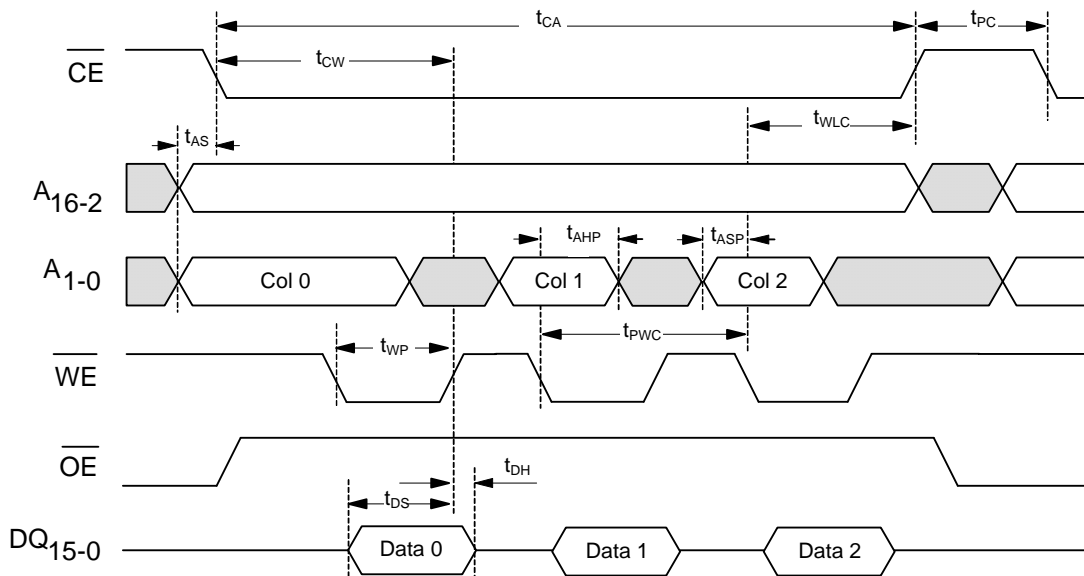


Figure 15. Page Mode Write Cycle Timing



Note  
10.  $\overline{\text{UB}}$  and  $\overline{\text{LB}}$  to show byte enable and byte masking cases.

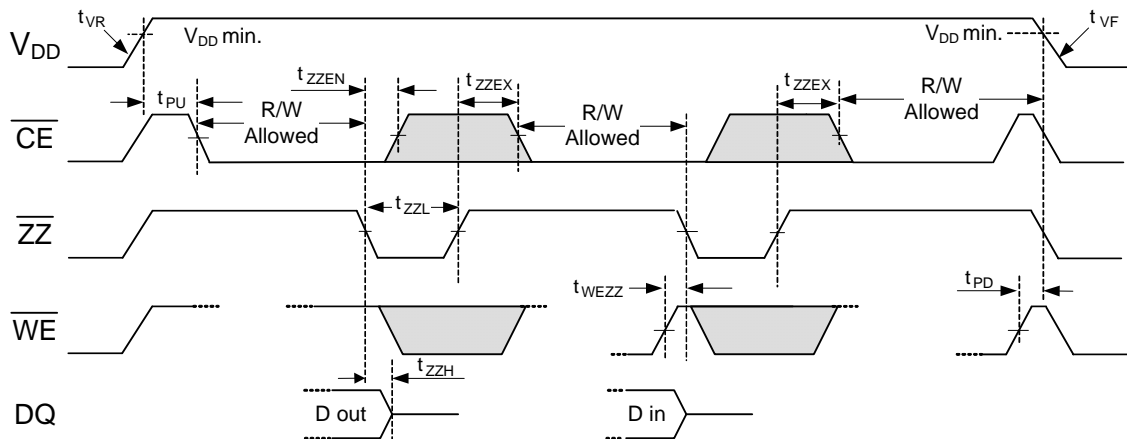
## Power Cycle and Sleep Mode Timing

Over the [Operating Range](#)

Parameter	Description	Min	Max	Unit
$t_{PU}$	Power-up (after $V_{DD}$ min. is reached) to first access time	1	–	ms
$t_{PD}$	Last write ( $\overline{WE}$ high) to power down time	0	–	ms
$t_{VR}^{[11]}$	$V_{DD}$ power-up slew rate	50	–	$\mu\text{s/V}$
$t_{VF}^{[11]}$	$V_{DD}$ power-down slew rate	100	–	$\mu\text{s/V}$
$t_{ZZH}$	$\overline{ZZ}$ active to DQ HI-Z time	–	20	ns
$t_{WEZZ}$	Last write to sleep mode entry time	0	–	$\mu\text{s}$
$t_{ZZL}$	$\overline{ZZ}$ active low time	1	–	$\mu\text{s}$
$t_{ZZEN}$	Sleep mode entry time ( $\overline{ZZ}$ low to $\overline{CE}$ don't care)	–	0	$\mu\text{s}$
$t_{ZZEX}$	Sleep mode exit time ( $\overline{ZZ}$ high to 1 <sup>st</sup> access after wakeup)	–	450	$\mu\text{s}$

## Switching Waveform

Figure 16. Power Cycle and Sleep Mode Timing



**Note**

11. Slope measured at any point on  $V_{DD}$  waveform.

**Functional Truth Table**

$\overline{CE}$	$\overline{WE}$	A <sub>16-2</sub>	A <sub>1-0</sub>	$\overline{ZZ}$	Operation <sup>[12, 13]</sup>
X	X	X	X	L	Sleep Mode
H	X	X	X	H	Standby/Idle
↓ L	H H	V V	V V	H H	Read
L	H	No Change	Change	H	Page Mode Read
L	H	Change	V	H	Random Read
↓ L	L L	V V	V V	H H	$\overline{CE}$ -Controlled Write <sup>[13]</sup>
L	↓	V	V	H	$\overline{WE}$ -Controlled Write <sup>[13, 14]</sup>
L	↓	No Change	V	H	Page Mode Write <sup>[15]</sup>
↑ L	X X	X X	X X	H H	Starts Pre-charge

**Byte Select Truth Table**

$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Operation <sup>[16]</sup>
H	H	X	X	Read; Outputs Disabled
	X	H	H	
H	L	H	L	Read upper byte; HI-Z lower byte
		L	H	Read lower byte; HI-Z upper byte
		L	L	Read both bytes
L	X	H	L	Write upper byte; Mask lower byte
		L	H	Write lower byte; Mask upper byte
		L	L	Write both bytes

**Notes**

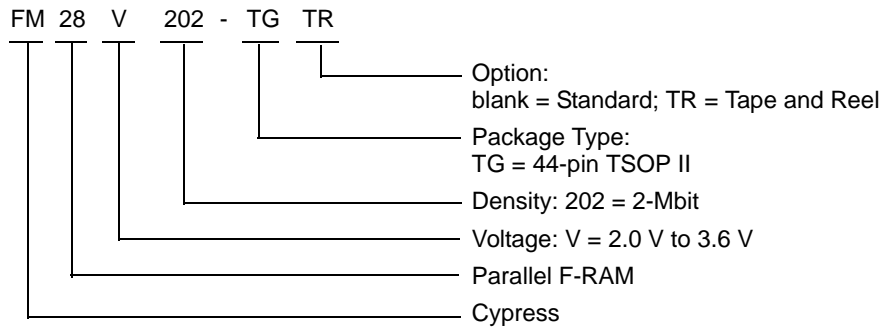
- 12. H = Logic High, L = Logic Low, V = Valid Data, X = Don't Care, ↓ = toggle low, ↑ = toggle high.
- 13. For write cycles, data-in is latched on the rising edge of CE or WE, whichever comes first.
- 14. WE-controlled write cycle begins as a Read cycle and then A<sub>16-2</sub> is latched.
- 15. Addresses A<sub>1-0</sub> must remain stable for at least 15 ns during page mode operation.
- 16. The UB and LB pins may be grounded if 1) the system does not perform byte writes and 2) the device is not configured as a 256K x 8.

**Ordering Information**

Access time (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
60	FM28V202-TG	51-85087	44-pin TSOP II with software WP, sleep mode	Industrial
	FM28V202-TGTR	51-85087		

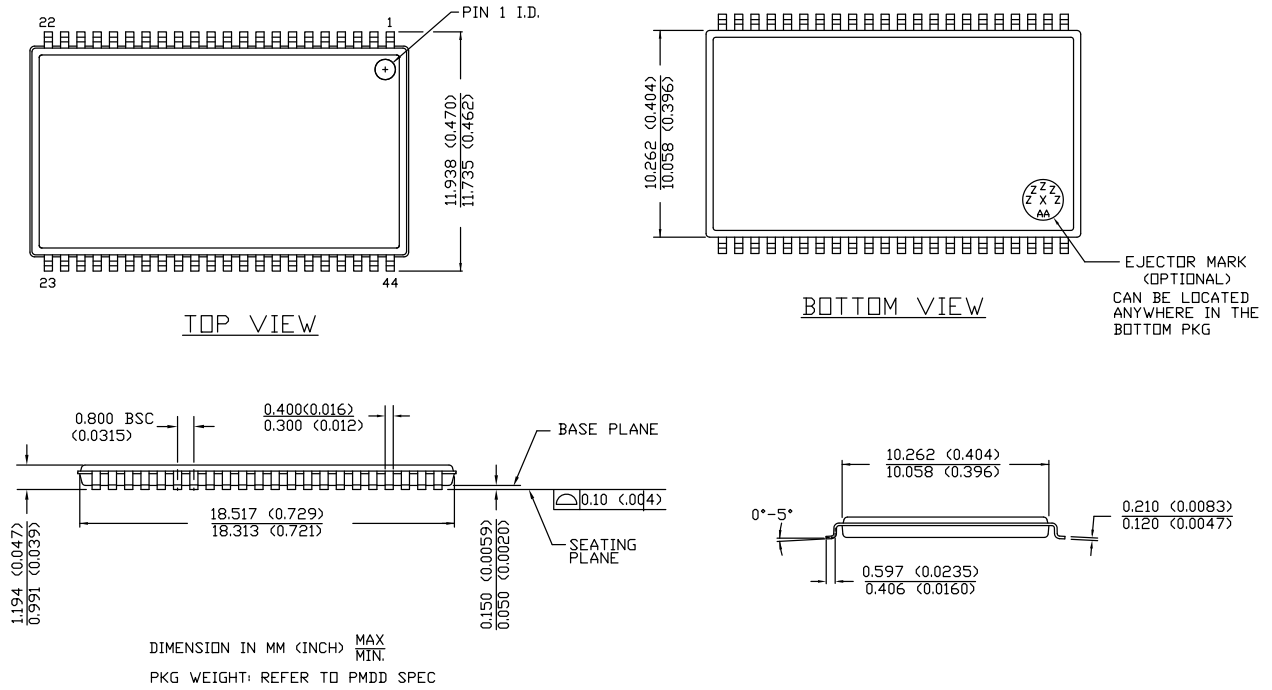
All the above parts are Pb-free.

**Ordering Code Definitions**



**Package Diagram**

**Figure 17. 44-pin TSOP Z44-II Package Outline, 51-85087**



51-85087 \*E

**Acronyms**

Acronym	Description
UB	upper byte
LB	lower byte
CE	chip enable
CMOS	complementary metal oxide semiconductor
EIA	Electronic Industries Alliance
F-RAM	ferroelectric random access memory
I/O	input/output
OE	output enable
RoHS	restriction of hazardous substances
RW	read and write
SRAM	static random access memory
TSOP	thin small outline package
WE	write enable

**Document Conventions**

**Units of Measure**

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
μA	microampere
μF	microfarad
μs	microsecond
mA	milliampere
ms	millisecond
MΩ	megaohm
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

**Document History Page**

Document Title: FM28V202, 2-Mbit (128 K × 16) F-RAM Memory				
Document Number: 001-86602				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	3930342	GVCH	03/12/2013	New spec.
*A	4043471	GVCH	06/28/2013	Added 48-ball FBGA package
*B	4123023	GVCH	09/20/2013	Converted source from word file to frame maker file.
*C	4136685	GVCH	10/01/2013	Removed 48-ball FBGA package Updated min values for $t_{WP}$ from 20 ns to 22 ns for $V_{DD} = 2.0$ V to 2.7 V and 30 ns to 18 ns for $V_{DD} = 2.7$ V to 3.6 V. Modified the description for $t_{VR}$ and $t_{VF}$ parameters for clarity.

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