FM24V05

512Kb Serial 3V F-RAM Memory

Features

512K bit Ferroelectric Nonvolatile RAM

- Organized as 65,536 x 8 bits
- High Endurance 100 Trillion (10^{14}) Read/Writes
- 10 year Data Retention
- NoDelay™ Writes
- Advanced High-Reliability Ferroelectric Process

Fast Two-wire Serial Interface

- Up to 3.4 MHz maximum bus frequency
- Direct hardware replacement for EEPROM
- Supports legacy timing for 100 kHz & 400 kHz

Device ID

- Device ID reads out Manufacturer ID & Part ID

Low Voltage, Low Power Operation

- Low Voltage Operation 2.0V – 3.6V
- Active Current < 150 µA (typ. @ 100KHz)
- 90 µA Standby Current (typ.)
- 5 µA Sleep Mode Current (typ.)

Industry Standard Configuration

- Industrial Temperature -40° C to +85° C
- 8-pin "Green"/RoHS SOIC Package

Description

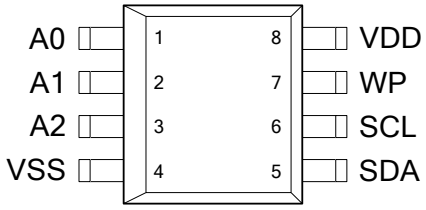
The FM24V05 is a 512Kbit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or F-RAM is nonvolatile and performs reads and writes like a RAM. It provides reliable data retention for 10 years while eliminating the complexities, overhead, and system level reliability problems caused by EEPROM and other nonvolatile memories.

The FM24V05 performs write operations at bus speed. No write delays are incurred. The next bus cycle may commence immediately without the need for data polling. In addition, the product offers write endurance orders of magnitude higher than EEPROM. Also, F-RAM exhibits much lower power during writes than EEPROM since write operations do not require an internally elevated power supply voltage for write circuits.

These capabilities make the FM24V05 ideal for nonvolatile memory applications requiring frequent or rapid writes. Examples range from data collection where the number of write cycles may be critical, to demanding industrial controls where the long write time of EEPROM can cause data loss. The combination of features allows more frequent data writing with less overhead for the system.

The FM24V05 provides substantial benefits to users of serial EEPROM, yet these benefits are available in a hardware drop-in replacement. The devices are available in industry standard 8-pin SOIC package using a familiar two-wire (I^2C) protocol. Both devices incorporate a read-only Device ID that allows the host to determine the manufacturer, product density, and product revision. The devices are guaranteed over an industrial temperature range of -40°C to +85°C.

Pin Configuration



Pin Name	Function
A0-A2	Device Select Address
SDA	Serial Data/address
SCL	Serial Clock
WP	Write Protect
VDD	Supply Voltage
VSS	Ground

This product conforms to specifications per the terms of the Ramtron standard warranty. The product has completed Ramtron's internal qualification testing and has reached production status.

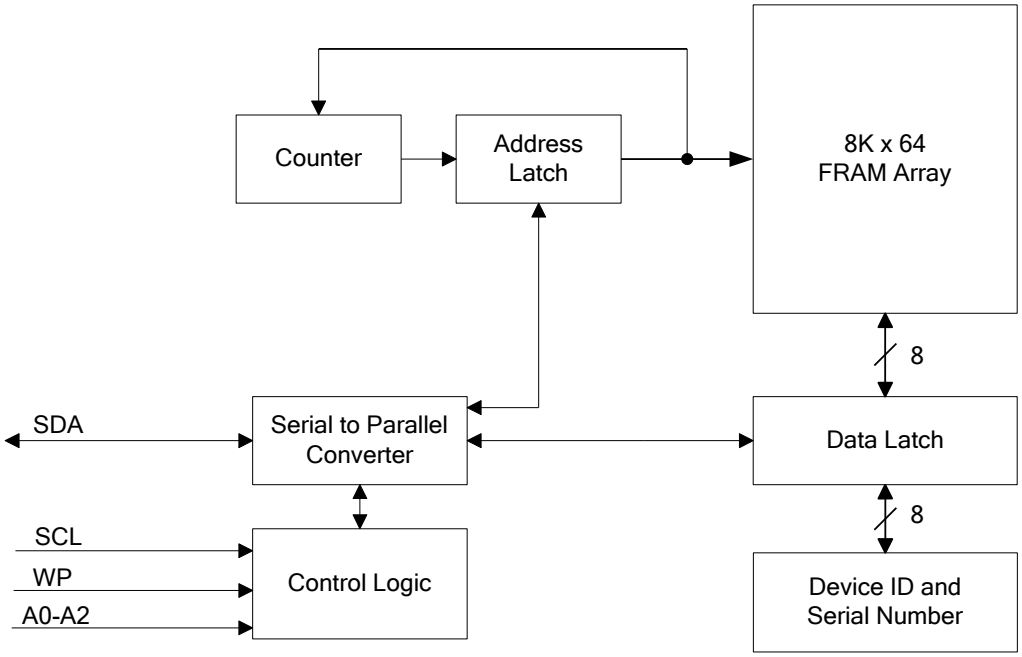


Figure 1. FM24V05 Block Diagram

Pin Description

Pin Name	Type	Pin Description
A0-A2	Input	Device Select Address 0-2: These pins are used to select one of up to 8 devices of the same type on the same two-wire bus. To select the device, the address value on the two pins must match the corresponding bits contained in the slave address. The address pins are pulled down internally.
SDA	I/O	Serial Data/Address: This is a bi-directional pin for the two-wire interface. It is open-drain and is intended to be wire-OR'd with other devices on the two-wire bus. The input buffer incorporates a Schmitt trigger for noise immunity and the output driver includes slope control for falling edges. An external pull-up resistor is required.
SCL	Input	Serial Clock: The serial clock pin for the two-wire interface. Data is clocked out of the part on the falling edge, and into the device on the rising edge. The SCL input also incorporates a Schmitt trigger input for noise immunity.
WP	Input	Write Protect: When tied to VDD, addresses in the entire memory map will be write-protected. When WP is connected to ground, all addresses may be written. This pin is pulled down internally.
VDD	Supply	Supply Voltage
VSS	Supply	Ground

Overview

The FM24V05 is a family of serial F-RAM memory devices. The memory array is logically organized as a 65,536 x 8 bit memory array and is accessed using an industry standard two-wire (I^2C) interface. Functional operation of the F-RAM is similar to serial EEPROM. The major difference between the FM24V05 and serial EEPROM is F-RAM's superior write performance.

Memory Architecture

When accessing the FM24V05, the user addresses 65,536 locations each with 8 data bits. These data bits are shifted serially. The 65,536 addresses are accessed using the two-wire protocol, which includes a slave address (to distinguish other non-memory devices) and a 2-byte address. All 16 address bits are used by the decoder for accessing the memory.

The access time for memory operation is essentially zero beyond the time needed for the serial protocol. That is, the memory is read or written at the speed of the two-wire bus. Unlike an EEPROM, it is not necessary to poll the device for a ready condition since writes occur at bus speed. That is, by the time a new bus transaction can be shifted into the part, a write operation will be complete. This is explained in more detail in the interface section below.

Users expect several obvious system benefits from the FM24V05 due to its fast write cycle and high endurance as compared with EEPROM. However there are less obvious benefits as well. For example in a high noise environment, the fast-write operation is less susceptible to corruption than an EEPROM since it is completed quickly. By contrast, an EEPROM requiring milliseconds to write is vulnerable to noise during much of the cycle.

Note that it is the user's responsibility to ensure that V_{DD} is within datasheet tolerances to prevent incorrect operation.

Two-wire Interface

The FM24V05 employs a bi-directional two-wire bus protocol using few pins or board space. Figure 2 illustrates a typical system configuration using the FM24V05 in a microcontroller-based system. The industry standard two-wire bus is familiar to many users but is described in this section.

By convention, any device that is sending data onto the bus is the transmitter while the target device for this data is the receiver. The device that is controlling the bus is the master. The master is responsible for generating the clock signal for all operations. Any device on the bus that is being controlled is a slave. The FM24V05 always is a slave device.

The bus protocol is controlled by transition states in the SDA and SCL signals. There are four conditions including start, stop, data bit, or acknowledge. Figure 3 illustrates the signal conditions that specify the four states. Detailed timing diagrams are shown in the electrical specifications section.

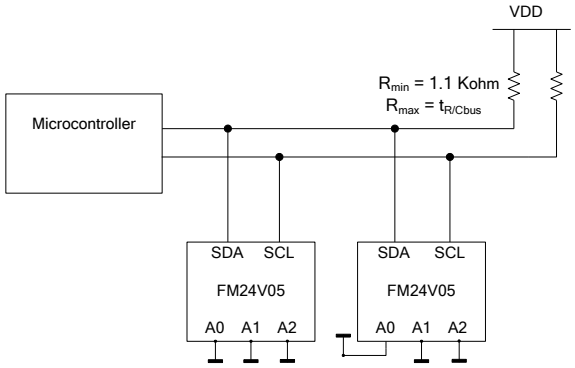


Figure 2. Typical System Configuration

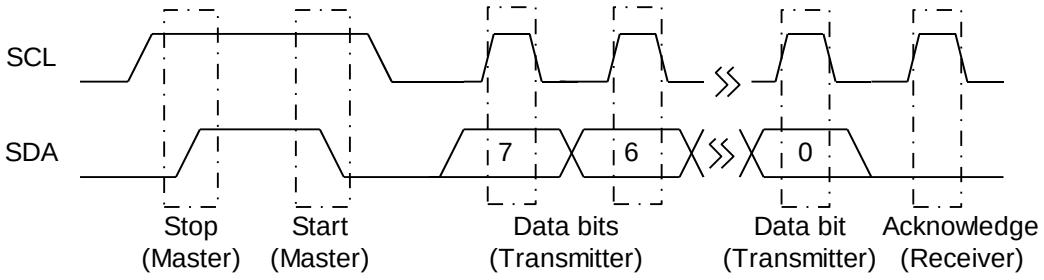


Figure 3. Data Transfer Protocol

Stop Condition

A stop condition is indicated when the bus master drives SDA from low to high while the SCL signal is high. All operations using the FM24V05 should end with a stop condition. If an operation is in progress when a stop is asserted, the operation will be aborted. The master must have control of SDA (not a memory read) in order to assert a stop condition.

Start Condition

A start condition is indicated when the bus master drives SDA from high to low while the SCL signal is high. All commands should be preceded by a start condition. An operation in progress can be aborted by asserting a start condition at any time. Aborting an operation using the start condition will ready the FM24V05 for a new operation.

If during operation the power supply drops below the specified V_{DD} minimum, the system should issue a start condition prior to performing another operation.

Data/Address Transfer

All data transfers (including addresses) take place while the SCL signal is high. Except under the two conditions described above, the SDA signal should not change while SCL is high.

Acknowledge

The acknowledge takes place after the 8th data bit has been transferred in any transaction. During this state the transmitter should release the SDA bus to allow the receiver to drive it. The receiver drives the SDA signal low to acknowledge receipt of the byte. If the receiver does not drive SDA low, the condition is a no-acknowledge and the operation is aborted.

The receiver would fail to acknowledge for two distinct reasons. First is that a byte transfer fails. In this case, the no-acknowledge ceases the current operation so that the part can be addressed again. This allows the last byte to be recovered in the event of a communication error.

Second and most common, the receiver does not acknowledge to deliberately end an operation. For example, during a read operation, the FM24V05 will continue to place data onto the bus as long as the receiver sends acknowledges (and clocks). When a read operation is complete and no more data is needed, the receiver must not acknowledge the last byte. If the receiver acknowledges the last byte, this will cause the FM24V05 to attempt to drive the bus on the next clock while the master is sending a new command such as stop.

Slave Address

The first byte that the FM24V05 expects after a start condition is the slave address. As shown in Figure 4, the slave address contains the device type or slave ID, the device select address bits, a page address bit, and a bit that specifies if the transaction is a read or a write.

Bits 7-4 are the device type (slave ID) and should be set to 1010b for the FM24V05. These bits allow other function types to reside on the 2-wire bus within an identical address range. Bits 3-1 are the device select address bits. They must match the corresponding value on the external address pins to select the device. Up to eight FM24V05 devices can reside on the same two-wire bus by assigning a different address to each. Bit 0 is the read/write bit. R/W=1 indicates a read operation and R/W=0 indicates a write operation.

High Speed Mode (HS-mode)

The FM24V05 supports a 3.4MHz high speed mode. A master code (0000 1XXXb) must be issued to place the device into high speed mode. Communication between master and slave will then be enabled for speeds up to 3.4MHz. A stop condition will exit HS-mode. Single- and multiple-byte reads and writes are supported. See Figures 10 and 11 for HS-mode timings.

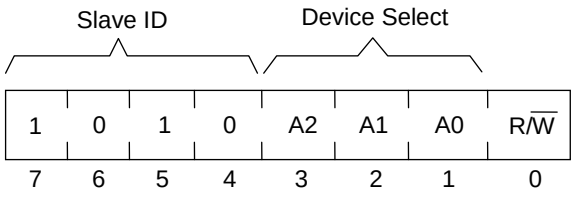


Figure 4. Slave Address

Addressing Overview

After the FM24V05 (as receiver) acknowledges the slave address, the master can place the memory address on the bus for a write operation. The address requires two bytes. The complete 16-bit address is latched internally. Each access causes the latched address value to be incremented automatically. The current address is the value that is held in the latch -- either a newly written value or the address following the last access. The current address will be held for as long as power remains or until a new value is written. Reads always use the current address. A random read address can be loaded by beginning a write operation as explained below.

After transmission of each data byte, just prior to the acknowledge, the FM24V05 increments the internal address latch. This allows the next sequential byte to be accessed with no additional addressing. After the last address (FFFFh) is reached, the address latch will roll over to 0000h. There is no limit to the number of bytes that can be accessed with a single read or write operation.

Data Transfer

After the address information has been transmitted, data transfer between the bus master and the FM24V05 can begin. For a read operation the FM24V05 will place 8 data bits on the bus then wait for an acknowledge from the master. If the acknowledge occurs, the FM24V05 will transfer the next sequential byte. If the acknowledge is not sent, the FM24V05 will end the read operation. For a write operation, the FM24V05 will accept 8 data bits from the master then send an acknowledge. All data transfer occurs MSB (most significant bit) first.

Memory Operation

The FM24V05 is designed to operate in a manner very similar to other 2-wire interface memory products. The major differences result from the higher performance write capability of F-RAM technology. These improvements result in some differences between the FM24V05 and a similar configuration EEPROM during writes. The complete operation for both writes and reads is explained below.

Write Operation

All writes begin with a slave address, then a memory address. The bus master indicates a write operation by setting the LSB of the slave address (R/W bit) to a '0'. After addressing, the bus master sends each byte of data to the memory and the memory generates an acknowledge condition. Any number of sequential bytes may be written. If the end of the address range is reached internally, the address counter will wrap from FFFFh to 0000h.

Unlike other nonvolatile memory technologies, there is no effective write delay with F-RAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory cycle occurs in less time than a single bus clock. Therefore, any operation including read or write can occur immediately following a write. Acknowledge polling, a technique used with EEPROMs to determine if a write is complete is unnecessary and will always return a ready condition.

Internally, an actual memory write occurs after the 8th data bit is transferred. It will be complete before the acknowledge is sent. Therefore, if the user desires to abort a write without altering the memory contents, this should be done using start or stop condition prior to the 8th data bit. The FM24V05 uses no page buffering.

The memory array can be write-protected using the WP pin. This feature is available only on FM24V05 devices. Setting the WP pin to a high condition (V_{DD}) will write-protect all addresses. The FM24V05 will not acknowledge data bytes that are written to protected addresses. In addition, the address counter will not increment if writes are attempted to these addresses. Setting WP to a low state (V_{SS}) will deactivate this feature. WP is pulled down internally.

Figures 5 and 6 below illustrate a single-byte and multiple-byte write cycles.

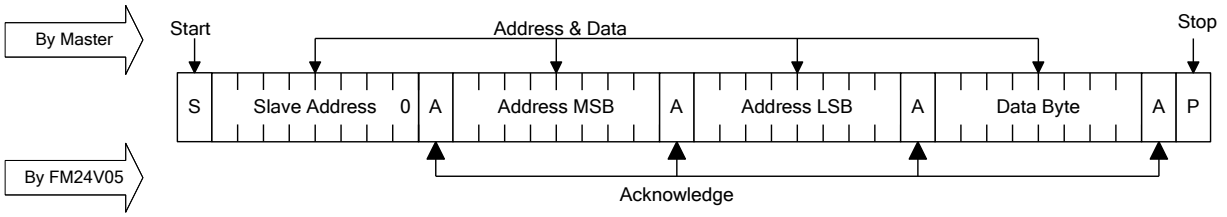


Figure 5. Single Byte Write

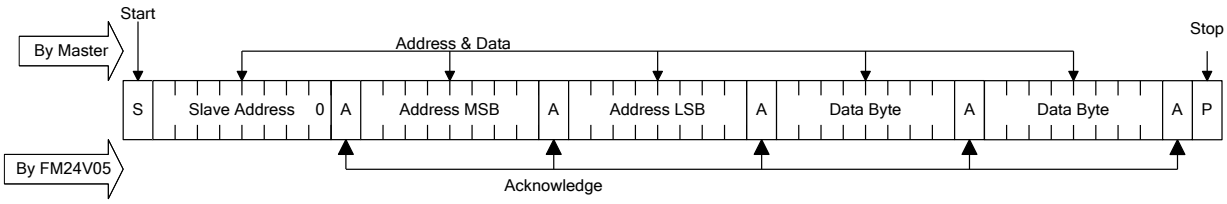


Figure 6. Multiple Byte Write

Read Operation

There are two basic types of read operations. They are current address read and selective address read. In a current address read, the FM24V05 uses the internal address latch to supply the address. In a selective read, the user performs a procedure to set the address to a specific value.

Current Address & Sequential Read

As mentioned above the FM24V05 uses an internal latch to supply the address for a read operation. A current address read uses the existing value in the address latch as a starting place for the read operation. The system reads from the address immediately following that of the last operation.

To perform a current address read, the bus master supplies a slave address with the LSB set to a '1'. This indicates that a read operation is requested. After receiving the complete slave address, the FM24V05 will begin shifting out data from the current address on the next clock. The current address is the value held in the internal address latch.

Beginning with the current address, the bus master can read any number of bytes. Thus, a sequential read is simply a current address read with multiple byte transfers. After each byte the internal address counter will be incremented.

Each time the bus master acknowledges a byte, this indicates that the FM24V05 should read out the next sequential byte.

There are four ways to properly terminate a read operation. Failing to properly terminate the read will most likely create a bus contention as the FM24V05 attempts to read out additional data onto the bus. The four valid methods are:

1. The bus master issues a no-acknowledge in the 9th clock cycle and a stop in the 10th clock cycle. This is illustrated in the diagrams below. This is preferred.
2. The bus master issues a no-acknowledge in the 9th clock cycle and a start in the 10th.
3. The bus master issues a stop in the 9th clock cycle.
4. The bus master issues a start in the 9th clock cycle.

If the internal address reaches FFFFh, it will wrap around to 0000h on the next read cycle. Figures 7 and 8 below show the proper operation for current address reads.

Selective (Random) Read

There is a simple technique that allows a user to select a random address location as the starting point for a read operation. This involves using the first three bytes of a write operation to set the internal address followed by subsequent read operations.

To perform a selective read, the bus master sends out the slave address with the LSB set to 0. This specifies a write operation. According to the write protocol, the bus master then sends the address bytes that are loaded into the internal address latch. After the FM24V05 acknowledges the address, the bus master issues a start condition. This simultaneously aborts

the write operation and allows the read command to be issued with the slave address LSB set to a '1'. The operation is now a current address read.

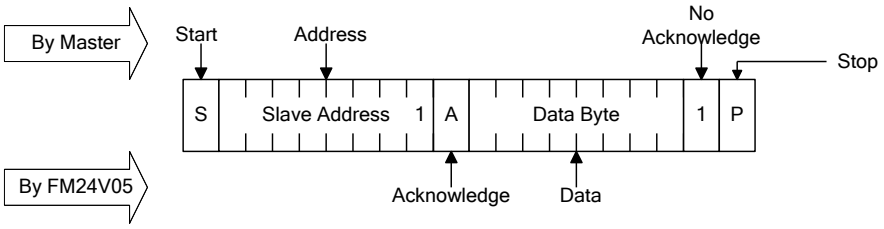


Figure 7. Current Address Read

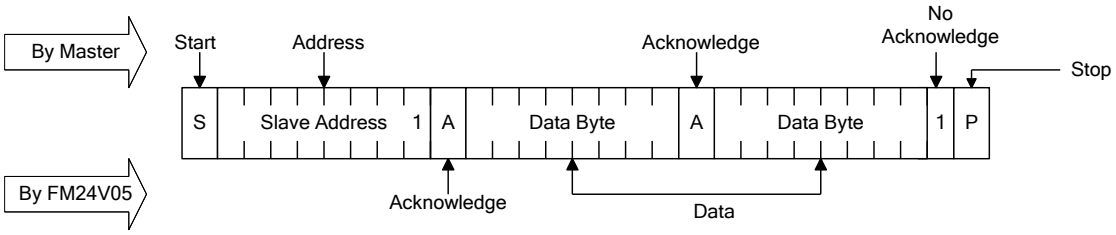


Figure 8. Sequential Read

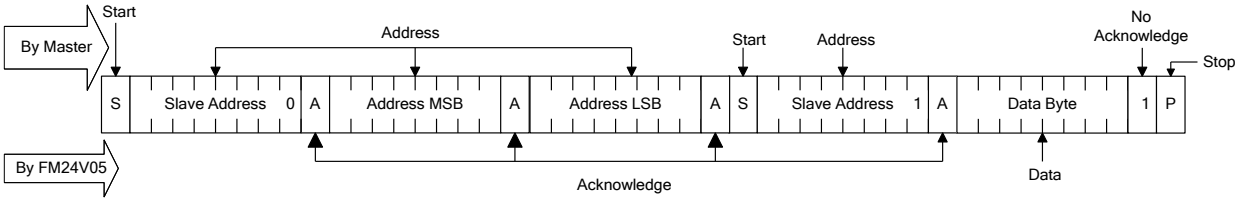


Figure 9. Selective (Random) Read

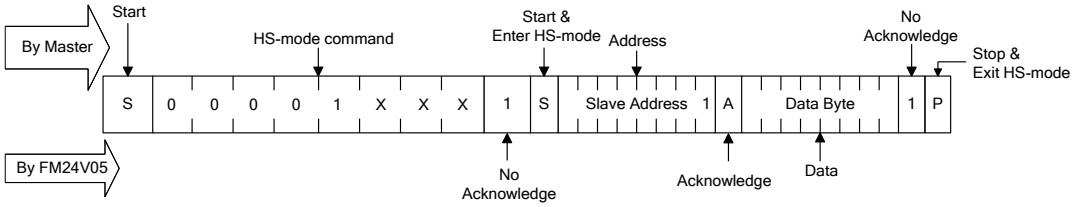


Figure 10. HS-mode Current Address Read

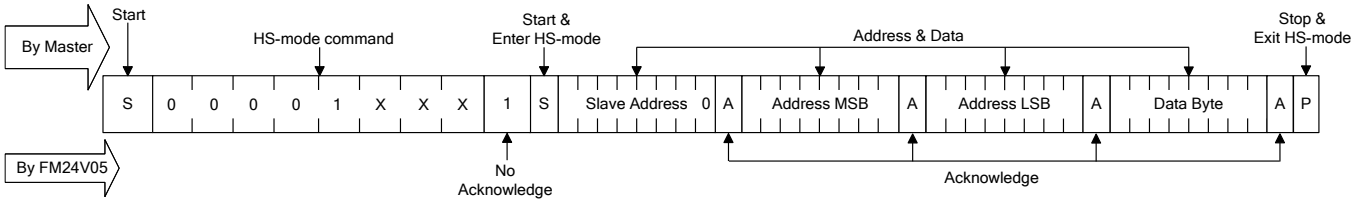


Figure 11. HS-mode Byte Write

Sleep Mode

A low power mode called Sleep Mode is implemented on both FM24V05 devices. The device will enter this low power state when the Sleep command 86h is clocked-in. Sleep Mode entry can be entered as follows:

1. The master sends a START command.
2. The master sends Reserved Slave ID 0xF8
3. The master sends the I^2C-bus slave address of the slave device it needs to identify. The last bit is a 'Don't care' value (R/W bit). Only one device must acknowledge this byte (the one that has the I^2C-bus slave address).
4. The master sends a Re-START command.
5. The master sends Reserved Slave ID 0x86
6. The FM24V05 sends an ACK.
7. The master sends STOP to ensure the device enters sleep mode.

Once in sleep mode, the device draws I_{ZZ} current, but the device continues to monitor the I^2C pins. Once the master sends a Slave Address that the FM24V05 identifies, it will "wakeup" and be ready for normal operation within t_{REC} (400 µs max.). As an alternative method of determining when the device is ready, the master can send read or write commands and look for an ACK. While the device is waking up, it will NACK the master until it is ready.

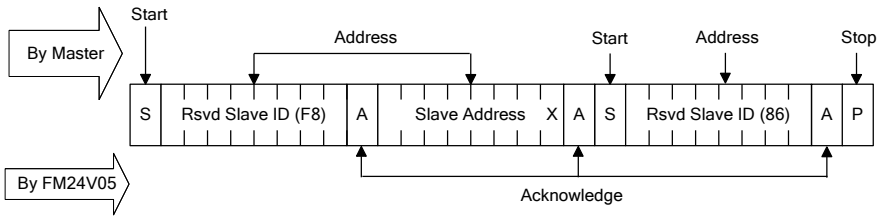


Figure 12. Sleep Mode Entry

Device ID

The FM24V05 devices incorporate a means of identifying the device by providing three bytes of data, which are manufacturer, product ID, and die revision. The Device ID is read-only. It can be accessed as follows:

1. The master sends a START command.
2. The master sends Reserved Slave ID 0xF8
3. The master sends the I^2C-bus slave address of the slave device it needs to identify. The last bit is a 'Don't care' value (R/W bit). Only one device must acknowledge this byte (the one that has the I^2C-bus slave address).
4. The master sends a Re-START command.
5. The master sends Reserved Slave ID 0xF9
6. The Device ID Read can be done, starting with the 12 manufacturer bits, followed by the 9 part identification bits, and then the 3 die revision bits.
7. The master ends the Device ID read sequence by NACKing the last byte, thus resetting the slave device state machine and allowing the master to send the STOP command.

Note: The reading of the Device ID can be stopped anytime by sending a NACK command.

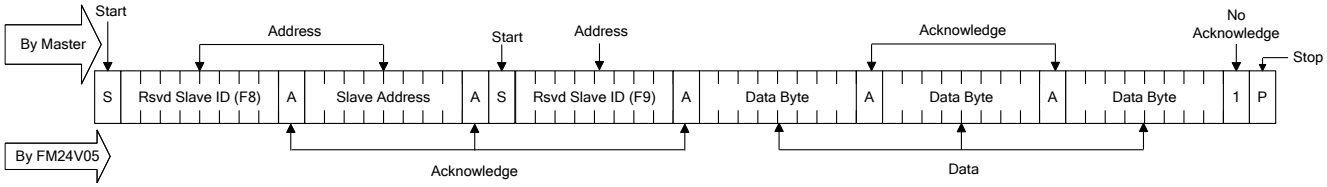


Figure 13. Read Device ID

Manufacturer ID												Product ID									Die Rev.		
11	10	9	8	7	6	5	4	3	2	1	0	8	7	6	5	4	3	2	1	0	2	1	0
Ramtron												Density				Variation							
0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	N	0	0	0	0	0	0	0

Figure 14. Manufacturer and Product ID

Density: 01h=128Kb, 02h=256Kb, 03h=512Kb, 04=1Mb
Variation: Product ID bit 4 = S/N, Product ID bit 0 = reserved

The 3-byte hex code for an FM24V05 will be: `0x00 0x43 0x00`

Electrical Specifications

Absolute Maximum Ratings

Symbol	Description	Ratings
V_{DD}	Power Supply Voltage with respect to V_{SS}	-1.0V to +4.5V
V_{IN}	Voltage on any pin with respect to V_{SS}	-1.0V to +4.5V and $V_{IN} < V_{DD}$+1.0V *
T_{STG}	Storage Temperature	-55°C to +125°C
T_{LEAD}	Lead Temperature (Soldering, 10 seconds)	260° C
V_{ESD}	Electrostatic Discharge Voltage - Human Body Model (AEC-Q100-002 Rev. E) - Charged Device Model (AEC-Q100-011 Rev. B) - Machine Model (AEC-Q100-003 Rev. E)	 2.5kV 1.25kV 200V
	Package Moisture Sensitivity Level	MSL-1

* Exception: The "$V_{IN} < V_{DD}$+1.0V" restriction does not apply to the SCL and SDA inputs.
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC Operating Conditions (T_A = -40° C to + 85° C, V_{DD} =2.0V to 3.6V unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Main Power Supply	2.0	3.3	3.6	V	
I_{DD}	V_{DD} Supply Current @ SCL = 100 kHz @ SCL = 1 MHz @ SCL = 3.4 MHz			 175 400 1000	 µA µA µA	1
I_{SB}	Standby Current		90	150	µA	2
I_{ZZ}	Sleep Mode Current		5	8	µA	2
I_{LI}	Input Leakage Current			±1	µA	3
I_{LO}	Output Leakage Current			±1	µA	3
V_{IL}	Input Low Voltage	-0.3		0.3 V_{DD}	V	
V_{IH}	Input High Voltage	0.7 V_{DD}		V_{DD} + 0.3	V	
V_{OL1}	Output Low Voltage (I_{OL} = 2 mA, $V_{DD} \geq$ 2.7V)			0.4	V	
V_{OL2}	Output Low Voltage (I_{OL} = 150 µA)			0.2	V	
R_{IN}	Address Input Resistance (WP, A2-A0) For $V_{IN} = V_{IL}$ (max) For $V_{IN} = V_{IH}$ (min)	 50 1			 KΩ MΩ	4

Notes
1. SCL toggling between V_{DD}-0.2V and V_{SS}, other inputs V_{SS} or V_{DD}-0.2V.
2. SCL = SDA = V_{DD}. All inputs V_{SS} or V_{DD}. Stop command issued.
3. VIN or VOUT = V_{SS} to V_{DD}. Does not apply to WP, A2-A0 pins.
4. The input pull-down circuit is stronger (50KΩ) when the input voltage is below V_{IL} and weak (1MΩ) when the input voltage is above V_{IH}.

AC Parameters (T_A = -40° C to + 85° C, V_{DD} =2.0V to 3.6V unless otherwise specified)

Symbol	Parameter	F/S-mode (C_L<500pF)		HS-mode (C_L<100pF)		Units	Notes
		Min	Max	Min	Max		
f_{SCL}	SCL Clock Frequency	0	1.0	0	3.4	MHz	1
t_{LOW}	Clock Low Period	500		160		ns	
t_{HIGH}	Clock High Period	260		60		ns	
t_{AA}	SCL Low to SDA Data Out Valid		450		130	ns	
t_{BUF}	Bus Free Before New Transmission	0.5		0.3		µs	
$t_{HD:STA}$	Start Condition Hold Time	260		160		ns	
$t_{SU:STA}$	Start Condition Setup for Repeated Start	260		160		ns	
$t_{HD:DAT}$	Data In Hold	0		0		ns	
$t_{SU:DAT}$	Data In Setup	50		10		ns	3
t_R	Input Rise Time		120		80	ns	2
t_F	Input Fall Time		120		80	ns	2
$t_{SU:STO}$	Stop Condition Setup	260		160		ns	
t_{DH}	Data Output Hold (from SCL @ V_{IL})	0		0		ns	
t_{SP}	Noise Suppression Time Constant on SCL, SDA		50		5	ns	

Notes: All SCL specifications as well as start and stop conditions apply to both read and write operations.
1. The speed-related specifications are guaranteed characteristic points along a continuous curve of operation from DC to f_{SCL} (max).
2. This parameter is periodically sampled and not 100% tested.
3. In HS-mode and V_{DD} < 2.7V, the $t_{SU:DAT}$ (min.) spec is 15ns.

Capacitance (T_A = 25° C, f=1.0 MHz, V_{DD} = 3.3V)

Symbol	Parameter	Min	Max	Units	Notes
$C_{I/O}$	Input/Output Capacitance (SDA)	-	8	pF	1
C_{IN}	Input Capacitance	-	6	pF	1

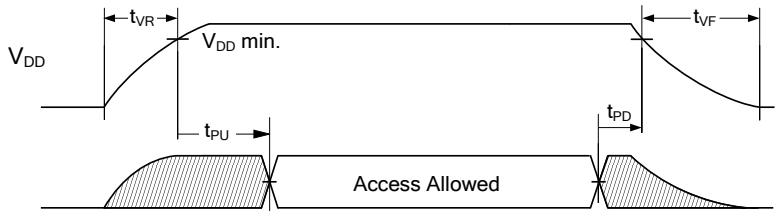
Notes
1. This parameter is periodically sampled and not 100% tested.

Power Cycle Timing (T_A = -40° C to +85° C, V_{DD} = 2.0V to 3.6V)

Symbol	Parameter	Min	Max	Units	Notes
t_{VR}	V_{DD} Rise Time	50	-	µs/V	1,2
t_{VF}	V_{DD} Fall Time	100	-	µs/V	1,2
t_{PU}	Power Up (V_{DD} min) to First Access (Start condition)	250	-	µs	
t_{PD}	Last Access (Stop condition) to Power Down (V_{DD} min)	0	-	µs	
t_{REC}	Recovery Time from Sleep Mode	-	400	µs	

Notes
1. This parameter is characterized and not 100% tested.
2. Slope measured at any point on V_{DD} waveform.

Power Cycle Timing



AC Test Conditions

Input Pulse Levels	0.1 V_{DD} to 0.9 V_{DD}
Input rise and fall times	10 ns
Input and output timing levels	0.5 V_{DD}

Equivalent AC Test Load Circuit

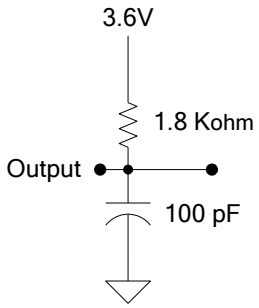
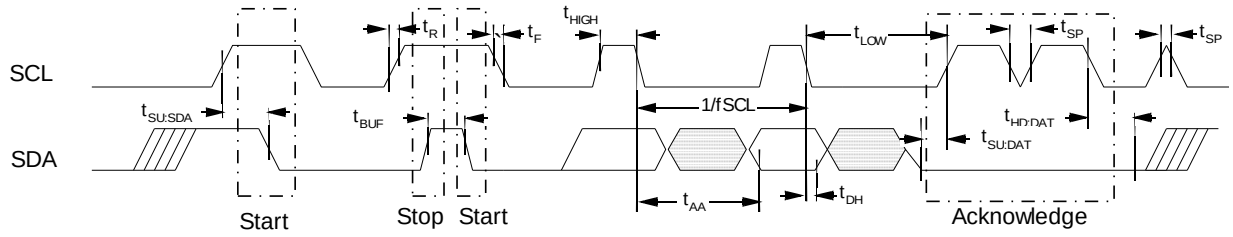


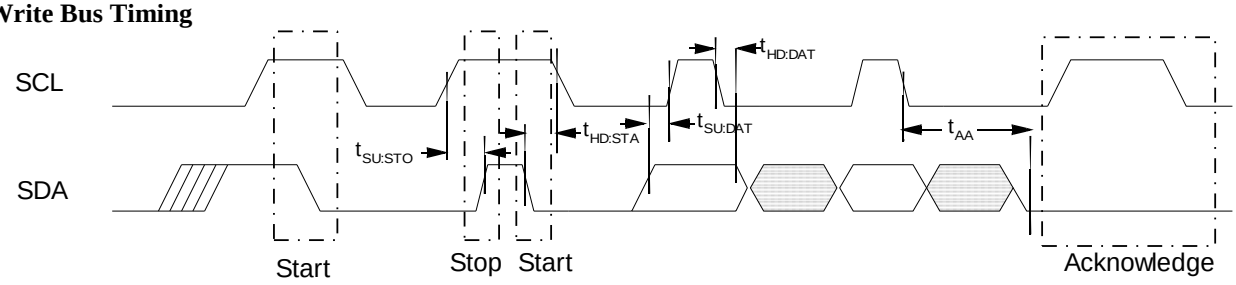
Diagram Notes

All start and stop timing parameters apply to both read and write cycles. Clock specifications are identical for read and write cycles. Write timing parameters apply to slave address, word address, and write data bits. Functional relationships are illustrated in the relevant datasheet sections. These diagrams illustrate the timing parameters only.

Read Bus Timing



Write Bus Timing

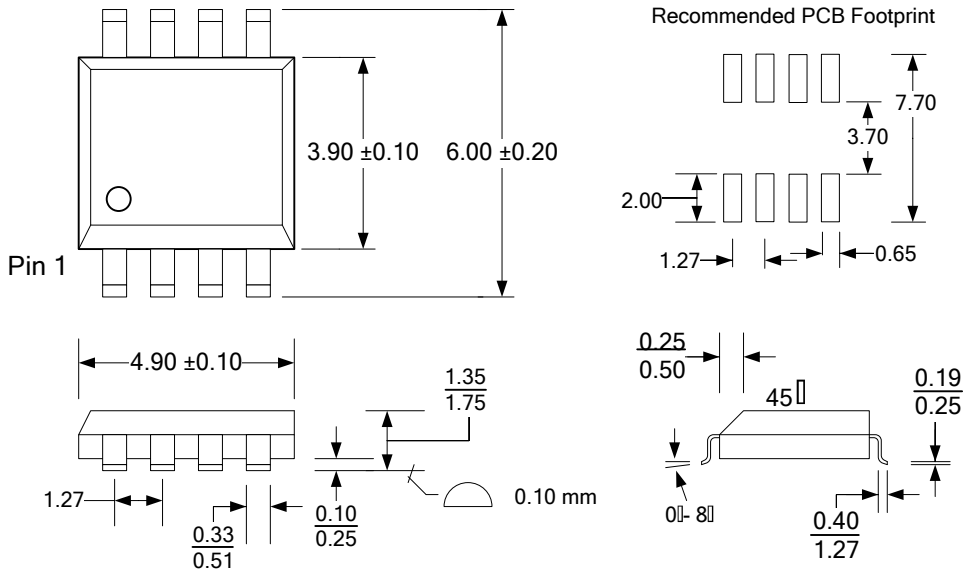


Data Retention (T_A = -40° C to +85° C)

Parameter	Min	Max	Units	Notes
Data Retention	10	-	Years	

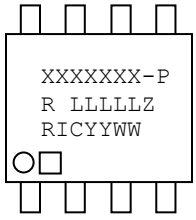
Mechanical Drawing

8-pin SOIC (JEDEC Standard MS-012 variation AA)



Refer to JEDEC MS-012 for complete dimensions and notes.
All dimensions in millimeters.

SOIC Package Marking Scheme



Legend:
XXXXXXX = part number, P = package type
R = rev code, LLLLL = lot code, Z = Package code
RIC = Ramtron Int'l Corp, YY = year, WW = work week
□ = Pb-free

Example:
FM24V05, "Green"/RoHS SOIC
Rev. A, Lot 67989, SOIC
Year 2013, Work Week 07
Pb-free

FM24V05-G
A 67989S
RIC1307
□

Revision History

Revision	Date	Summary
1.0	8/22/2008	Initial Release
1.1	2/2/2009	Added tape and reel ordering information.
2.0	5/25/2010	Changed to Pre-Production status. Updated ESD ratings. Changed part marking scheme. Expanded CRC check description.
2.1	11/22/2011	Removed S/N option.
3.0	1/30/2012	Changed to Production status.

Ordering Information

Part Number	Features	Operating Voltage	Package
FM24V05-G	Device ID	2.0-3.6V	8-pin “Green”/RoHS SOIC
FM24V05-GTR	Device ID	2.0-3.6V	8-pin “Green”/RoHS SOIC, Tape & Reel

Appendix A - Errata for FM24V05

Errata Number 001

Date January 12, 2011 (Updated Jan. 2012)

Product FM24V05

The FM24V05 devices have a problem with the sleep mode function. Some devices will not exit sleep at Vdd voltages within the specified operating range. Worst case is at high V_{DD} (3.6V). The failing voltage will be lower at cold temperatures. This does not affect operation if the sleep function is not used.

There is an effective screen that is implemented at final test. A temporary part number has been assigned for customers who use sleep mode. Customers who require sleep mode should order the FM24V05-G. The part will be marked with a triangle to the right of the part mark. An example of the mark is as follows:

No Sleep Mode Screen
FM24V05-G
A9646447
RIC1011

Sleep Mode Screen
FM24V05-G
A9646447 △
RIC1011

This errata will remain in effect until the sleep function is fixed.

UPDATE: Ramtron has implemented a screen such that all devices comply with the datasheet specifications without exception over all operating temperature and voltage conditions. Therefore the above errata no longer applies. The starting date code for errata-free devices is 1204. (YY=12, WW=04)

Document History

Document Title: FM24V05 512Kb Serial 3V F-RAM Memory
Document Number: 001-84462

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3902204	GVCH	02/25/2013	New Spec
*A	3985098	GVCH	05/09/2013	Removed FM24VN05 part number related information Updated SOIC package marking scheme
*B	4014247	GVCH	05/29/2013	Added Appendix A - Errata for FM24V05

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