CMF20120D-Silicon Carbide Power MOSFET
1200V 80 mΩ

Z-FET™ MOSFET

N-Channel Enhancement Mode

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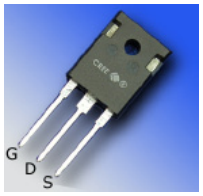
V_{DS}	= 1200 V
$R_{DS(on)}$	= 80 mΩ
$I_{D(MAX)}$@T_C=25°C	= 33 A

Features

- Industry Leading $R_{DS(on)}$
- High Speed Switching
- Low Capacitances
- Easy to Parallel
- Simple to Drive
- Pb-Free Plating, RoHS Compliant, Halogen Free

Package



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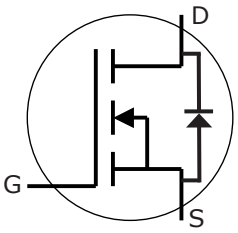

Benefits

- Higher System Efficiency
- Reduced Cooling Requirements
- Avalanche Ruggedness
- Increased System Switching Frequency

Part Number	Package
CMF20120D	TO-247-3

Applications

- Solar Inverters
- High Voltage DC/DC Converters
- Motor Drives

Maximum Ratings

Symbol	Parameter	Value	Unit	Test Conditions	Note
I_D	Continuous Drain Current	33	A	V_{GS}@20V, T_C = 25°C	
		17		V_{GS}@20V, T_C = 100°C	
I_{Dpulse}	Pulsed Drain Current	78	A	Pulse width t_P limited by T_{jmax} T_C = 25°C	
E_{AS}	Single Pulse Avalanche Energy	2.2	J	I_D = 20A, V_{DD} = 50 V, L = 9.5 mH	
E_{AR}	Repetitive Avalanche Energy	1.5	J	t_{AR} limited by T_{jmax}	
I_{AR}	Repetitive Avalanche Current	20	A	I_D = 20A, V_{DD} = 50 V, L = 3 mH t_{AR} limited by T_{jmax}	
V_{GS}	Gate Source Voltage	-5/+25	V		
P_{tot}	Power Dissipation	150	W	T_C=25°C	
T_J , T_{stg}	Operating Junction and Storage Temperature	-55 to +125	°C		
T_L	Solder Temperature	260	°C	1.6mm (0.063”) from case for 10s	
M_d	Mounting Torque	1 8.8	Nm lbf-in	M3 or 6-32 screw	

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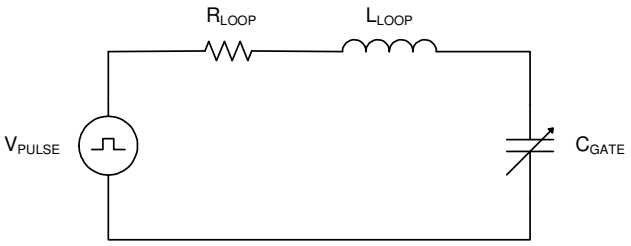
Applications Information

The Cree SiC MOSFET has removed the upper voltage limit of silicon MOSFETs. However, there are some differences in characteristics when compared to what is usually expected with high voltage silicon MOSFETs. These differences need to be carefully addressed to get maximum benefit from the SiC MOSFET. In general, although the SiC MOSFET is a superior switch compared to its silicon counterparts, it should not be considered as a direct drop-in replacement in existing applications.

There are two key characteristics that need to be kept in mind when applying the SiC MOSFETs: modest transconductance requires that V_{GS} needs to be 20 V to optimize performance. This can be see in the Output and Transfer Characteristics shown in Figures 1-3. The modest transconductance also affects the transition where the device behaves as a voltage controlled resistance to where it behaves as a voltage controlled current source as a funtion of $V_{DS.}$ The result is that the transition occurs over higher values of V_{DS} than are usually experienced with Si MOSFETs and IGBTs. This might affect the operation anti-desaturation circuits, especially if the circuit takes advantage of the device entering the constant current region at low values of forward voltage.

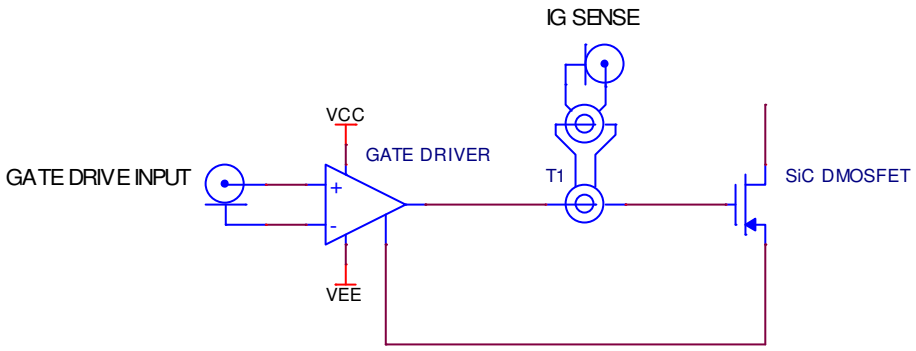
The modest transconductance needs to be carefully considered in the design of the gate drive circuit. The first obvious requirement is that the gate be capable of a >22 V (+20 V to -2V) swing. The recommended on state V_{GS} is +20 V and the recommended off state V_{GS} is between -2 V to -5 V. Please carefully note that although the gate voltage swing is higher than the typical silicon MOSFETs and IGBTs, the total gate charge of the SiC MOSFET is considerably lower. In fact, the product of gate voltage swing and gate charge for the SiC MOSFET is lower than comparable silicon devices. The gate voltage must have a fast dV/dt to achieve fast switching times which indicates that a very low impedance driver is necessary. Lastly, the fidelity of the gate drive pulse must be carefully controlled. The nominal threshold voltage is 2.5V and the device is not fully on ($dV_{DS}/dt \approx 0$) until the V_{GS} is above 16V. This is a noticeably wider range than what is typically experienced with silicon MOSFETs and IGBTs. The net result of this is that the SiC MOSFET has a somewhat lower 'noise margin'. Any excessive ringing that is present on the gate drive signal could cause unintentional turn-on or partial turn-off of the device. The gate resistance should be carefully selected to ensure that the gate drive pulse is adequately dampened. To first order, the gate circuit can be approximated as a simple series RLC circuit driven by a voltage pulse as shown below.



$$\zeta = \frac{R_{LOOP}}{2}\sqrt{\frac{C_{GATE}}{L_{LOOP}}} \geq 1$$

$$\therefore\ R_{LOOP} \geq 2\sqrt{\frac{L_{LOOP}}{C_{GATE}}}$$

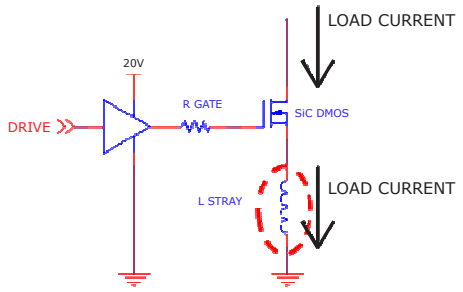
As shown, minimizing L_{LOOP} minimizes the value of R_{LOOP} needed for critical dampening. Minimizing L_{LOOP} also minimizes the rise/fall time. Therefore, it is strongly recommended that the gate drive be located as close to the SiC MOSFET as possible to minimize L_{LOOP}. The internal gate resistance of the SiC MOSFET is 5 Ω. An external resistance of 6.8 Ω was used to characterize this device.
Lower values of external gate resistance can be used so long as the gate fidelity is maintained. In the event that no external gate resistance is used, it is suggested that the gate current be checked to indirectly verify that there is no ringing present in the gate circuit. This can be accomplished with a very small current transformer. A recommended setup is a two-stage current transformer as shown below:



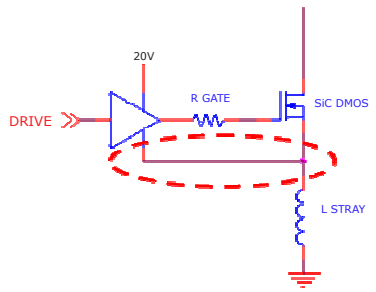
The two stage current transformer first stage consists of 10 turns of AWG 30 wire on a small high permeability core. A Ferroxcube 3E27 material is recommended. The second stage is a small wide bandwidth current transformer, such as the Tektronix CT-2. Lastly, a separate source return should be used for the gate drive as shown below:

Stray inductance on source lead causes load di/dt to be fed back into gate drive which causes the following:

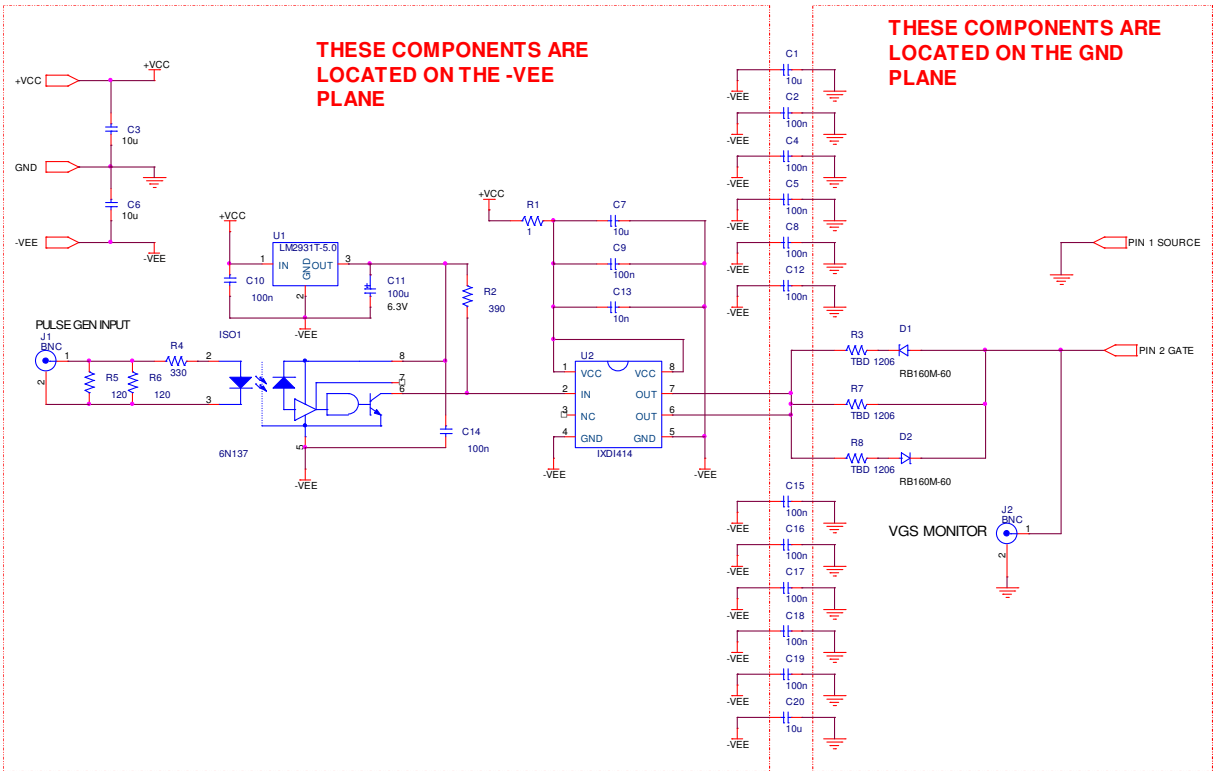
- *Switch di/dt is limited*
- *Could cause oscillation*



Kelvin gate connection with separate source return is highly recommended



A schematic of the gate driver circuit used for characterization of the SiC MOSFET is shown below:



The gate driver is an IXYS IXDI414. This device has a 35 V ouput swing, output resistance of 0.6 Ω typical, and a peak current capability of 14 A. The external gate resistance used for characterization of the SiC MOSFET was 6.8 Ω. Careful consideration needs to be given to the selection of the gate driver. The typical application error is selection of a gate driver that has adequate swing, but output

resistance and current drive capability are not carefully considered. It is critical that the gate driver possess high peak current capability and low output resistance along with adequate voltage swing.

A significant benefit of the SiC MOSFET is the elimination of the tail current observed in silicon IGBTs. However, it is very important to note that the current tail does provide a certain degree of parasitic dampening during turn-off. Additional ringing and overshoot is typically observed when silicon IGBTs are replaced with SiC MOSFETs. The additional voltage overshoot can be high enough to destroy the device. Therefore, it is critical to manage the output interconnection parasitics (and snubbers) to keep the ringing and overshoot from becoming problematic.

ESD RATINGS

ESD Test	Total Devices Sampled	Resulting Classification
ESD-HBM	All Devices Passed 1000V	2 (>2000V)
ESD-MM	All Devices Passed 400V	C (>400V)
ESD-CDM	All Devices Passed 1000V	IV (>1000V)

Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS} = 0V, I_D = 100μA	
$V_{GS(th)}$	Gate Threshold Voltage		2.5	4	V	V_{DS} = V_{GS}, I_D = 1mA, T_J = 25ºC	1
			1.8			V_{DS} = V_{GS}, I_D = 1mA, T_J = 125ºC	
I_{DSS}	Zero Gate Voltage Drain Current		1	100	μA	V_{DS} = 1200V, V_{GS} = 0V, T_J = 25ºC	
			10	250		V_{DS} = 1200V, V_{GS} = 0V, T_J = 125ºC	
I_{GSS}	Gate-Source Leakage Current			250	nA	V_{GS} = 20V, V_{DS} = 0V	
$R_{DS(on)}$	Drain-Source On-State Resistance		80	110	mΩ	V_{GS} = 20V, I_D = 20A, T_J = 25ºC	
			95	130		V_{GS} = 20V, I_D = 20A, T_J = 125ºC	
g_{fs}	Transconductance		7.3		S	V_{DS}= 20V, I_{DS}= 20A, T_J = 25ºC	fig. 3
			6.8			V_{DS}= 20V, I_{DS}= 20A, T_J = 125ºC	
C_{iss}	Input Capacitance		1915		pF	V_{GS} = 0V V_{DS} = 800V f = 1MHz V_{AC} = 25mV	fig. 5
C_{oss}	Output Capacitance		120				
C_{rss}	Reverse Transfer Capacitance		13				
$t_{d(on)i}$	Turn-On Delay Time		17.2		ns	V_{DD} = 800V V_{GS} = -2/20V I_D = 20A R_G = 6.8Ω L = 856μH Per JEDEC24 Page 27	fig. 12
t_r	Rise Time		13.6				
$t_{d(off)i}$	Turn-Off Delay Time		62				
t_{fi}	Fall Time		35.6				
E_{ON}	Turn-On Switching Loss (25ºC) (125ºC)		530 422		μJ		
E_{Off}	Turn-Off Switching Loss (25ºC) (125ºC)		320 329		μJ		
R_G	Internal Gate Resistance		5		Ω	V_{GS} = 0V, f = 1MHz, V_{AC} = 25mV	

NOTES: 1. The recommended on-state V_{GS} is +20V and the recommended off-state V_{GS} is between -2V and -5V

Reverse Diode Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{sd}	Diode Forward Voltage	3.5		V	V_{GS} = -5V, I_F=10A, T_J = 25ºC	
		3.1			V_{GS} = -2V, I_F=10A, T_J = 25ºC	
t_{rr}	Reverse Recovery Time	220		ns	V_{GS} = -5V, I_F=20A, T_J = 25ºC V_R = 800V, di_F/dt= 100A/μs	fig. 13,14
Q_{rr}	Reverse Recovery Charge	142		nC		
I_{rrm}	Peak Reverse Recovery Current	2.3		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.58	0.7	°C/W		fig. 6
$R_{\theta CS}$	Case to Sink, w/ Thermal Compound	0.25				
$R_{\theta JA}$	Thermal Resistance From Junction to Ambient		40			

Gate Charge Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
Q_{gs}	Gate to Source Charge	23.8		nC	V_{DD} = 800V I_D =20A V_{GS} = -2/20V Per JEDEC24-2	fig.9
Q_{gd}	Gate to Drain Charge	43.1				
Q_g	Gate Charge Total	90.8				

Typical Performance

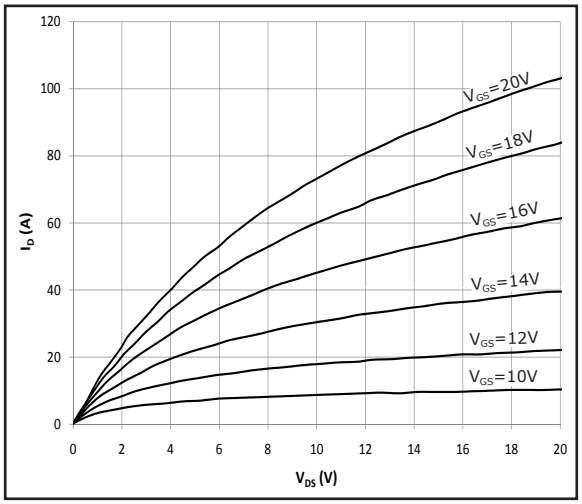


Fig 1. Typical Output Characteristics T_J = 25ºC

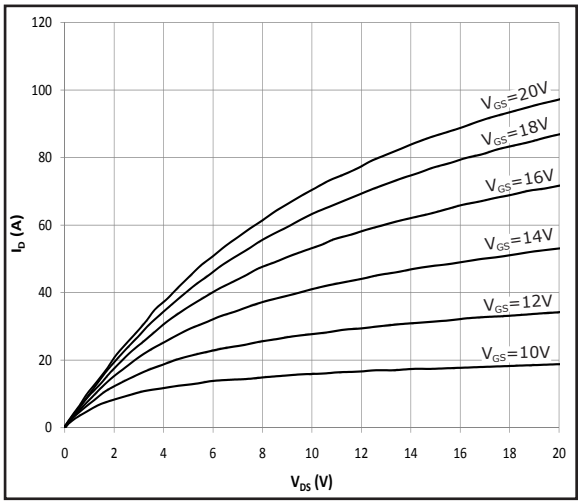


Fig 2. Typical Output Characteristics T_J = 125ºC

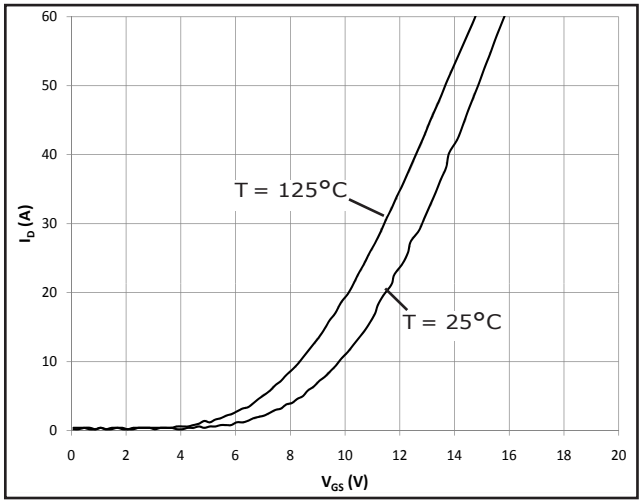


Figure 3. Typical Transfer Characteristics

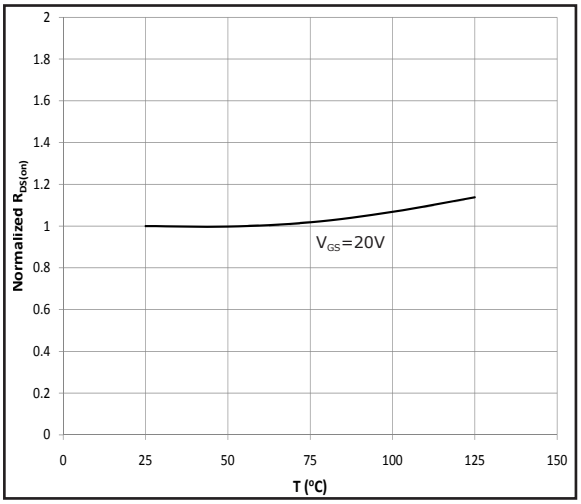
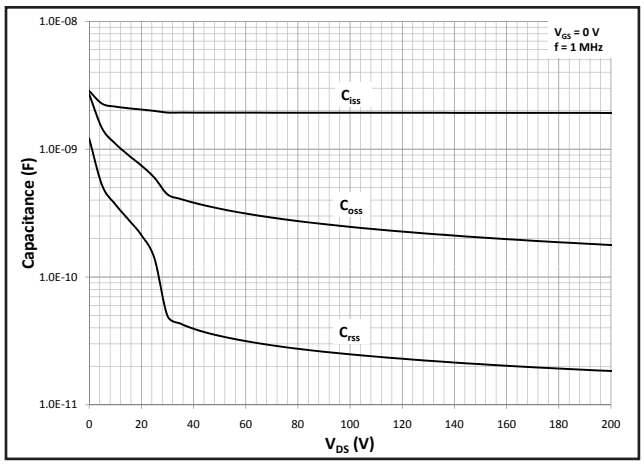


Fig 4. Normalized On-Resistance vs. Temperature



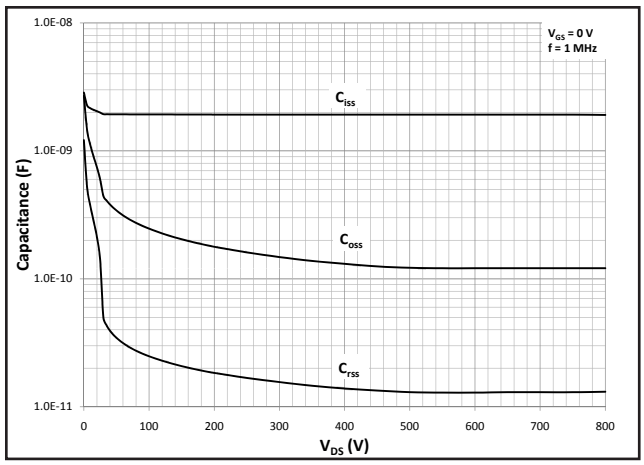


Fig 5A and 5B. Typical Capacitance vs. Drain – Source Voltage

Typical Performance

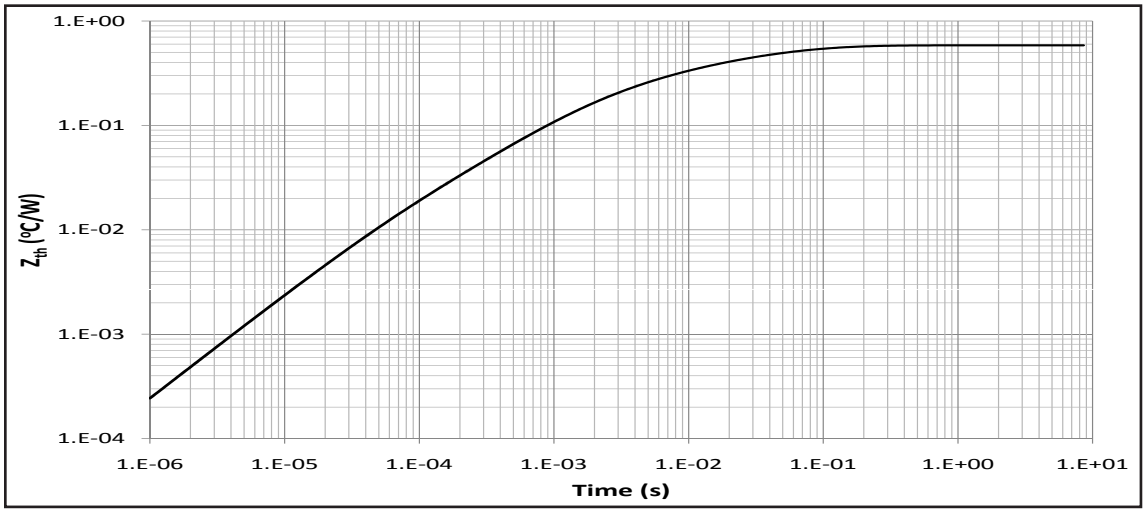


Fig 6. Transient Thermal Impedence, Junction - Case

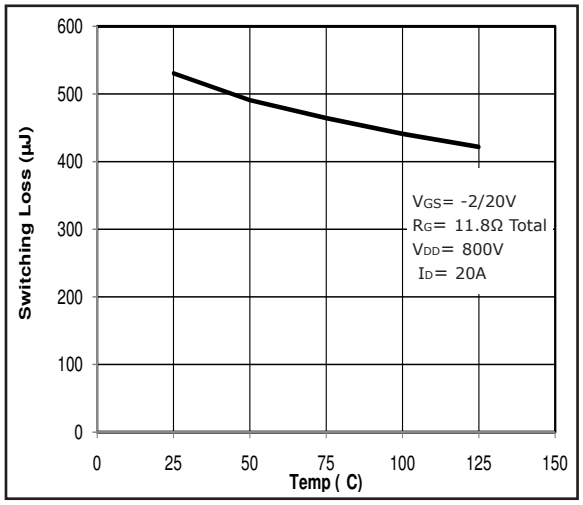


Fig 7. Inductive Switching Energy(Turn-on) vs. T

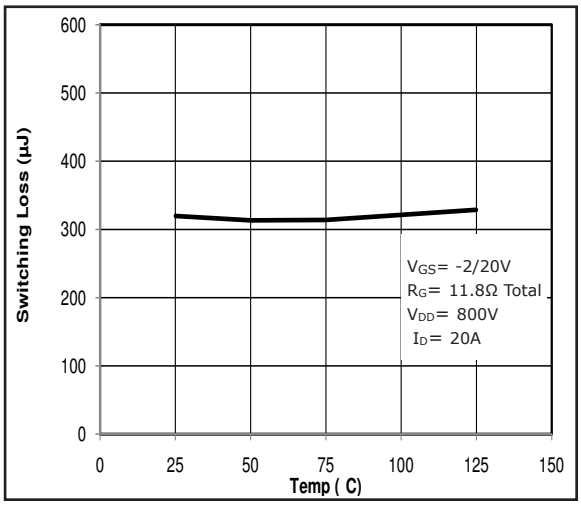


Fig 8. Inductive Switching Energy(Turn-off) vs. T

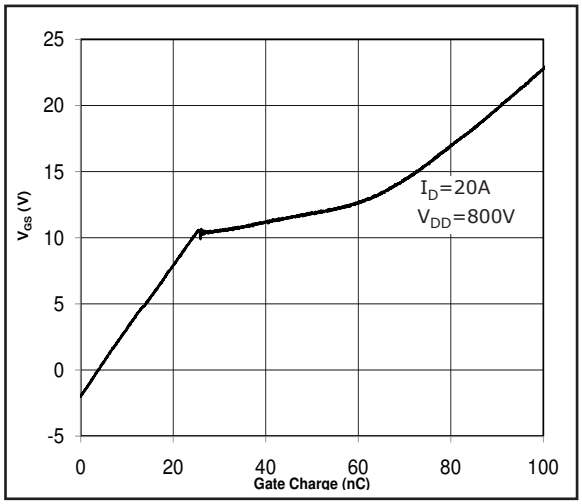


Fig 9. Typical Gate Charge Characteristics @ 25°C

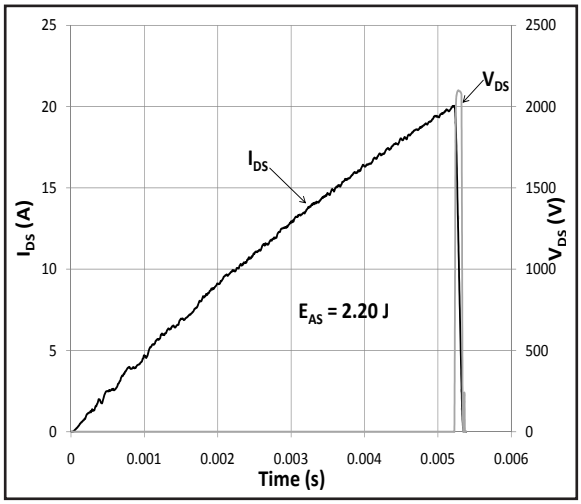


Fig 10. Typical Avalanche Waveform

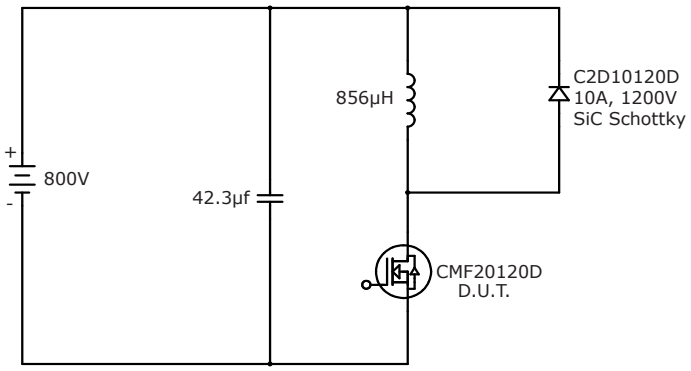


Fig 11. Switching Waveform Test Circuit

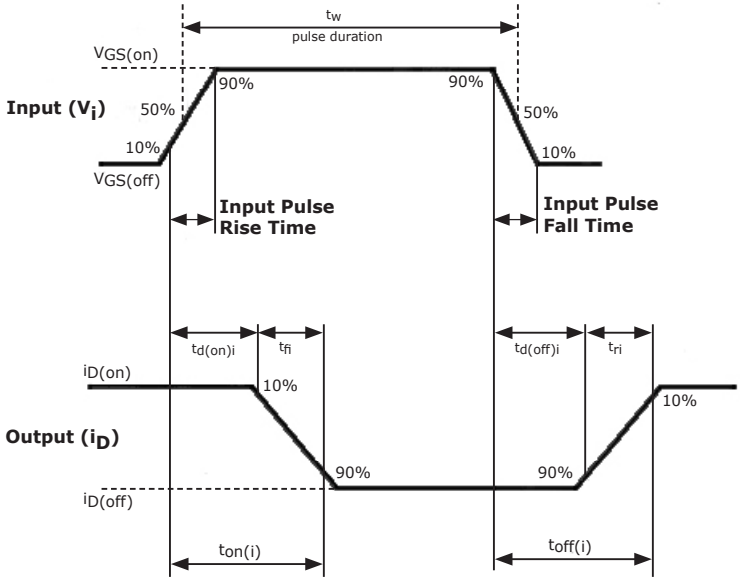


Fig 12. Switching Test Waveform Times

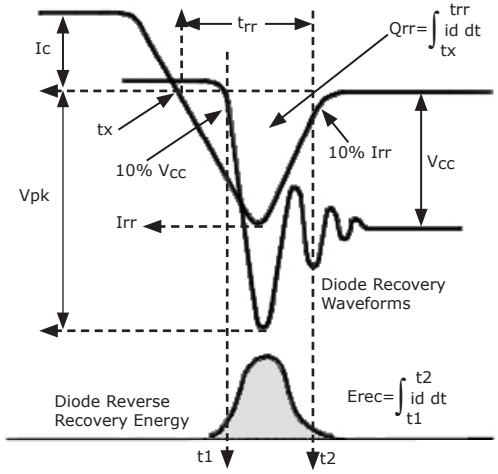


Fig 13. Body Diode Recovery Waveform

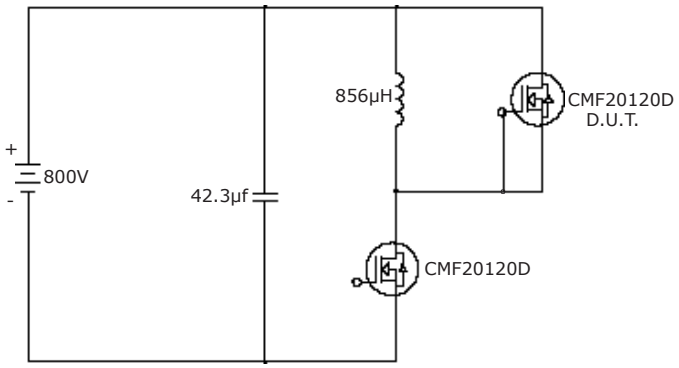


Fig 14. Body Diode Recovery Test

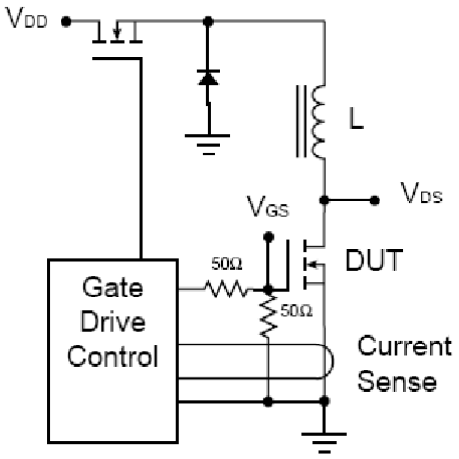
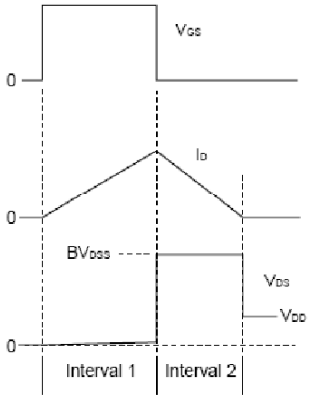


Fig 15. Avalanche Test Circuit

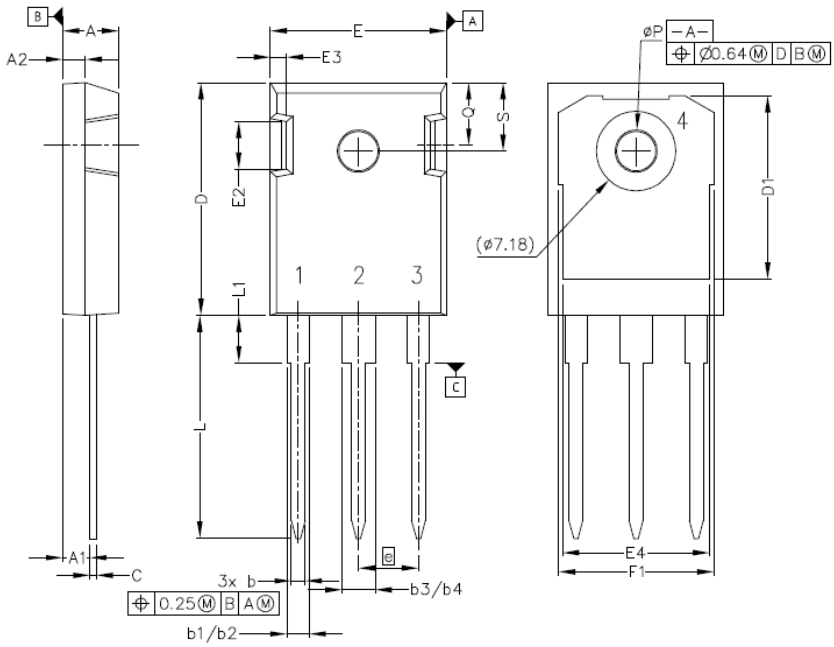


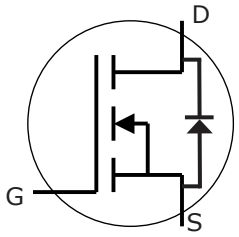
$$E_A = 1/2L \times I_D^2$$

Fig 16. Theoretical Avalanche Waveform

Package Dimensions

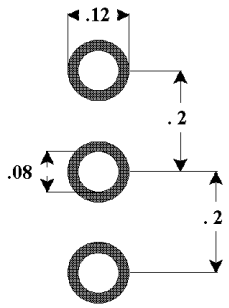
Package TO-247-3





POS	Inches		Millimeters	
	Min	Max	Min	Max
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.042	.052	1.07	1.33
b1	.075	.095	1.91	2.41
b2	.075	.085	1.91	2.16
b3	.113	.133	2.87	3.38
b4	.113	.123	2.87	3.13
c	.022	.027	0.55	0.68
D	.819	.831	20.80	21.10
D1	.640	.695	16.25	17.65
D2	.037	.049	0.95	1.25
E	.620	.635	15.75	16.13
E1	.516	.557	13.10	14.15
E2	.145	.201	3.68	5.10
E3	.039	.075	1.00	1.90
E4	.487	.529	12.38	13.43
e	.214 BSC		5.44 BSC	
N	3		3	
L	.780	.800	19.81	20.32
L1	.161	.173	4.10	4.40
ØP	.138	.144	3.51	3.65
Q	.216	.236	5.49	6.00
S	.238	.248	6.04	6.30

Recommended Solder Pad Layout



TO-247-3

Part Number	Package
CMF20120D	TO-247-3

"The levels of environmentally sensitive, persistent biologically toxic (PBT), persistent organic pollutants (POP), or otherwise restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS), as amended through April 21, 2006.

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