



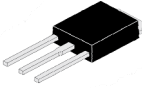
Continental Device India Pvt. Limited

An IATF 16949, ISO9001 and ISO 14001/ISO 45001 Certified Company



4A TRIAC

CST04H



TO-251 (I PAK)

**T0-251 (IPAK)
Plastic Package
RoHS compliant**

GENERAL DISCRIPTION:

With high ability to withstand the shock loading of large current, CST04H series triacs provide high dv/dt rate with strong resistance to electromagnetic interface. With high commutation performances, 3 quadrants products especially recommended for use on inductive load.

MAIN FEATURES

SYMBOL	VALUE	UNIT
$I_{T(RMS)}$	4	A
V_{DRM}/V_{RRM}	600/800	V

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C Unless otherwise specified)

PARAMETER	SYMBOL	VALUE	UNIT
Storage junction temperature range	T_{stg}	-40 to +150	°C
Operating junction temperature range	T_j	-40 to +125	°C
Repetitive peak off-state voltage ($T_j=25^{\circ}C$)	V_{DRM}	600/800	V
Repetitive peak reverse voltage ($T_j=25^{\circ}C$)	V_{RRM}	600/800	V
RMS on-state current	$I_{T(RMS)}$	4	A
Non repetitive surge peak on-state current (full cycle, F=50Hz)	I_{TSM}	40	A
I^2t value for fusing ($t_p=10ms$)	I^2t	8	A^2s
Critical rate of rise of on-state current ($I_G=2 \times I_{GT}$)	dI/dt	50	A/ μs
Peak gate current	I_{GM}	4	A
Average gate power dissipation	$P_{G(AV)}$	1	W
Peak gate power	P_{GM}	5	W

THERMAL RESISTANCES

junction to case(AC)	$R_{th(j-c)}$	2.8	°C/W
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CST04H

Rev0_02022023EBJ



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ELECTRICAL CHARACTERISTICS at (Ta = 25 °C Unless otherwise

3 Quadrants

Parameter	Quadrant	Symbol	Test Condition	Min/ Max	Value				Unit
					TW	SW	CW	BW	
Gate trigger current	I-II-III	I_{GT}	$V_D=12V R_L=33\Omega$	Max	5	10	35	50	mA
Gate trigger voltage	I-II-III	V_{GT}		Max	1.5				V
Non-triggering gate voltage	I-II-III	V_{GD}	$V_D=V_{DRM} T_j=125^\circ C$ $R_L=3.3K\Omega$	Min	0.2				V
Latching current	I-III	I_L	$I_G=1.2I_{GT}$	Max	10	20	50	70	mA
	II			Max	15	35	60	80	
Holding current		I_H	$I_T=100mA$	Max	10	15	35	60	mA
Critical rate of decrease of commutating on-state current		dV/dt	$V_D=2/3V_{DRM}$ Gate Open $T_j=125^\circ C$	Min	50	100	400	1000	V/ μs

STATIC CHARACTERISTICS

Parameter	Symbol	Test Condition	Value (Max)	Unit
Peak on-state voltage drop	$T_j=25^\circ C$ V_{TM}	$I_{TM}=5.5A t_p=380\mu s$	1.5	V
Maximum forward and reverse leakage	$T_j=25^\circ C$ I_{DRM}	$V_D=V_{DRM} V_R=V_{RRM}$	10	μA
Maximum leakage current for diodes	$T_j=125^\circ C$ I_{RRM}		0.75	mA

Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

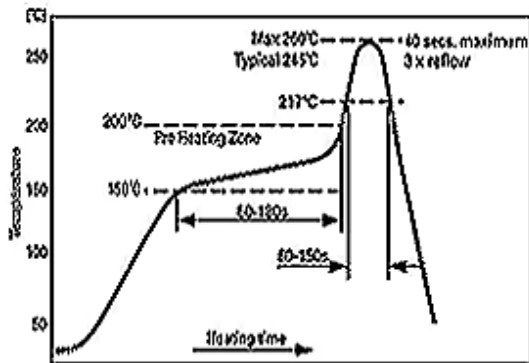
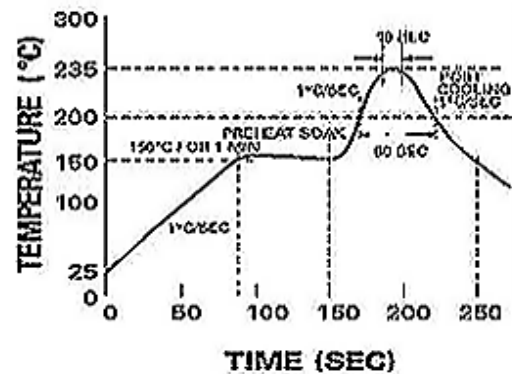


Figure 2



Reflow profiles in tabular form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat		
– Temperature Range	150-170°C	150-200°C
– Time	60-180 seconds	60-180 seconds
Time maintained above:		
– Temperature	200°C	217°C
– Time	30-50 seconds	60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.



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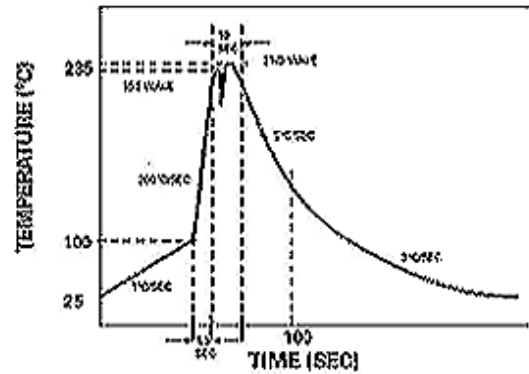
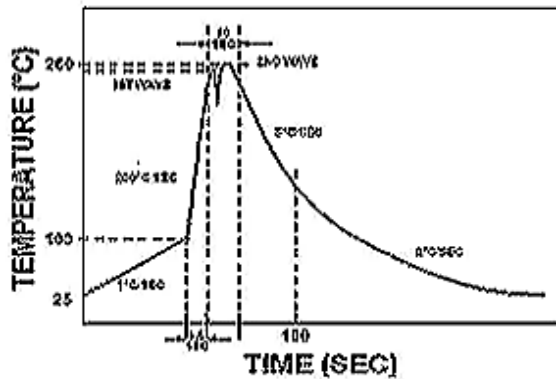
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Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used

The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder



Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max.

TYPICAL CHARACTERISTIC CURVES

Fig 1: Maximum power dissipation versus RMS on-state current

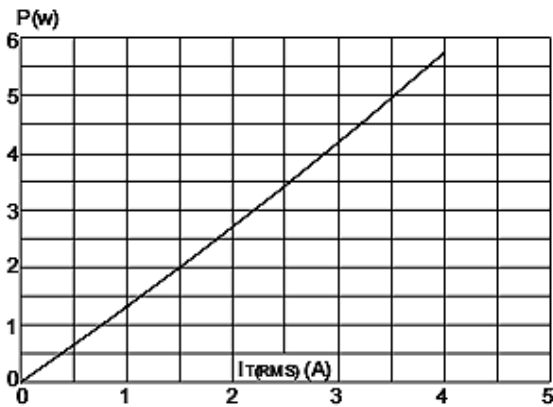


Fig 2: Surge peak on-state current versus number of cycles

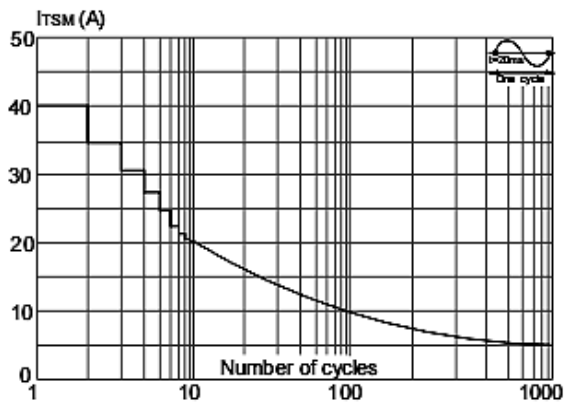


Fig 3: Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 20ms$ and corresponding value of I_t ($di/dt < 50A/\mu s$)

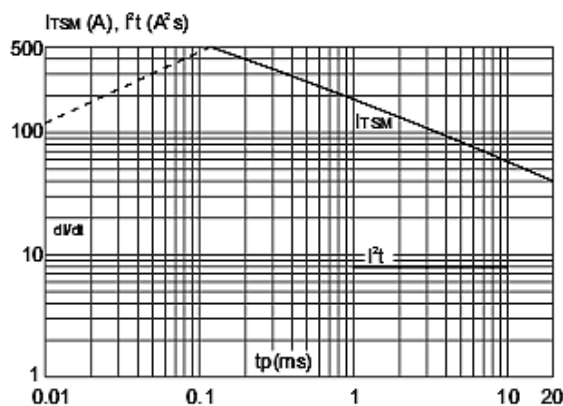


Fig 4: RMS on-state current versus case temperature

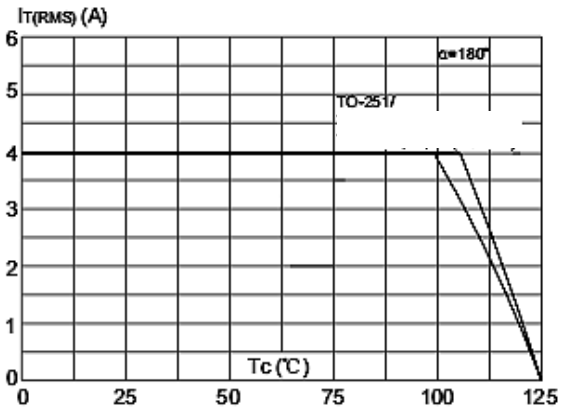


Fig 5: On-state characteristics (maximum values)

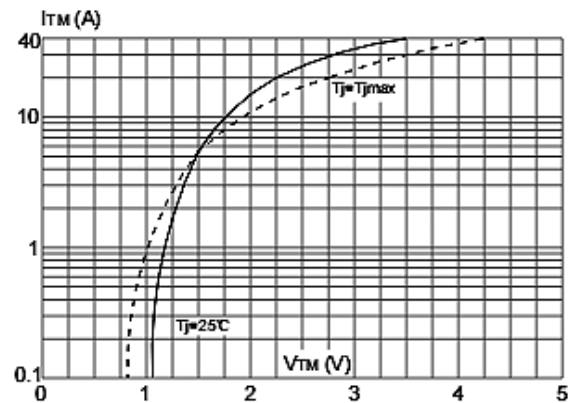
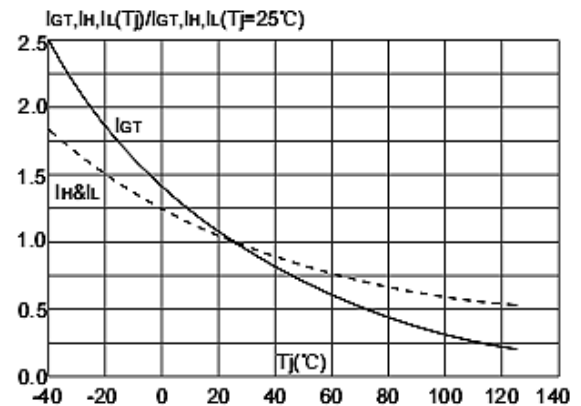
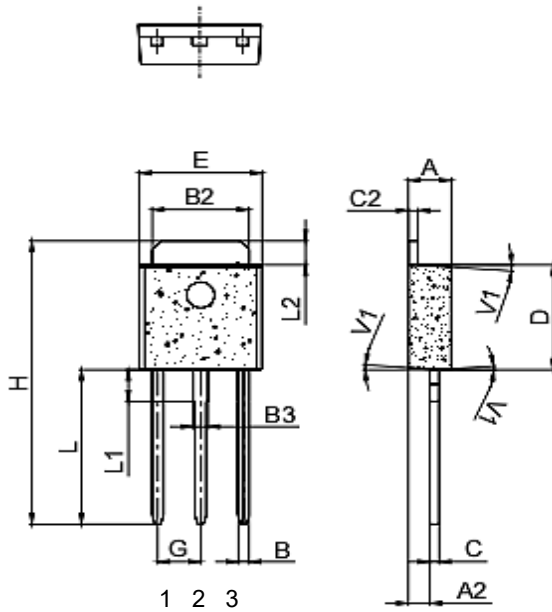


Fig 6: Relative variations of gate trigger current, holding current and latching current versus junction temperature



PACKAGE DETAILS

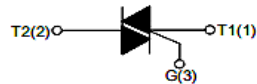
T0-251 (IPAK) Leaded Plastic Package



Ref.	Dimensions					
	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A	2.20		2.40	0.086		0.095
A2	0.90		1.20	0.04		0.047
B	0.55		0.65	0.02		0.026
B2	5.10		5.40	0.200		0.213
B3	0.76		0.85	0.030		0.033
C	0.45		0.62	0.02		0.024
C2	0.48		0.62	0.02		0.024
D	6		6.20	0.24		0.244
E	6.4		6.70	0.25		0.264
G		2.30			0.091	
H	16.0	3.75	17.0	0.630		0.669
L	8.90		9.40	0.350		0.370
L1	1.80		1.90	0.07		0.075
L2	1.37		1.50	0.05		0.059
V		4°			4°	

Pin Configuration

1. Terminal 1
2. Terminal 2
3. Gate





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Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.

If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.

The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.

For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	Time	Condition
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH



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Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

CDIL strives for continuous improvement and reserves the right to change the specifications of its products without prior notice.



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