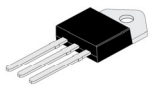
25A TRIACs

BTA26-600/800

TOP3 Insulated
Leaded Plastic
Package
RoHS compliant



TOP3 Insulated

MAIN FEATURES

SYMBOL	VALUE	UNIT
$I_{T(RMS)}$	25	A
V_{DRM} /V_{RRM}	600/800	V

GENERAL DISCRIPTION:

Suitable for Ac switching operations, the BTA26 can be set as an ON/OFF function in application such as static relays , heating regulation , induction motor, starting circuit for phase control in light dimmers motor speed controllers.
From all three terminals to external heatsink, BTA26 provide a rated insulation voltage of 2500 VRMS, complying with UL standards (File ref: E252906).

ABSOLUTE MAXIMUM RATINGS (Ta = 25 ℃ Unless otherwise specified)

PARAMETER		SYMBOL	VALUE	UNIT
Storage junction temperature range		Tstg	-40 -150	°C
Operating junction temperature range		T_j	-40 -125	°C
Repetitive peak off-state voltage Tj=25°C		V_{DRM}	600/800	V
Repetitive peak reverse voltage Tj=25°C		V_{RRM}	600/800	V
Non repetitive surge peak Off-state voltage		V_{DSM}	V_{DRM} +100	V
Non repetitive peak reverse voltage		V_{RSM}	V_{RRM} +100	V
RMS on-state current	T_C=100°C	$I_{T(RMS)}$	25	A
Non repetitive surge peak on-state current (full cycle, F=50Hz)		I_{TSM}	250	A
I^2t value for fusing (tp=10ms)		I^2t	340	A^2s
Critical rate of rise of on-state current (I_G =2×I_{GT})		dI/dt	50	A/µs
Peak gate current		I_{GM}	4	A
Average gate power dissipation		$P_{G(AV)}$	1	W
Peak gate power		P_{GM}	10	W

THERMAL RESISTANCES

Junction to case (AC)	TO-3P(Ins)	$R_{th\ (j-c)}$	1.0	°C/W

BTA26
Rev02 25072022E

ELECTRICAL CHARACTERISTICS at (Ta = 25 ℃ Unless otherwise specified)

3 Quadrants

PARAMETER	QUADRANT	SYMBOL	TEST CONDITION	VALUE			UNIT
					BW	CW	
Triggering gate current	I - II - III	I_{GT}	V_D=12V, R_L=33Ω	Max	50	35	mA
Triggering gate voltage	I - II - III	V_{GT}		Max	1.3		V
Non-triggering gate voltage	I - II - III	V_{GD}	V_D =V_{DRM} T_j =125°C R_L =3.3KΩ	Min	0.2		V
Latching current	I-III	I_L	I_G =1.2I_{GT}	Max	80	70	mA
	II				100	80	mA
Holding current		I_H	I_T =100mA	Max	75	50	mA
Critical rate of rise of off-state voltage		dV/dt	V_D=2/3V_{DRM} Gate Open Tj =125°C	Min	1000	500	V/μs

4 Quadrants

PARAMETER	QUADRANT	SYMBOL	TEST CONDITION	VALUE		UNIT
Triggering gate current	I - II - III	I_{GT}	V_D =12V R_L=33Ω	Max	50	mA
	IV				70	
Triggering gate voltage	ALL	V_{GT}		Max	1.3	V
Non-triggering gate voltage	ALL	V_{GD}	V_D =V_{DRM} T_j =125°C R_L =3.3KΩ	Min	0.2	V
Latching current	I-III	I_L	I_G =1.2I_{GT}	Max	90	mA
	II-IV				100	
Holding current		I_H	I_T =100mA	Max	80	mA
Critical rate of rise of off-state voltage		dV/dt	V_D=2/3V_{DRM} Gate Open Tj=125°C	Min	500	V/μs

STATIC CHARACTERISTICS

Peak on-state voltage drop	V_{TM}	I_{TM} =35A tp=380μs		1.5	V
Maximum forward leakage current	I_{DRM}	V_D =V_{DRM} V_R =V_{RRM}		5	μA
Maximum reverseleakage current	I_{RRM}			3	mA

Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

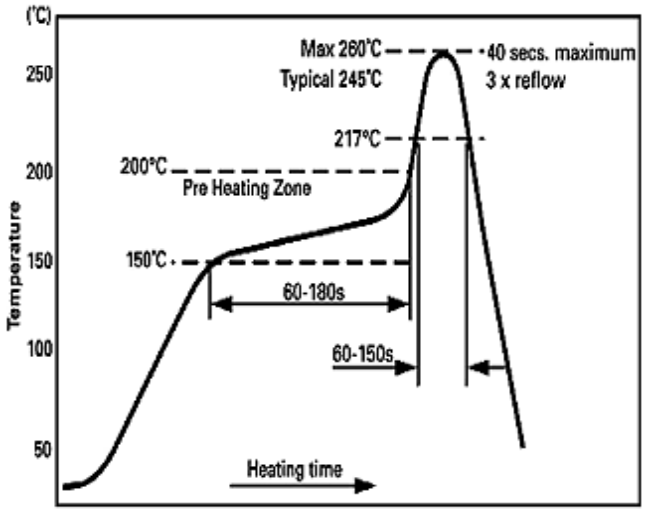
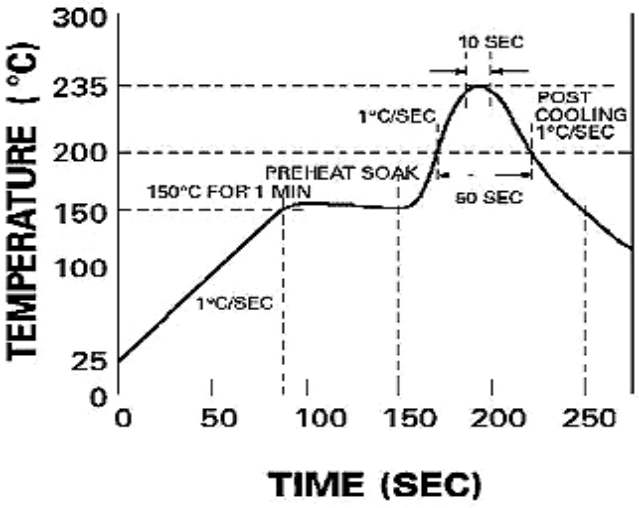


Figure 2

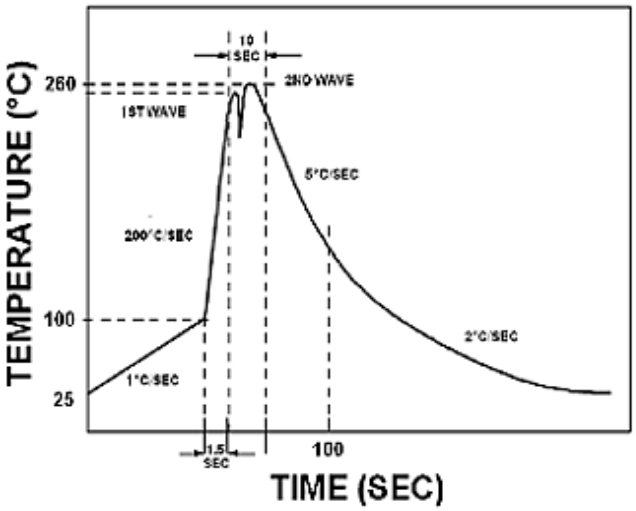


Reflow profiles in tabular form

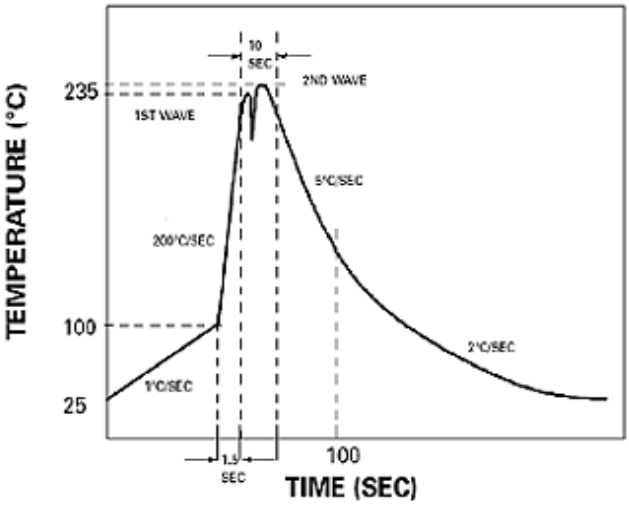
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat – Temperature Range – Time	 150-170°C 60-180 seconds	 150-200°C 60-180 seconds
Time maintained above: – Temperature – Time	 200°C 30-50 seconds	 217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder



Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max

TYPICAL CHARACTERISTIC CURVES

FIG.1: Maximum power dissipation versus RMS on-state current

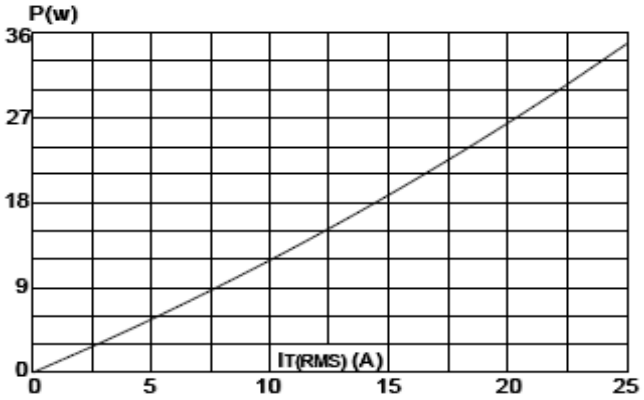


FIG.2: RMS on-state current versus case temperature

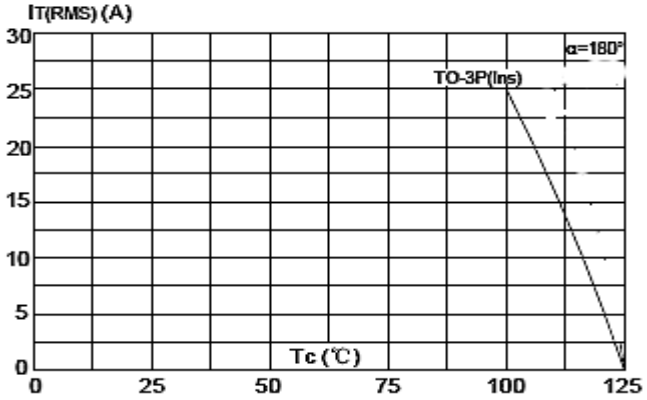


FIG.3: Surge peak on-state current versus number of cycles

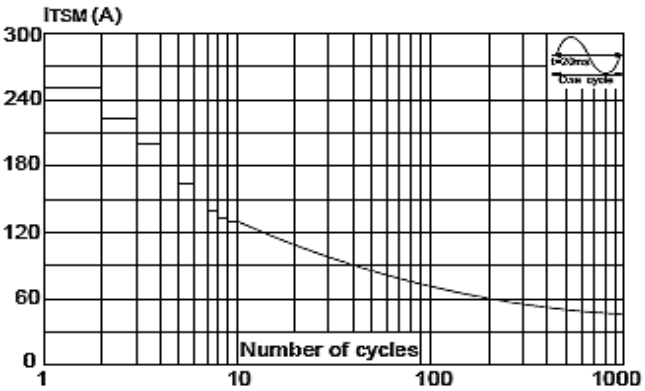


FIG.4: On-state characteristics (maximum values)

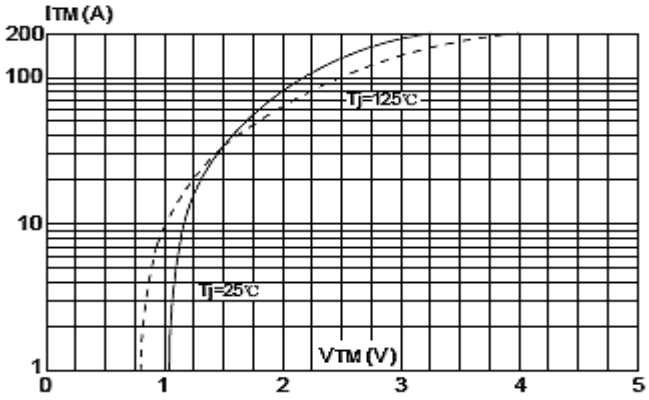


FIG.5: Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp<20ms, and corresponding value of I^2t (dI/dt < 50A/µs)

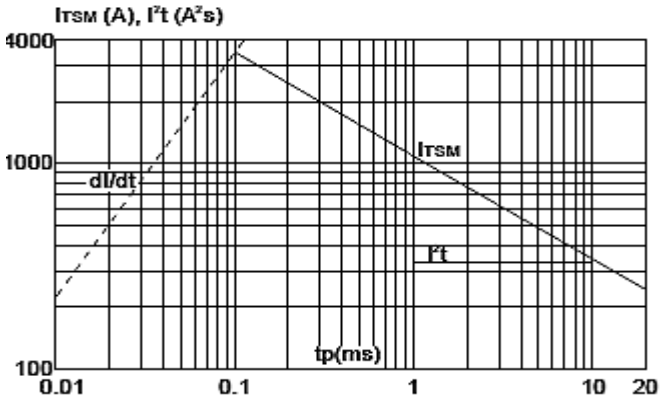
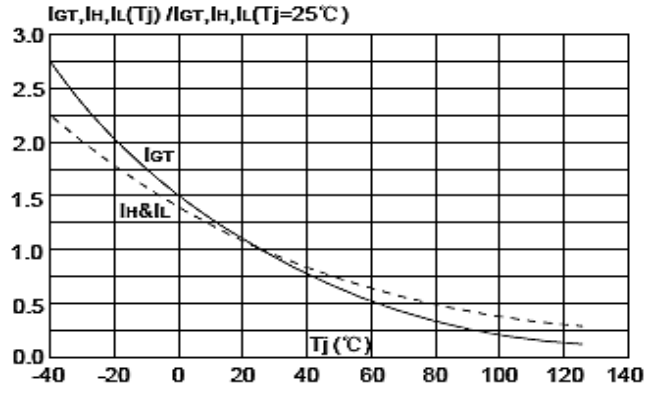
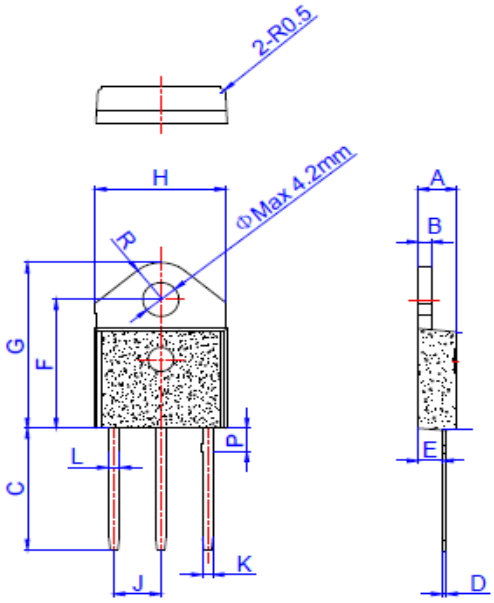


FIG.6: Relative variations of gate trigger current, holding current and latching current versus junction temperature



PACKAGE DETAIL

TOP3 Insulated Package

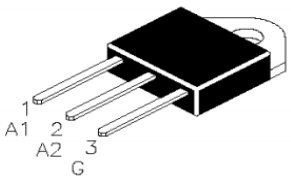


TO-3P Ins

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.173		0.181
B	1.45		1.55	0.057		0.061
C	14.35		15.60	0.565		0.614
D	0.50		0.70	0.020		0.028
E	2.70		2.90	0.106		0.114
F	15.80		16.50	0.622		0.650
G	20.40		21.10	0.803		0.831
H	15.10		15.50	0.594		0.610
J	5.40		5.65	0.213		0.222
K	1.10		1.40	0.043		0.055
L	1.35		1.50	0.053		0.059
P	2.80		3.00	0.110		0.118
R		4.35			0.171	

PIN CONFIGURATION

1. MAIN T1
2. MAIN T2
3. GATE



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Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).
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