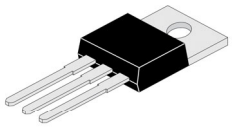
16A TRIACS

BTA16-600/800/1200 (Ins)
BTB16-600/800/1200 (Non-Ins)



TO-220

TO-220
Leaded Plastic Package
RoHS compliant

GENERAL DISCRIPTION :

BTA16 series triacs, with high ability to withstand the shock loading of large current, provide high dv/dt rate with strong resistance to electromagnetic interface. With high commutation performances, 3 quadrant products specially recommended for use on inductive load.

APPLICATIONS: High performance full-wave ac control applications

ABSOLUTE MAXIMUM RATINGS (Ta = 25 ℃ Unless otherwise specified)

PARAMETER		SYMBOL	VALUE	UNIT
Storage junction temperature range		T_{stg}	-40 to +150	°C
Operating junction temperature range		T_j	-40 to +125	°C
Repetitive peak off-state voltage (T_j=25°C)		V_{DRM}	600/800/1200	V
Repetitive peak reverse voltage (T_j=25°C)		V_{RRM}	600/800/1200	V
Non repetitive surge peak Off-state voltage		V_{DSM}	V_{DRM} +100	V
Non repetitive peak reverse voltage		V_{RSM}	V_{RRM} +100	V
RMS on-state current	TO-220 (Ins) (T_C=86°C)	$I_{T(RMS)}$	16	A
	TO-220 (Non-Ins) (T_C=107°C)			
Non repetitive surge peak on-state current (full cycle, F=50Hz)		I_{TSM}	160	A
I^2t value for fusing (t_p=10ms)		I^2t	128	A^2s
Critical rate of rise of on-state current (I_G =2×I_{GT})		dI/dt	50	A/µs
Peak gate current		I_{GM}	4	A
Average gate power dissipation		$P_{G(AV)}$	1	W
Peak gate power		P_{GM}	5	W

THERMAL RESISTANCES

PARAMETER		SYMBOL	VALUE (MAX)	UNIT
Maximum Thermal Resistance	TO-220 (Ins)	$R_{th(j-c)}$	2.1	°C/W
	TO-220 (Non-Ins)		1.2	

BTA16/BTB16_
Rev04 15092022EBJ

ELECTRICAL CHARACTERISTICS at (Ta = 25 ℃ Unless otherwise specified)

3 Quadrants (V_{DRM} /V_{RRM} : 600/800V)

PARAMETER	SYMBOL	QUADRANT	TEST CONDITION	VALUE				UNIT
				BW	CW	SW	TW	
Gate Trigger Current	I_{GT}	I - II - III	V_D =12V R_L =33Ω	<50	<35	<10	<5	mA
Gate Trigger Voltage	V_{GT}	I - II - III		<1.3				V
Off-State Gate Voltage	V_{GD}	I - II - III	V_D =V_{DRM} T_j =125°C R_L=3.3KΩ	>0.2				V
Latching Current	I_L	I - III	I_G =1.2I_{GT}	<70	<50	<30	<15	mA
		II		<80	<60	<40	<20	
Holding Current	I_H		I_T =100mA	<60	<40	<25	<15	mA
Critical Rate of Rise of Off-State Voltage	dV/dt		V_D=2/3V_{DRM} Gate Open T_j=125°C	>1000	>500	>200	>100	V/µs

4 Quadrant (V_{DRM}/V_{RRM}: 600/800V)

PARAMETER	SYMBOL	QUADRANT	TEST CONDITION	VALUE		UNIT
				B	C	
Gate Trigger Current	I_{GT}	I - II - III	V_D =12V R_L=33Ω	<50	<25	mA
		IV		<70	<50	
Gate Trigger Voltage	V_{GT}	ALL		<1.5		V
Off-State Gate Voltage	V_{GD}	ALL	V_D =V_{DRM} T_j =125°C R_L =3.3KΩ	>0.2		V
Latching Current	I_L	I - III - IV	I_G =1.2I_{GT}	<70	<50	mA
		II		<100	<80	
Holding Current	I_H		I_T =100mA	<60	<40	mA
Critical Rate of Rise of Off-State Voltage	dV/dt		V_D=2/3V_{DRM} Gate Open T_j=125°C	>500	>200	V/µs

3 Quadrants (V_{DRM}/V_{RRM}: 1200V)

PARAMETER	SYMBOL	QUADRANT	TEST CONDITION	VALUE	UNIT
Gate Trigger Current	I_{GT}	I - II - III	V_D =12V R_L =33Ω	<50	mA
Gate Trigger Voltage	V_{GT}	I - II - III		<1.5	V
Off-State Gate Voltage	V_{GD}	I - II - III	V_D =V_{DRM} T_j =125°C R_L=3.3KΩ	>0.2	V
Latching Current	I_L	I - III	I_G =1.2I_{GT}	<70	mA
		II		<90	
Holding Current	I_H		I_T =100mA	<60	mA
Critical Rate of Rise of Off-State Voltage	dV/dt		V_D=2/3V_{DRM} Gate Open T_j=125°C	>1500	V/µs

ELECTRICAL CHARACTERISTICS at (Ta = 25 ℃ Unless otherwise specified)

STATIC CHARACTERISTICS

PARAMETER		SYMBOL	TEST CONDITION	VALUE			UNIT
				600V	800V	1200V	
On-State Voltage	T_j=25°C	V_{TM}	I_{TM} =22.5A t_p=380μs		1.5		V
Off-State Leakage Current	T_j=25°C	I_{DRM}	V_D =V_{DRM} , V_R =V_{RRM}	5	5	10	μA
	T_j=125°C	I_{RRM}		2	2	1	mA

ORDERING INFORMATION

BTA12-XY
BTB12-XY

Where

X = 600: VDRM/VRRM ≥ 600
= 800: VDRM/VRRM ≥ 800
= 1200: VDRM/VRRM ≥ 1200

Y = BW: IGT1-3 ≤ 50mA
= CW: IGT1-3 ≤ 35mA
= SW: IGT1-3 ≤ 10mA
= TW: IGT1-3 ≤ 5mA
= B: IGT1-3≤50mA IGT4≤70mA
= C: IGT1-3≤25mA IGT4≤50mA

Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

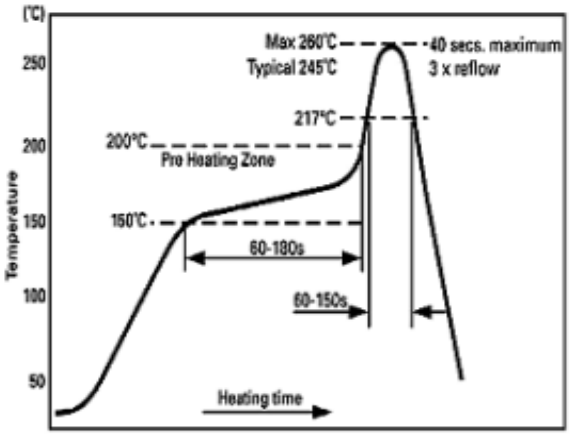
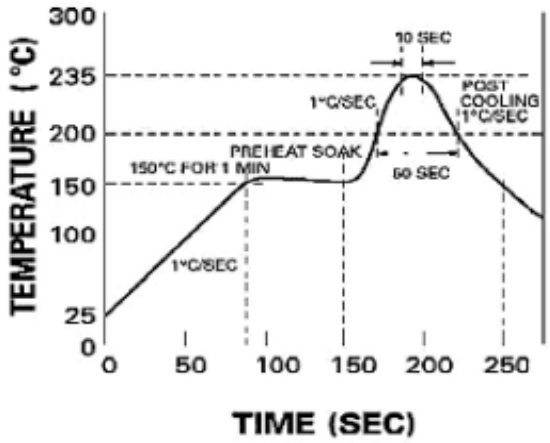


Figure 2

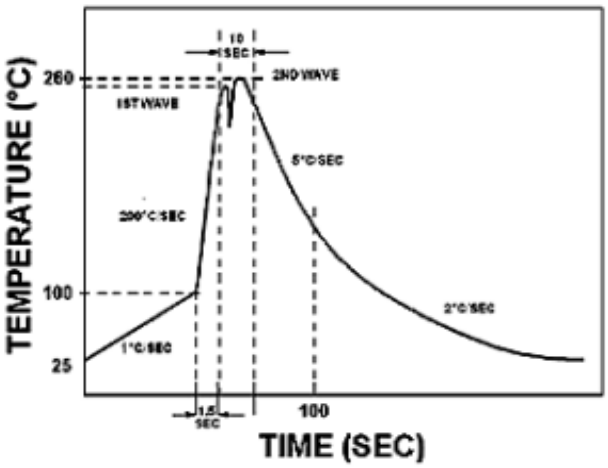


Reflow profiles in tabular form

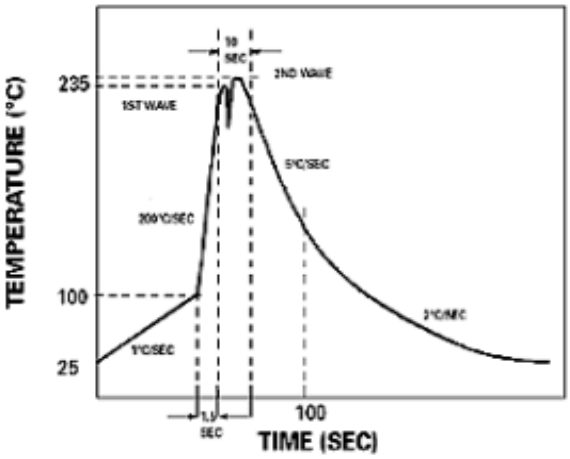
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat – Temperature Range – Time	 150-170°C 60-180 seconds	 150-200°C 60-180 seconds
Time maintained above: – Temperature – Time	 200°C 30-50 seconds	 217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder

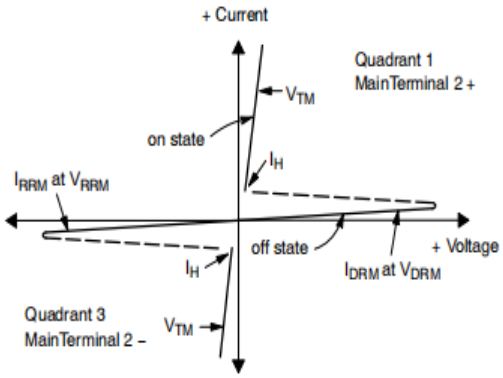


Wave Profiles in Tabular Form

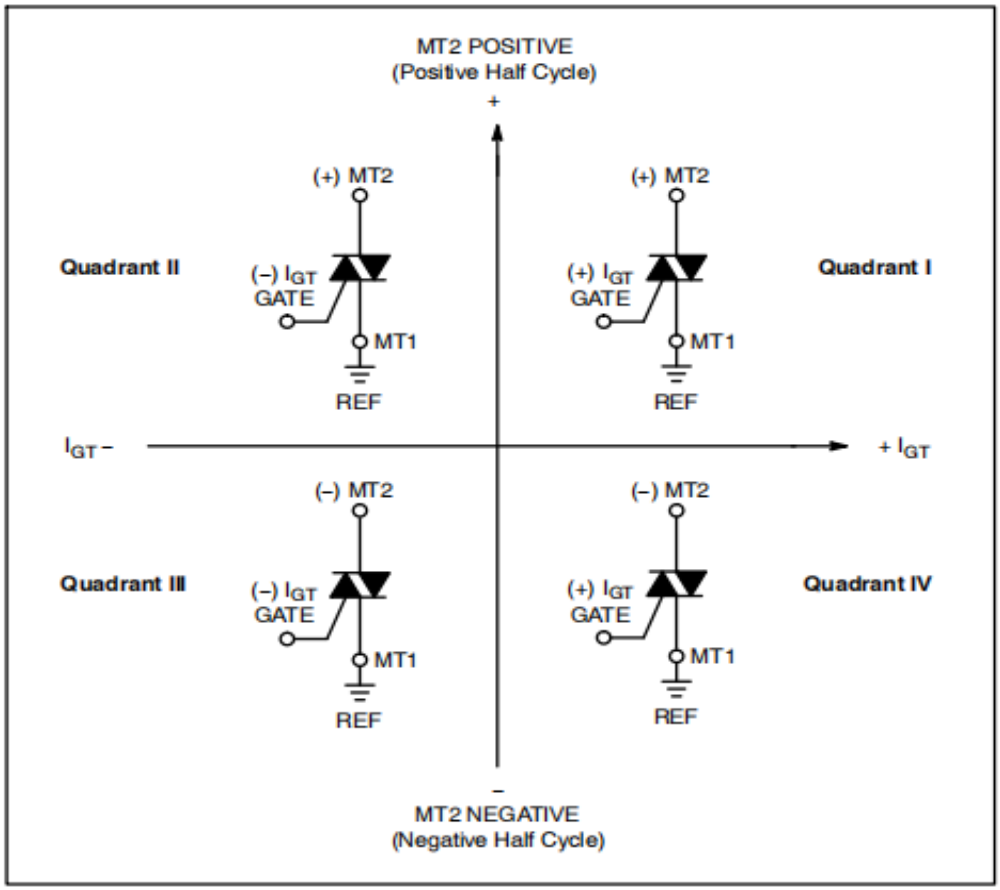
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max

Voltage Current Characteristic of Triacs
(Bidirectional Device)

SYMBOL	PARAMETER
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current



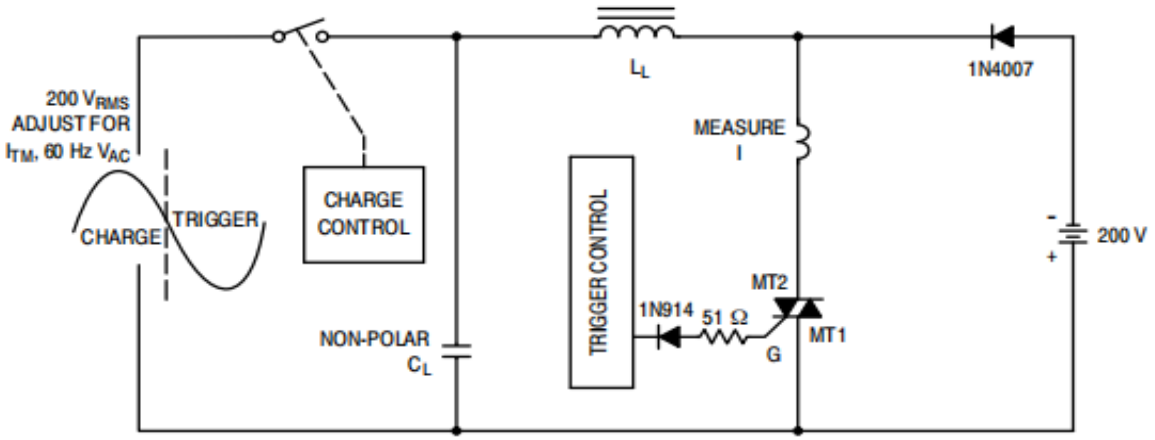
Quadrant Definitions for a Triac



All polarities are referenced to MT1.
With in−phase signals (using standard AC lines) quadrants I and III are used.

TEST CIRCUIT AND DIAGRAMS

Simplified Test Circuit to Measure the Critical Rate of Rise of Commutating Current (di/dt)c



Note: Component values are for verification of rated $(di/dt)_c$. See AN1048 for additional information.

TYPICAL CHARACTERISTICS CURVES

Fig 1: Typical RMS Current Derating

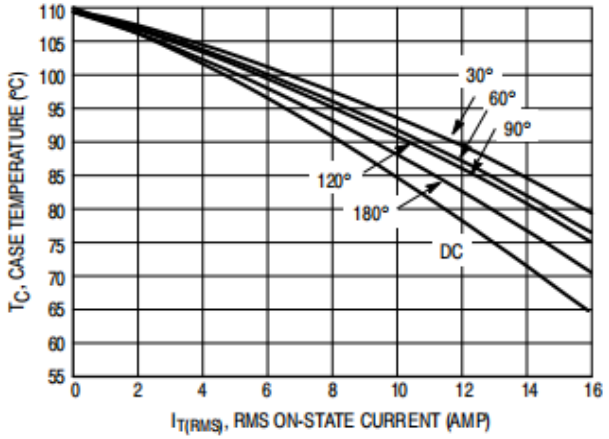


Fig 2: On-State Characteristics

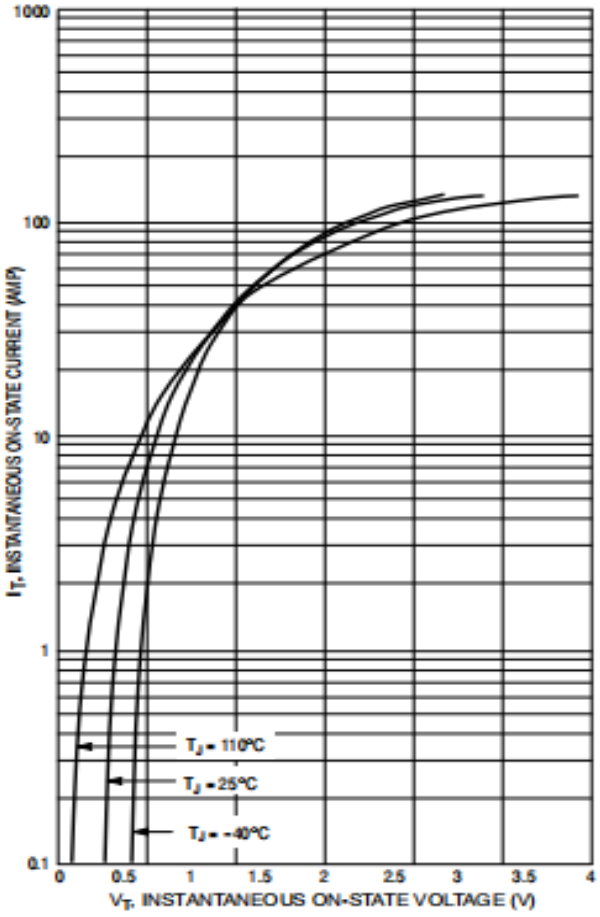


Fig 3: On-State Power Dissipation

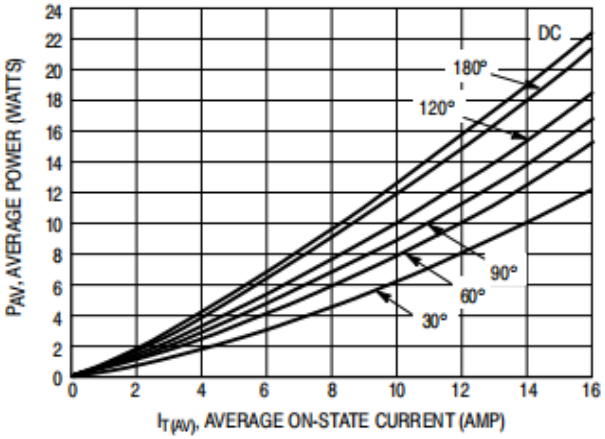


Fig 4: Thermal Response

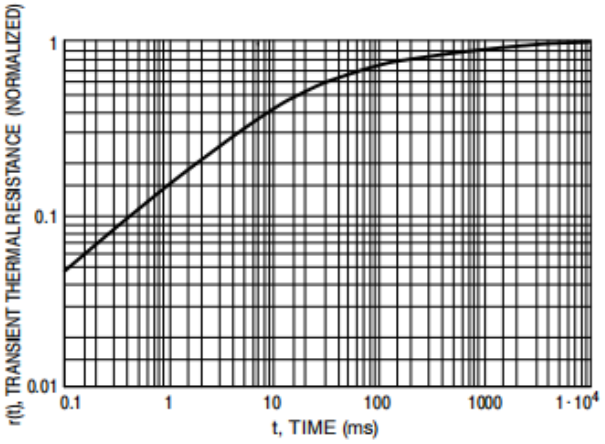
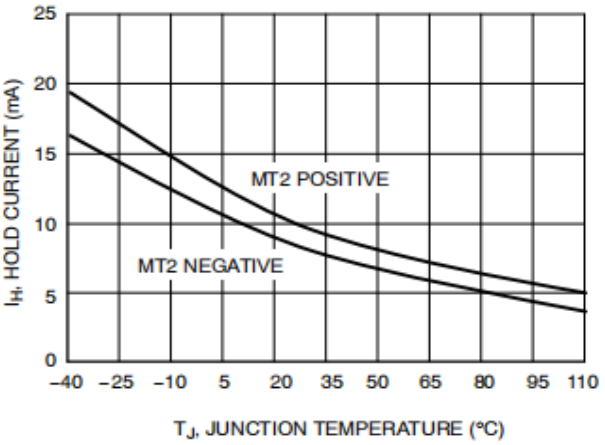


Fig 5: Typical Hold Current Variation



TYPICAL CHARACTERISTICS CURVES

Fig 6: Typical Gate Trigger Current Variation

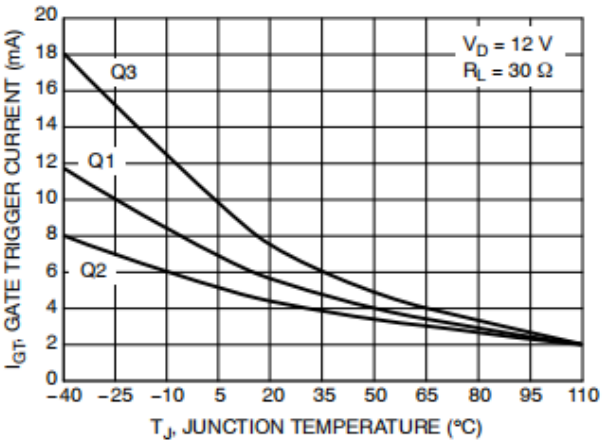


Fig 7: Typical Gate Trigger Voltage Variation

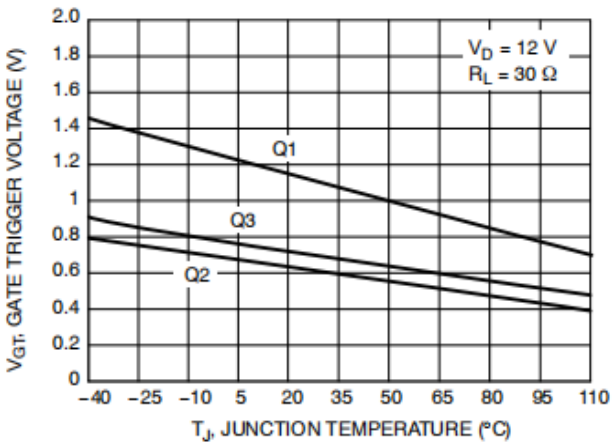
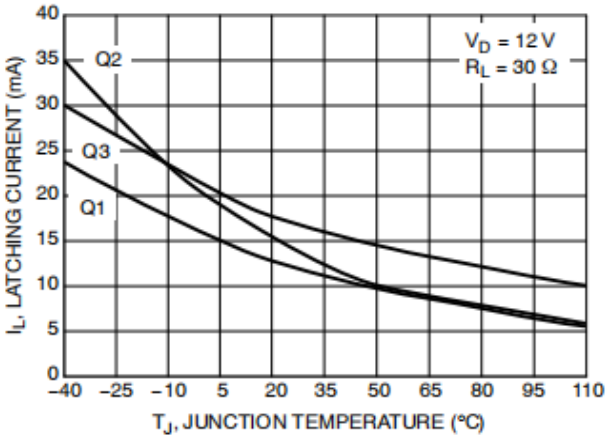
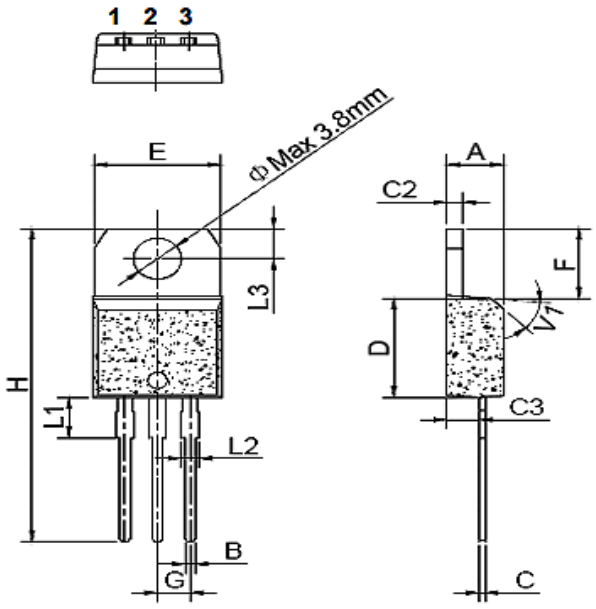


Fig 8: Typical Latching Current Variation



PACKAGE DETAILS

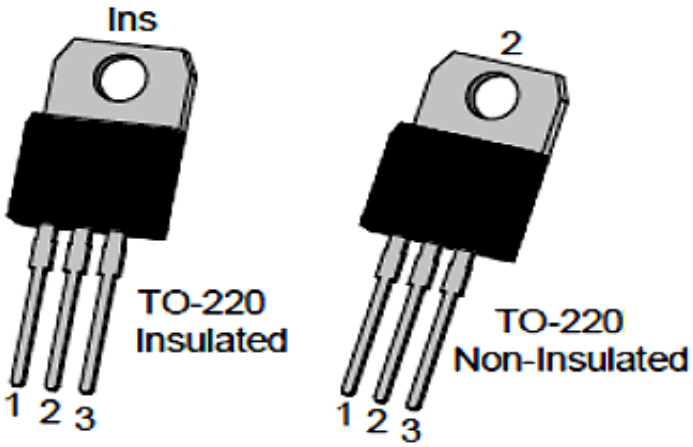
TO-220 Insulated/ Non-insulated Leaded Plastic Package



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.173		0.181
B	0.61		0.88	0.024		0.035
C	0.46		0.70	0.018		0.028
C2	1.21		1.32	0.048		0.052
C3	2.40		2.72	0.094		0.107
D	8.60		9.70	0.339		0.382
E	9.80		10.4	0.386		0.409
F	6.55		6.95	0.258		0.274
G		2.54			0.1	
H	28.0		29.8	1.102		1.173
L1		3.75			0.15	
L2	1.14		1.70	0.045		0.067
L3	2.65		2.95	0.104		0.116
V1		45°			45°	

Pin Configuration

1. T1
2. T2
3. GATE



Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).
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Continental Device India Pvt. Limited
C-120 Naraina Industrial Area, New Delhi 110 028, India.
Telephone +91-11-2579 6150, 4141 1112 Fax +91-11-2579 5290, 4141 1119
email@cdil.com www.cdil.com
CIN No. U32109DL1964PTC004291