

# Am49PDLI27BH/ Am49PDLI29BH

Data Sheet



July 2003

The following document specifies Spanion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

## **Continuity of Specifications**

There is no change to this datasheet as a result of offering the device as a Spanion product. Any changes that have been made are the result of normal datasheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

## **Continuity of Ordering Part Numbers**

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

## **For More Information**

Please contact your local AMD or Fujitsu sales office for additional information about Spanion memory solutions.

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# Am49PDL127BH/Am49PDL129BH

## Stacked Multi-Chip Package (MCP) Flash Memory and pSRAM

128 Megabit (8 M x 16-Bit) CMOS 3.0 Volt-only, Simultaneous Operation Flash Memory and 32 Mbit (2 M x 16-Bit) CMOS Pseudo Static RAM with Page Mode

### DISTINCTIVE CHARACTERISTICS

#### MCP Features

- **Power supply voltage of 2.7 to 3.3 volt**
- **High performance**
  - Access time as fast as 65 ns initial / 25 ns page
- **Package**
  - 73-Ball FBGA
- **Operating Temperature**
  - -40°C to +85°C

#### Flash Memory Features

#### ARCHITECTURAL ADVANTAGES

- **128 Mbit Page Mode device**
  - Page size of 8 words: Fast page read access from random locations within the page
- **Dual Chip Enable inputs (PDL129 only)**
  - Two CE# inputs control selection of each half of the memory space
- **Single power supply operation**
  - Full Voltage range: 2.7 to 3.3 volt read, erase, and program operations for battery-powered applications
- **Simultaneous Read/Write Operation**
  - Data can be continuously read from one bank while executing erase/program functions in another bank
  - Zero latency switching from write to read operations
- **FlexBank Architecture**
  - 4 separate banks, with up to two simultaneous operations per device
  - Bank A: 16 Mbit (4 Kw x 8 and 32 Kw x 31)
  - Bank B: 48 Mbit (32 Kw x 96)
  - Bank C: 48 Mbit (32 Kw x 96)
  - Bank D: 16 Mbit (4 Kw x 8 and 32 Kw x 31)
- **SecSi™ (Secured Silicon) Sector region**
  - Up to 128 words accessible through a command sequence
  - Up to 64 factory-locked words
  - Up to 64 customer-lockable words

- **Both top and bottom boot blocks in one device**
- **Manufactured on 0.13  $\mu$ m process technology**
- **20-year data retention at 125°C**
- **Minimum 1 million erase cycle guarantee per sector**

#### PERFORMANCE CHARACTERISTICS

- **High Performance**
  - Page access times as fast as 25 ns
  - Random access times as fast as 65 ns
- **Power consumption (typical values at 10 MHz)**
  - 45 mA active read current
  - 25 mA program/erase current
  - 1  $\mu$ A typical standby mode current

#### SOFTWARE FEATURES

- **Software command-set compatible with JEDEC 42.4 standard**
  - Backward compatible with Am29F and Am29LV families
- **CFI (Common Flash Interface) complaint**
  - Provides device-specific information to the system, allowing host software to easily reconfigure for different Flash devices
- **Erase Suspend / Erase Resume**
  - Suspends an erase operation to allow read or program operations in other sectors of same bank
- **Unlock Bypass Program command**
  - Reduces overall programming time when issuing multiple program command sequences

**HARDWARE FEATURES**

- **Ready/Busy# pin (RY/BY#)**
  - Provides a hardware method of detecting program or erase cycle completion
- **Hardware reset pin (RESET#)**
  - Hardware method to reset the device to reading array data
- **WP#/ACC (Write Protect/Acceleration) input**
  - At  $V_{IL}$ , hardware level protection for the first and last two 4K word sectors.
  - At  $V_{IH}$ , allows removal of sector protection
  - At  $V_{HH}$ , provides accelerated programming in a factory setting
- **Persistent Sector Protection**
  - A command sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector
  - Sectors can be locked and unlocked in-system at  $V_{CC}$  level
- **Password Sector Protection**
  - A sophisticated sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector using a user-defined 64-bit password

**pSRAM FEATURES**

- **Power dissipation**
  - Operating: 40 mA maximum
  - Standby: 70  $\mu$ A maximum
  - Deep power-down standby: 5  $\mu$ A
- **CE1s# and CE2ps Chip Select**
- **Power down features using CE1s# and CE2ps**
- **Data retention supply voltage: 2.7 to 3.3 volt**
- **Byte data control: LB#s (DQ7–DQ0), UB#s (DQ15–DQ8)**
- **8-word page mode access**

## GENERAL DESCRIPTION

The Am29PDL127H/Am29PDL129H are 128 Mbit, 3.0 volt-only Page Mode and Simultaneous Read/Write Flash memory devices organized as 8 Mwords. The word-wide data (x16) appears on DQ15-DQ0. The devices can be programmed in-system or in standard EPROM programmers. A 12.0 V  $V_{PP}$  is not required for write or erase operations.

The devices offer fast page access time of 25 and 30 ns, with corresponding random access times of 65 and 85 ns, respectively, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the devices have separate chip enable (CE#f1, CE#f2), write enable (WE#) and output enable (OE#) controls. Dual Chip Enables allow access to two 64 Mbit partitions of the 128 Mbit memory space.

### Simultaneous Read/Write Operation with Zero Latency

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into 4 banks, which can be considered to be four separate memory arrays as far as certain operations are concerned. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from another bank with zero latency (with two simultaneous operations operating at any one time). This releases the system from waiting for the completion of a program or erase operation, greatly improving system performance.

The device can be organized in both top and bottom sector configurations. The banks are organized as follows:

#### PDL127 Configuration

| Chip Enable Control | Bank | Sectors                           |
|---------------------|------|-----------------------------------|
| CE#f1               | A    | 16 Mbit (4 Kw x 8 and 32 Kw x 31) |
|                     | B    | 48 Mbit (32 Kw x 96)              |
|                     | C    | 48 Mbit (32 Kw x 96)              |
|                     | D    | 16 Mbit (4 Kw x 8 and 32 Kw x 31) |

#### PDL129H Configuration

| Chip Enable Control | Bank | Sectors                           |
|---------------------|------|-----------------------------------|
| CE#f1               | A    | 16 Mbit (4 Kw x 8 and 32 Kw x 31) |
|                     | B    | 48 Mbit (32 Kw x 96)              |
| CE#f2               | C    | 48 Mbit (32 Kw x 96)              |
|                     | D    | 16 Mbit (4 Kw x 8 and 32 Kw x 31) |

### Page Mode Features

The page size is 8 words. After initial page access is accomplished, the page mode operation provides fast read access speed of random locations within that page.

### Standard Flash Memory Features

The device requires a **single 3.0 volt power supply** (2.7 V to 3.3 V) for both read and write functions. Internally gener-

ated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC 42.4 single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timing. Register contents serve as inputs to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. The Unlock Bypass mode facilitates faster programming times by requiring only two write cycles to program data instead of four. Device erasure occurs by executing the erase command sequence.

The host system can detect whether a program or erase operation is complete by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The sector erase architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

**Hardware data protection** measures include a low  $V_{CC}$  detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

**The Erase Suspend/Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved. If a read is needed from the SecSi Sector area (One Time Program area) after an erase suspend, then the user must use the proper command sequence to enter and exit this region.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the standby mode. Power consumption is greatly reduced in both these modes.

AMD's Flash technology combined years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

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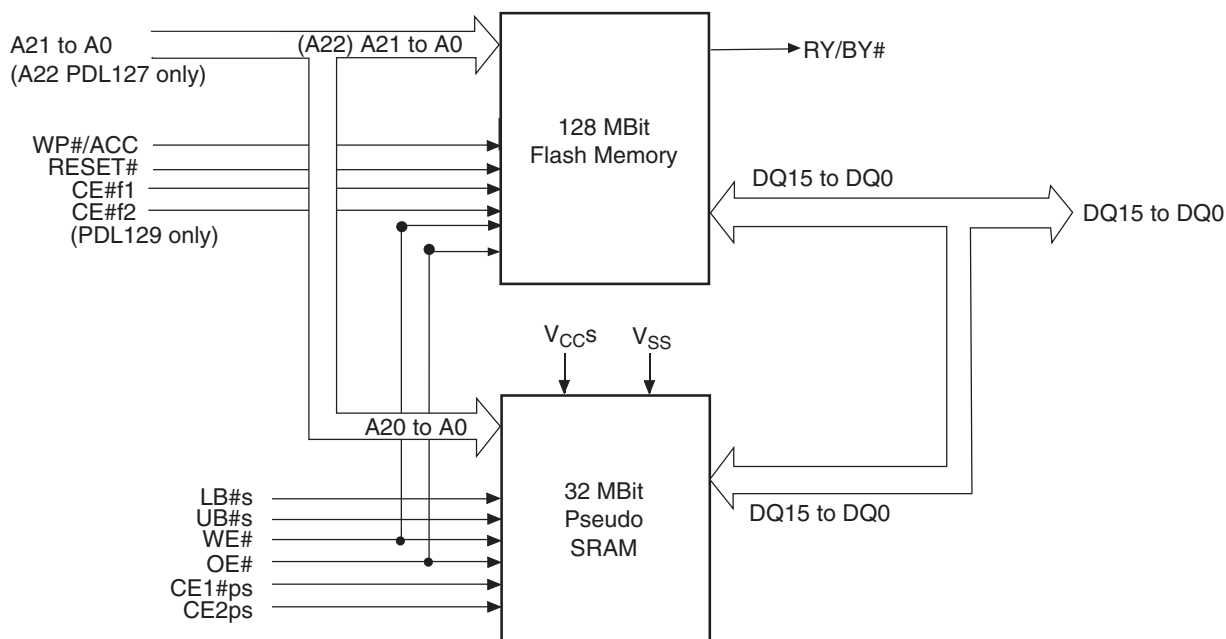
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## PRODUCT SELECTOR GUIDE

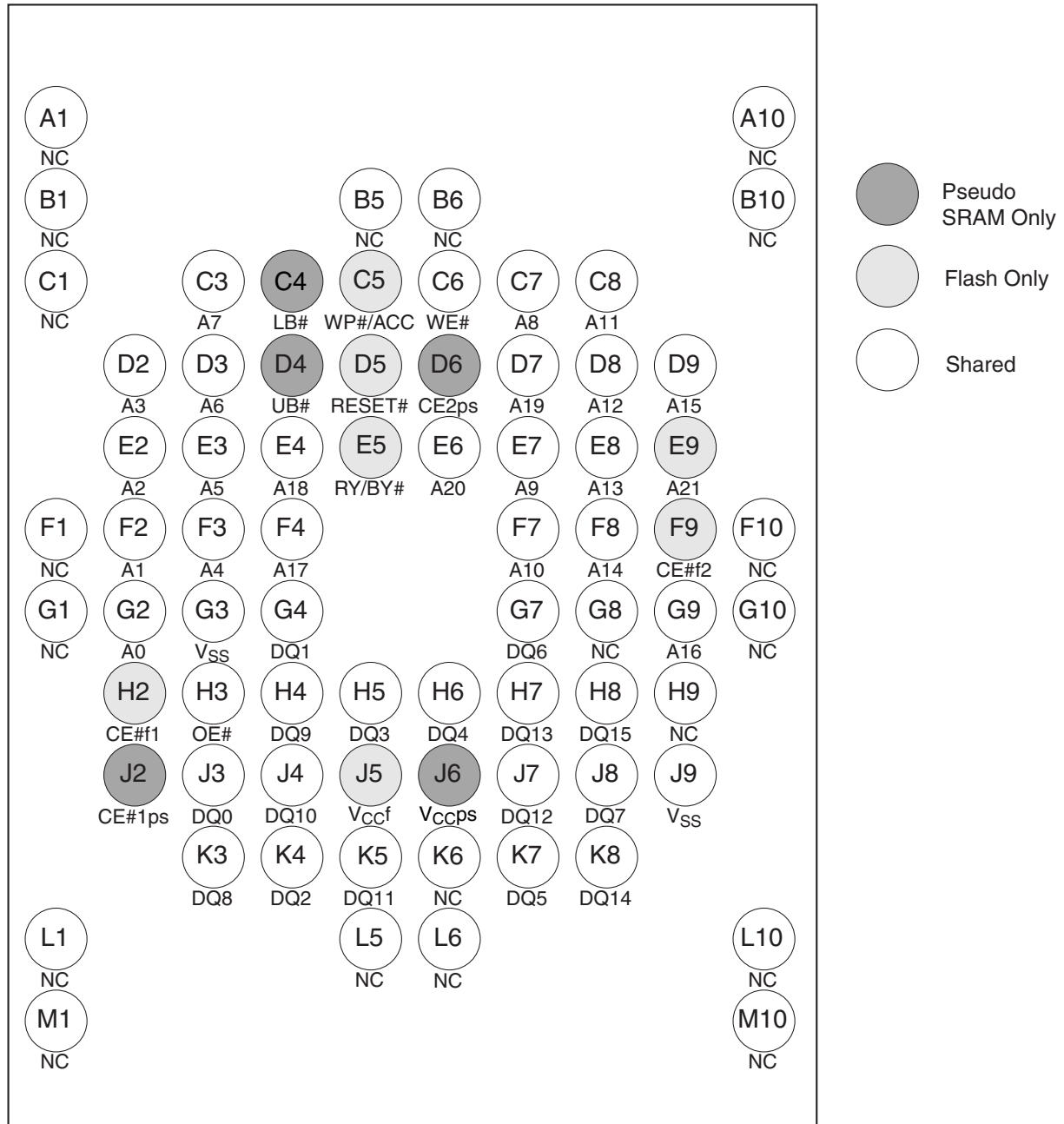
| Part Number          |                                                        | Am49PDL127BH/Am49PDL129BH |    |             |    |
|----------------------|--------------------------------------------------------|---------------------------|----|-------------|----|
| Speed Option         | Standard Voltage Range:<br>V <sub>CC</sub> = 2.7–3.3 V | Flash Memory              |    | Pseudo SRAM |    |
|                      |                                                        | 66                        | 85 | 66          | 85 |
| Max Access Time, ns  |                                                        | 65                        | 85 | 70          | 85 |
| Page Access Time, ns |                                                        | 25                        | 30 | 30          | 35 |
| CE#f1 Access, ns     |                                                        | 65                        | 85 | 70          | 85 |
| OE# Access, ns       |                                                        | 25                        | 30 | 25          | 30 |

## MCP BLOCK DIAGRAM



# CONNECTION DIAGRAM-PDL129

73-Ball FBGA  
Top View

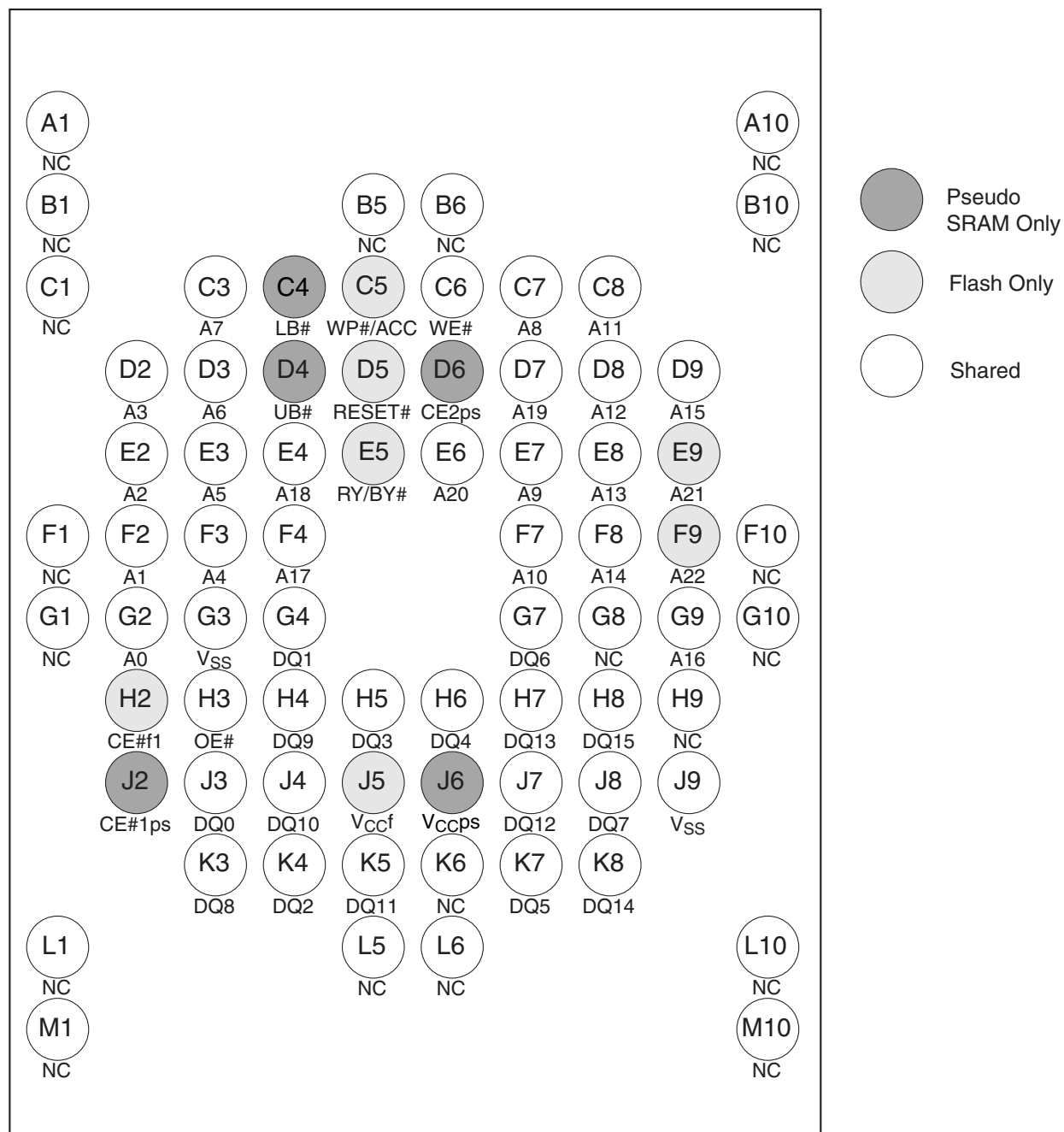


## Special Package Handling Instructions

Special handling is required for Flash Memory products in molded packages (BGA). The package and/or data integrity may be compromised if the package body is

exposed to temperatures above 150°C for prolonged periods of time.

## CONNECTION DIAGRAM—PDL127

73-Ball FBGA  
Top View**Special Package Handling Instructions**

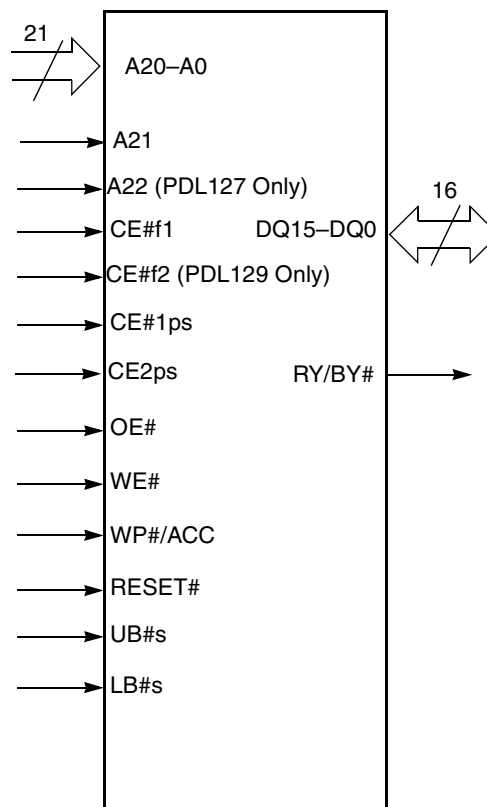
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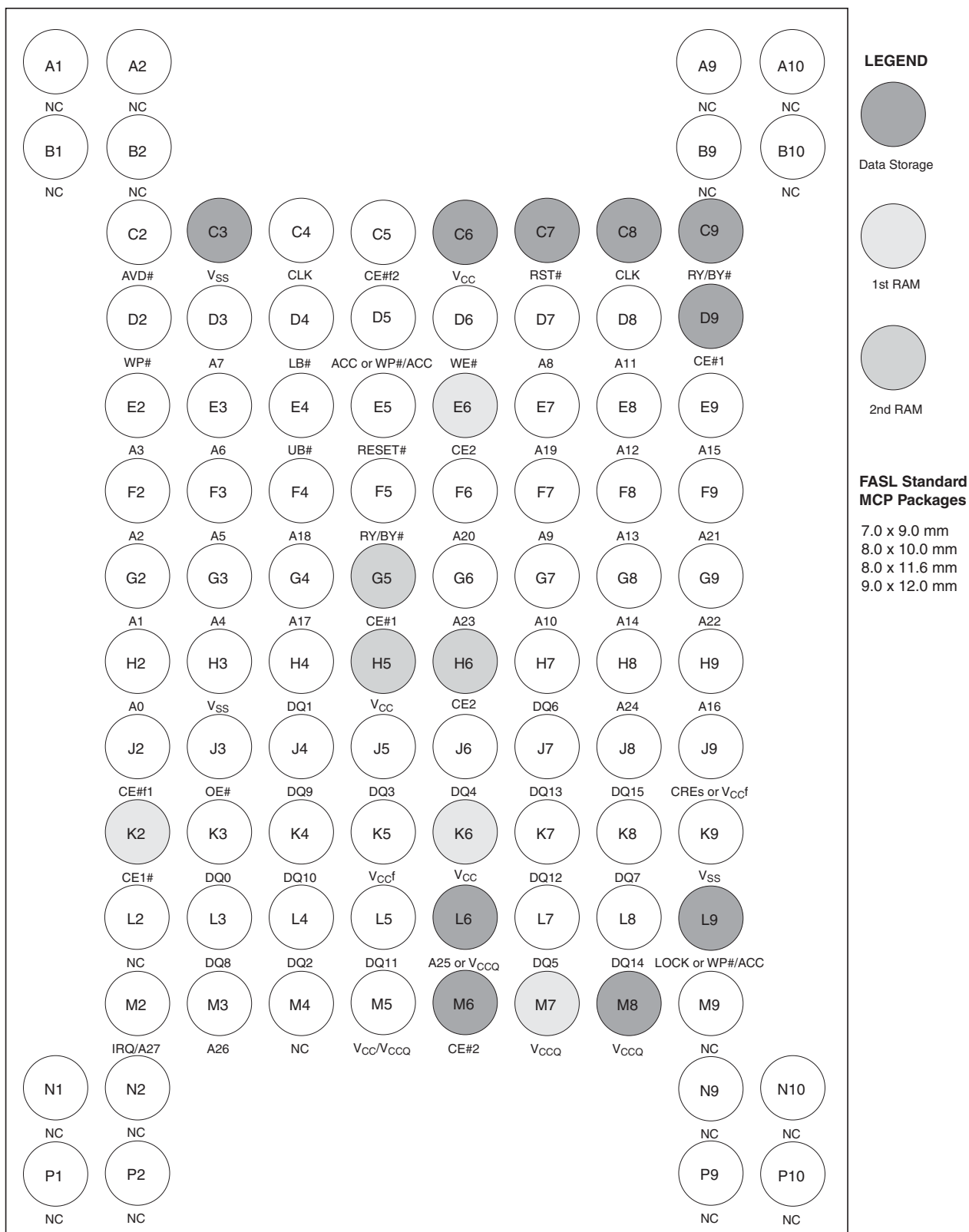
## PIN DESCRIPTION

|            |                                                                                                                                                                                                                                                                                                                                                  |
|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A20–A0     | = 21 Address Inputs (Common)                                                                                                                                                                                                                                                                                                                     |
| A21        | = Address Inputs (Flash)                                                                                                                                                                                                                                                                                                                         |
| A22        | = Address Input (PDL127 only) (Flash)                                                                                                                                                                                                                                                                                                            |
| DQ15–DQ0   | = 16 Data Inputs/Outputs (Common)                                                                                                                                                                                                                                                                                                                |
| CE#f1      | = Chip Enable 1 (Flash)                                                                                                                                                                                                                                                                                                                          |
| CE#f2      | = Chip Enable 2 (Flash) (PDL 129 only)                                                                                                                                                                                                                                                                                                           |
| CE#1ps     | = Chip Enable 1 (pSRAM)                                                                                                                                                                                                                                                                                                                          |
| CE2ps      | = Chip Enable 2 (pSRAM)                                                                                                                                                                                                                                                                                                                          |
| OE#        | = Output Enable (Common)                                                                                                                                                                                                                                                                                                                         |
| WE#        | = Write Enable (Common)                                                                                                                                                                                                                                                                                                                          |
| RY/BY#     | = Ready/Busy Output and open drain. When RY/BY# = $V_{IH}$ , the device is ready to accept read operations and commands. When RY/BY# = $V_{OL}$ , the device is either executing an embedded algorithm or the device is executing a hardware reset operation.                                                                                    |
| UB#s       | = Upper Byte Control (pSRAM)                                                                                                                                                                                                                                                                                                                     |
| LB#s       | = Lower Byte Control (pSRAM)                                                                                                                                                                                                                                                                                                                     |
| RESET#     | = Hardware Reset Pin, Active Low                                                                                                                                                                                                                                                                                                                 |
| WP#/ACC    | = Write Protect/Acceleration Input. When WP/ACC# = $V_{IL}$ , the highest and lowest two 4K-word sectors are write protected regardless of other sector protection configurations. When WP/ACC# = $V_{IH}$ , these sector are unprotected unless the DYB or PPB is programmed. When WP/ACC# = 12V, program and erase operations are accelerated. |
| $V_{CC}^f$ | = Flash 3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)                                                                                                                                                                                                                           |
| $V_{CC}^s$ | = pSRAM Power Supply                                                                                                                                                                                                                                                                                                                             |
| $V_{SS}$   | = Device Ground (Common)                                                                                                                                                                                                                                                                                                                         |
| NC         | = Pin Not Connected Internally                                                                                                                                                                                                                                                                                                                   |

## LOGIC SYMBOL



## LOOK AHEAD BALLOUT DIAGRAM



**Note:** The future ballouts shown in this diagram represent possible future products with densities up to 4 Gbits of Flash plus 4 Gbits of SRAM. Device combinations include NOR Flash plus SRAM, NOR Flash plus pSRAM, and NOR Flash plus pSRAM plus data storage. Contact a sales representative for device specifications, planned production, and availability before designing in any future product.

To provide customers with a migration path to higher densities, as well as the option of stacking more die in one package, the preceding diagram shows a look-ahead ballout that supports:

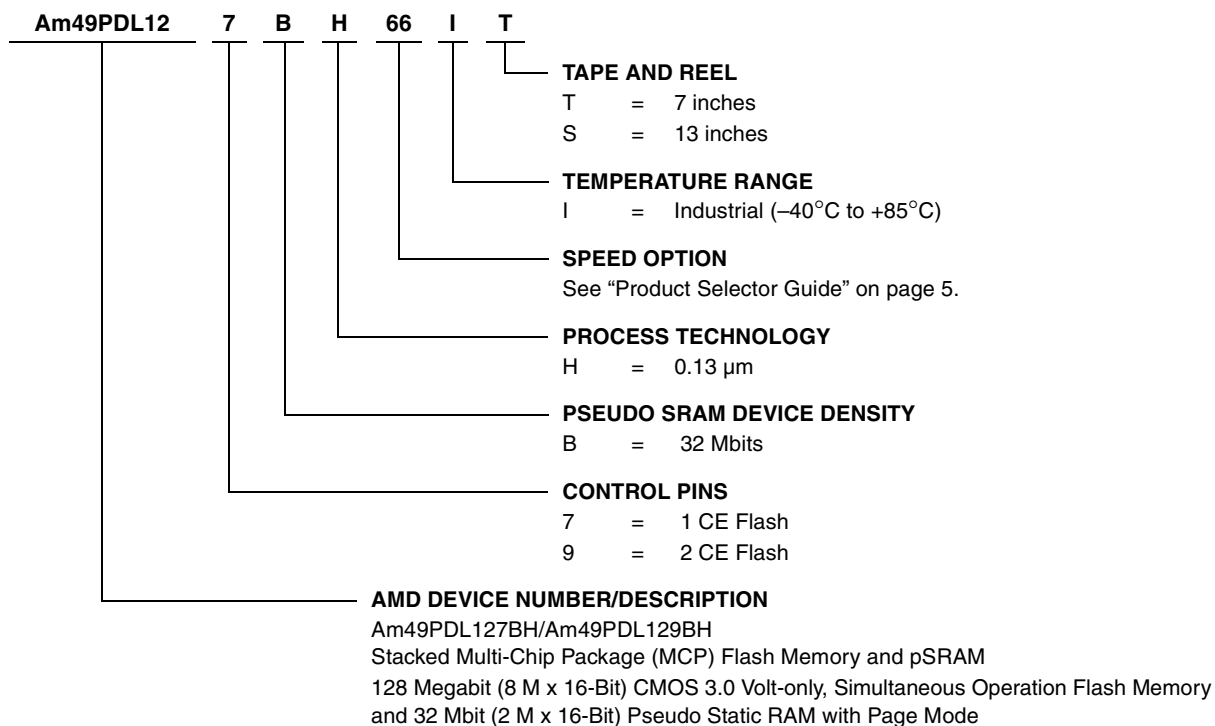
- NOR Flash and SRAM densities up to 4 Gigabits
- NOR Flash and PSRAM densities up to 4 Gigabits
- NOR Flash and PSRAM and DATA STORAGE densities up to 4 Gigabits

The signal locations of the resultant MCP device are shown in the diagram. Note that for different densities, the actual package outline may vary. However, any ballout in any MCP will be a subset of the ballout diagram shown.

In some cases, there may be outrigger balls in locations outside the grid shown. Do not connect these outrigger balls to any signal. For further information regarding the look-ahead ballout, contact the appropriate AMD or Fujitsu sales office.

## ORDERING INFORMATION

The order number (Valid Combination) is formed by the following:



## Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

| Valid Combinations |      |                 |
|--------------------|------|-----------------|
| Order Number       |      | Package Marking |
| Am49PDL127BH66I    | T, S | M490000028      |
| Am49PDL127BH85I    | T, S | M490000029      |
| Am49PDL129BH66I    | T, S | M490000030      |
| Am49PDL129BH85I    | T, S | M490000031      |

## MCP DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information

needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Tables 1-2 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Device Bus Operations

| Operation<br>(Notes 1, 2)           |          | CE#f1<br>Active         | CE#f2<br>(PDL129<br>only) | CE#1ps | CE2ps | OE# | WE# | Addr.                                 | LB#s<br>(Note<br>3) | UB#s<br>(Note<br>3) | RESET#                  | WP#/<br>ACC<br>(Note 4) | DQ7–<br>DQ0      | DQ15–<br>DQ8     |
|-------------------------------------|----------|-------------------------|---------------------------|--------|-------|-----|-----|---------------------------------------|---------------------|---------------------|-------------------------|-------------------------|------------------|------------------|
| Read from<br>Active Flash           | (Note 7) | L (H)                   | H (L)                     | H      | H     | L   | H   | A <sub>IN</sub>                       | X                   | X                   | H                       | L/H                     | D <sub>OUT</sub> | D <sub>OUT</sub> |
|                                     | (Note 8) |                         |                           | H      | L     |     |     |                                       |                     |                     |                         |                         |                  |                  |
| Write to Active<br>Flash            | (Note 7) | L (H)                   | H (L)                     | H      | H     | H   | L   | A <sub>IN</sub>                       | X                   | X                   | H                       | (Note 4)                | D <sub>IN</sub>  | D <sub>IN</sub>  |
|                                     | (Note 8) |                         |                           | H      | L     |     |     |                                       |                     |                     |                         |                         |                  |                  |
| Standby                             |          | V <sub>CC</sub> ± 0.3 V |                           | H      | H     | X   | X   | X                                     | X                   | X                   | V <sub>CC</sub> ± 0.3 V | H                       | High-Z           | High-Z           |
| Deep Power-down<br>Standby          |          | V <sub>CC</sub> ± 0.3 V |                           | H      | L     | X   | X   | X                                     | X                   | X                   | V <sub>CC</sub> ± 0.3 V | H                       | High-Z           | High-Z           |
| Output Disable (Note 9)             |          | L (H)                   | H (L)                     | L      | H     | H   | H   | X                                     | X                   | X                   | H                       | L/H                     | High-Z           | High-Z           |
|                                     |          |                         |                           |        |       | H   | H   | X                                     | X                   | X                   |                         |                         |                  |                  |
| Flash Hardware<br>Reset             | (Note 7) | X                       |                           | H      | H     | X   | X   | X                                     | X                   | X                   | L                       | L/H                     | High-Z           | High-Z           |
|                                     | (Note 8) |                         |                           | H      | L     |     |     |                                       |                     |                     |                         |                         |                  |                  |
| Sector Protect<br>(Notes 6, 10)     | (Note 7) | L (H)                   | H (L)                     | H      | H     | H   | L   | SADD,<br>A6 = L,<br>A1 = H,<br>A0 = L | X                   | X                   | V <sub>ID</sub>         | L/H                     | D <sub>IN</sub>  | X                |
|                                     | (Note 9) |                         |                           | H      | L     |     |     |                                       |                     |                     |                         |                         |                  |                  |
| Sector<br>Unprotect<br>(Notes 5, 9) | (Note 7) | L (H)                   | H (L)                     | H      | H     | H   | L   | SADD,<br>A6 = H,<br>A1 = H,<br>A0 = L | X                   | X                   | V <sub>ID</sub>         | (Note 6)                | D <sub>IN</sub>  | X                |
|                                     | (Note 8) |                         |                           | H      | L     |     |     |                                       |                     |                     |                         |                         |                  |                  |
| Temporary<br>Sector<br>Unprotect    | (Note 7) | X                       |                           | H      | H     | X   | X   | X                                     | X                   | X                   | V <sub>ID</sub>         | (Note 6)                | D <sub>IN</sub>  | High-Z           |
|                                     | (Note 8) |                         |                           | H      | L     |     |     |                                       |                     |                     |                         |                         |                  |                  |
| Read from pSRAM                     |          | H                       | H                         | L      | H     | L   | H   | A <sub>IN</sub>                       | L                   | L                   | H                       | X                       | D <sub>OUT</sub> | D <sub>OUT</sub> |
|                                     |          |                         |                           |        |       |     |     |                                       | H                   | L                   |                         |                         | High-Z           | D <sub>OUT</sub> |
|                                     |          |                         |                           |        |       |     |     |                                       | L                   | H                   |                         |                         | D <sub>OUT</sub> | High-Z           |
| Write to pSRAM                      |          | H                       | H                         | L      | H     | X   | L   | A <sub>IN</sub>                       | L                   | L                   | H                       | X                       | D <sub>IN</sub>  | D <sub>IN</sub>  |
|                                     |          |                         |                           |        |       |     |     |                                       | H                   | L                   |                         |                         | High-Z           | D <sub>IN</sub>  |
|                                     |          |                         |                           |        |       |     |     |                                       | L                   | H                   |                         |                         | D <sub>IN</sub>  | High-Z           |

**Legend:** L = Logic Low =  $V_{IL}$ , H = Logic High =  $V_{IH}$ ,  $V_{ID} = 11.5-12.5 V$ ,  $V_{HH} = 9.0 \pm 0.5 V$ , X = Don't Care, SADD = Flash Sector Address,  $A_{IN}$  = Address In,  $D_{IN}$  = Data In,  $D_{OUT}$  = Data Out

**Notes:**

- Other operations except for those indicated in this column are inhibited.
- Do not apply CE#f1 or 2 =  $V_{IL}$ , CE#1ps =  $V_{IL}$  and CE2ps =  $V_{IH}$  at the same time.
- Don't care or open LB#s or UB#s.
- If WP#/ACC =  $V_{IL}$ , the boot sectors will be protected. If WP#/ACC =  $V_{IH}$ , the boot sectors protection will be removed. If WP#/ACC =  $V_{ACC}$  (9V), the program time will be reduced by 40%.
- The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector/Sector Block Protection and Unprotection" section.
- If WP#/ACC =  $V_{IL}$ , the two outermost boot sectors remain protected. If WP#/ACC =  $V_{IH}$ , the two outermost boot sector protection depends on whether they were last protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotection". If WP#/ACC =  $V_{HH}$ , all sectors will be unprotected.
- Data will be retained in pSRAM.
- Data will be lost in pSRAM.
- Both CE#f1 inputs may be held low for this operation.

## Requirements for Reading Array Data

To read array data from the outputs, the system must drive the OE# and appropriate CE#f1/CE#f2 (PDL129 only) pins to  $V_{IL}$ . CE#f1 and CE#f2 are the power control and for PDL129 select the lower (CE#f1) or upper (CE#f2) halves of the device. OE# is the output control and gates array data to the output pins. WE# should remain at  $V_{IH}$ .

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. Each bank remains enabled for read access until the command register contents are altered.

Refer to the Flash AC Characteristics table for timing specifications and to Figure 14 for the timing diagram.  $I_{CC1}$  in the DC Characteristics table represents the active current specification for reading array data.

### Random Read (Non-Page Read)

Address access time ( $t_{ACC}$ ) is equal to the delay from stable addresses to valid output data. The chip enable access time ( $t_{CE}$ ) is the delay from the stable addresses and stable CE#f1 to valid data at the output inputs. The output enable access time is the delay from the falling edge of the OE# to valid data at the output inputs (assuming the addresses have been stable for at least  $t_{ACC}-t_{OE}$  time).

### Page Mode Read

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. Address bits A22–A3 (A21–A3 for PDL129) select an 8-word page, and address bits A2–A0 select a specific word within that page. This is an asynchronous operation with the microprocessor supplying the specific word location.

The random or initial page access is  $t_{ACC}$  or  $t_{CE}$  and subsequent page read accesses (as long as the locations specified by the microprocessor fall within that page) are  $t_{PACC}$ . When CE#f1 and CE#f2 (PDL129 only) are deasserted (CE#f1=CE#f2= $V_{IH}$ ), the reassertion of CE#f1 or CE#f2 (PDL129 only) for subsequent access has access time of  $t_{ACC}$  or  $t_{CE}$ . Here again, CE#f1/CE#f2 (PDL129 only) selects the device and OE# is the output control and should be used to gate data to the output inputs if the device is selected. Fast

page mode accesses are obtained by keeping A22–A3 (A21–A3 for PDL129) constant and changing A2 to A0 to select the specific word within that page.

**Table 2. Page Select**

| Word   | A2 | A1 | A0 |
|--------|----|----|----|
| Word 0 | 0  | 0  | 0  |
| Word 1 | 0  | 0  | 1  |
| Word 2 | 0  | 1  | 0  |
| Word 3 | 0  | 1  | 1  |
| Word 4 | 1  | 0  | 0  |
| Word 5 | 1  | 0  | 1  |
| Word 6 | 1  | 1  | 0  |
| Word 7 | 1  | 1  | 1  |

## Simultaneous Operation

In addition to the conventional features (read, program, erase-suspend read, and erase-suspend program), the device is capable of reading data from one bank of memory while a program or erase operation is in progress in another bank of memory (simultaneous operation). The bank can be selected by bank addresses (A22–A20) (A21–A20 for PDL129) with zero latency.

The simultaneous operation can execute multi-function mode in the same bank.

**Table 3. Bank Select (PDL129H)**

| Bank   | CE#f1 | CE#f2 | A21–A20    |
|--------|-------|-------|------------|
| Bank A | 0     | 1     | 00, 01, 10 |
| Bank B | 0     | 1     | 11         |
| Bank C | 1     | 0     | 00         |
| Bank D | 1     | 0     | 01, 10, 11 |

**Table 4. Bank Select (PDL127H)**

| Bank   | A22–A20       |
|--------|---------------|
| Bank A | 000           |
| Bank B | 001, 010, 011 |
| Bank C | 100, 101, 110 |
| Bank D | 111           |

## Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE#f1 or CE#f2 (PDL 129 only) to  $V_{IL}$ , and OE# to  $V_{IH}$ .

The device features an **Unlock Bypass** mode to facilitate faster programming. Once a bank enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four. The “Word Program Command Sequence” section has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 4 indicates the address space that each sector occupies. A “bank address” is the address bits required to uniquely select a bank. Similarly, a “sector address” refers to the address bits required to uniquely select a sector. The “Command Definitions” section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

$I_{CC2}$  in the DC Characteristics table represents the active current specification for the write mode. The Flash AC Characteristics section contains timing specification tables and timing diagrams for write operations.

### Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts  $V_{HH}$  on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing  $V_{HH}$  from the WP#/ACC pin returns the device to normal operation. *Note that  $V_{HH}$  must not be asserted on WP#/ACC for operations other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin should be raised to  $V_{CC}$  when not in use. That is, the WP#/ACC pin should not be left floating or unconnected; inconsistent behavior of the device may result.*

## Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ15–DQ0. Standard read cycle timings apply in this mode. Refer to the Autoselect Command Sequence sections for more information.

## Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE#f1, CE#f2 (PDL129 only) and RESET# pins are all held at  $V_{IO} \pm 0.3$  V. (Note that this is a more restricted voltage range than  $V_{IH}$ .) If CE#f1, CE#f2 (PDL129 only), and RESET# are held at  $V_{IH}$ , but not within  $V_{CC} \pm 0.3$  V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time ( $t_{CE}$ ) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

$I_{CC3}$  in the DC Characteristics table represents the CMOS standby current specification.

## Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for  $t_{ACC} + 150$  ns. The automatic sleep mode is independent of the CE#f1/CE#f2 (PDL129 only), WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. Note that during automatic sleep mode, OE# must be at  $V_{IH}$  before the device reduces current to the stated sleep mode specification.  $I_{CC5}$  in the DC Characteristics table represents the automatic sleep mode current specification.

## RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of  $t_{RP}$  the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at  $V_{SS} \pm 0.3$  V, the device draws CMOS standby current ( $I_{CC4}$ ). If RESET# is held at  $V_{IL}$  but not within  $V_{SS} \pm 0.3$  V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash

memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a “0” (busy) until the internal reset operation is complete, which requires a time of  $t_{READY}$  (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is “1”), the reset operation is completed within a time of  $t_{READY}$  (not during Embedded Algorithms). The system can read data  $t_{RH}$  after the RESET# pin returns to  $V_{IH}$ .

Refer to the pSRAM AC Characteristics tables for RESET# parameters and to Figure 16 for the timing diagram.

## Output Disable Mode

When the OE# input is at  $V_{IH}$ , output from the device is disabled. The output pins (except for RY/BY#) are placed in the highest Impedance state

Table 5. Am29PDL127H Sector Architecture

| Bank   | Sector | Sector Address (A22-A12) | Sector Size (Kwords) | Address Range (x16) |
|--------|--------|--------------------------|----------------------|---------------------|
| Bank A | SA0    | 00000000000              | 4                    | 000000h–000FFFh     |
|        | SA1    | 00000000001              | 4                    | 001000h–001FFFh     |
|        | SA2    | 00000000010              | 4                    | 002000h–002FFFh     |
|        | SA3    | 00000000011              | 4                    | 003000h–003FFFh     |
|        | SA4    | 00000000100              | 4                    | 004000h–004FFFh     |
|        | SA5    | 00000000101              | 4                    | 005000h–005FFFh     |
|        | SA6    | 00000000110              | 4                    | 006000h–006FFFh     |
|        | SA7    | 00000000111              | 4                    | 007000h–007FFFh     |
|        | SA8    | 00000001XXX              | 32                   | 008000h–00FFFFh     |
|        | SA9    | 00000010XXX              | 32                   | 010000h–017FFFh     |
|        | SA10   | 00000011XXX              | 32                   | 018000h–01FFFFh     |
|        | SA11   | 00000100XXX              | 32                   | 020000h–027FFFh     |
|        | SA12   | 00000101XXX              | 32                   | 028000h–02FFFFh     |
|        | SA13   | 00000110XXX              | 32                   | 030000h–037FFFh     |
|        | SA14   | 00000111XXX              | 32                   | 038000h–03FFFFh     |
|        | SA15   | 00001000XXX              | 32                   | 040000h–047FFFh     |
|        | SA16   | 00001001XXX              | 32                   | 048000h–04FFFFh     |
|        | SA17   | 00001010XXX              | 32                   | 050000h–057FFFh     |
|        | SA18   | 00001011XXX              | 32                   | 058000h–05FFFFh     |
|        | SA19   | 00001100XXX              | 32                   | 060000h–067FFFh     |
|        | SA20   | 00001101XXX              | 32                   | 068000h–06FFFFh     |
|        | SA21   | 00001110XXX              | 32                   | 070000h–077FFFh     |
|        | SA22   | 00001111XXX              | 32                   | 078000h–07FFFFh     |
|        | SA23   | 00010000XXX              | 32                   | 080000h–087FFFh     |
|        | SA24   | 00010001XXX              | 32                   | 088000h–08FFFFh     |
|        | SA25   | 00010010XXX              | 32                   | 090000h–097FFFh     |
|        | SA26   | 00010011XXX              | 32                   | 098000h–09FFFFh     |
|        | SA27   | 00010100XXX              | 32                   | 0A0000h–0A7FFFh     |
|        | SA28   | 00010101XXX              | 32                   | 0A8000h–0AFFFFh     |
|        | SA29   | 00010110XXX              | 32                   | 0B0000h–0B7FFFh     |
|        | SA30   | 00010111XXX              | 32                   | 0B8000h–0BFFFFh     |
|        | SA31   | 00011000XXX              | 32                   | 0C0000h–0C7FFFh     |
|        | SA32   | 00011001XXX              | 32                   | 0C8000h–0CFFFFh     |
|        | SA33   | 00011010XXX              | 32                   | 0D0000h–0D7FFFh     |
|        | SA34   | 00011011XXX              | 32                   | 0D8000h–0DFFFFh     |
|        | SA35   | 00011100XXX              | 32                   | 0E0000h–0E7FFFh     |
|        | SA36   | 00011101XXX              | 32                   | 0E8000h–0EFFFFh     |
|        | SA37   | 00011110XXX              | 32                   | 0F0000h–0F7FFFh     |
|        | SA38   | 00011111XXX              | 32                   | 0F8000h–0FFFFFh     |
| Bank   | Sector | Sector Address (A22-A12) | Sector Size (Kwords) | Address Range (x16) |

Table 5. Am29PDL127H Sector Architecture (Continued)

|        |      |             |    |                 |
|--------|------|-------------|----|-----------------|
| Bank B | SA39 | 00100000XXX | 32 | 100000h–107FFFh |
|        | SA40 | 00100001XXX | 32 | 108000h–10FFFFh |
|        | SA41 | 00100010XXX | 32 | 110000h–117FFFh |
|        | SA42 | 00100011XXX | 32 | 118000h–11FFFFh |
|        | SA43 | 00100100XXX | 32 | 120000h–127FFFh |
|        | SA44 | 00100101XXX | 32 | 128000h–12FFFFh |
|        | SA45 | 00100110XXX | 32 | 130000h–137FFFh |
|        | SA46 | 00100111XXX | 32 | 138000h–13FFFFh |
|        | SA47 | 00101000XXX | 32 | 140000h–147FFFh |
|        | SA48 | 00101001XXX | 32 | 148000h–14FFFFh |
|        | SA49 | 00101010XXX | 32 | 150000h–157FFFh |
|        | SA50 | 00101011XXX | 32 | 158000h–15FFFFh |
|        | SA51 | 00101100XXX | 32 | 160000h–167FFFh |
|        | SA52 | 00101101XXX | 32 | 168000h–16FFFFh |
|        | SA53 | 00101110XXX | 32 | 170000h–177FFFh |
|        | SA54 | 00101111XXX | 32 | 178000h–17FFFFh |
|        | SA55 | 00110000XXX | 32 | 180000h–187FFFh |
|        | SA56 | 00110001XXX | 32 | 188000h–18FFFFh |
|        | SA57 | 00110010XXX | 32 | 190000h–197FFFh |
|        | SA58 | 00110011XXX | 32 | 198000h–19FFFFh |
|        | SA59 | 00110100XXX | 32 | 1A0000h–1A7FFFh |
|        | SA60 | 00110101XXX | 32 | 1A8000h–1AFFFFh |
|        | SA61 | 00110110XXX | 32 | 1B0000h–1B7FFFh |
|        | SA62 | 00110111XXX | 32 | 1B8000h–1BFFFFh |
|        | SA63 | 00111000XXX | 32 | 1C0000h–1C7FFFh |
|        | SA64 | 00111001XXX | 32 | 1C8000h–1CFFFFh |
|        | SA65 | 00111010XXX | 32 | 1D0000h–1D7FFFh |
|        | SA66 | 00111011XXX | 32 | 1D8000h–1DFFFFh |
|        | SA67 | 00111100XXX | 32 | 1E0000h–1E7FFFh |
|        | SA68 | 00111101XXX | 32 | 1E8000h–1EFFFFh |
|        | SA69 | 00111110XXX | 32 | 1F0000h–1F7FFFh |
|        | SA70 | 00111111XXX | 32 | 1F8000h–1FFFFFh |
|        | SA71 | 01000000XXX | 32 | 200000h–207FFFh |
|        | SA72 | 01000001XXX | 32 | 208000h–20FFFFh |
|        | SA73 | 01000010XXX | 32 | 210000h–217FFFh |
|        | SA74 | 01000011XXX | 32 | 218000h–21FFFFh |
|        | SA75 | 01000100XXX | 32 | 220000h–227FFFh |
|        | SA76 | 01000101XXX | 32 | 228000h–22FFFFh |
|        | SA77 | 01000110XXX | 32 | 230000h–237FFFh |
|        | SA78 | 01000111XXX | 32 | 238000h–23FFFFh |

| Bank | Sector | Sector Address (A22-A12) | Sector Size (Kwords) | Address Range (x16) |
|------|--------|--------------------------|----------------------|---------------------|
|------|--------|--------------------------|----------------------|---------------------|

Table 5. Am29PDL127H Sector Architecture (Continued)

|        |       |             |    |                 |
|--------|-------|-------------|----|-----------------|
| Bank B | SA79  | 01001000XXX | 32 | 240000h–247FFFh |
|        | SA80  | 01001001XXX | 32 | 248000h–24FFFFh |
|        | SA81  | 01001010XXX | 32 | 250000h–257FFFh |
|        | SA82  | 01001011XXX | 32 | 258000h–25FFFFh |
|        | SA83  | 01001100XXX | 32 | 260000h–267FFFh |
|        | SA84  | 01001101XXX | 32 | 268000h–26FFFFh |
|        | SA85  | 01001110XXX | 32 | 270000h–277FFFh |
|        | SA86  | 01001111XXX | 32 | 278000h–27FFFFh |
|        | SA87  | 01010000XXX | 32 | 280000h–287FFFh |
|        | SA88  | 01010001XXX | 32 | 288000h–28FFFFh |
|        | SA89  | 01010010XXX | 32 | 290000h–297FFFh |
|        | SA90  | 01010011XXX | 32 | 298000h–29FFFFh |
|        | SA91  | 01010100XXX | 32 | 2A0000h–2A7FFFh |
|        | SA92  | 01010101XXX | 32 | 2A8000h–2AFFFFh |
|        | SA93  | 01010110XXX | 32 | 2B0000h–2B7FFFh |
|        | SA94  | 01010111XXX | 32 | 2B8000h–2BFFFFh |
|        | SA95  | 01011000XXX | 32 | 2C0000h–2C7FFFh |
|        | SA96  | 01011001XXX | 32 | 2C8000h–2CFFFFh |
|        | SA97  | 01011010XXX | 32 | 2D0000h–2D7FFFh |
|        | SA98  | 01011011XXX | 32 | 2D8000h–2DFFFFh |
|        | SA99  | 01011100XXX | 32 | 2E0000h–2E7FFFh |
|        | SA100 | 01011101XXX | 32 | 2E8000h–2EFFFFh |
|        | SA101 | 01011110XXX | 32 | 2F0000h–2F7FFFh |
|        | SA102 | 01011111XXX | 32 | 2F8000h–2FFFFFh |
|        | SA103 | 01100000XXX | 32 | 300000h–307FFFh |
|        | SA104 | 01100001XXX | 32 | 308000h–30FFFFh |
|        | SA105 | 01100010XXX | 32 | 310000h–317FFFh |
|        | SA106 | 01100011XXX | 32 | 318000h–31FFFFh |
|        | SA107 | 01100100XXX | 32 | 320000h–327FFFh |
|        | SA108 | 01100101XXX | 32 | 328000h–32FFFFh |
|        | SA109 | 01100110XXX | 32 | 330000h–337FFFh |
|        | SA110 | 01100111XXX | 32 | 338000h–33FFFFh |
|        | SA111 | 01101000XXX | 32 | 340000h–347FFFh |
|        | SA112 | 01101001XXX | 32 | 348000h–34FFFFh |
|        | SA113 | 01101010XXX | 32 | 350000h–357FFFh |
|        | SA114 | 01101011XXX | 32 | 358000h–35FFFFh |
|        | SA115 | 01101100XXX | 32 | 360000h–367FFFh |
|        | SA116 | 01101101XXX | 32 | 368000h–36FFFFh |
|        | SA117 | 01101110XXX | 32 | 370000h–377FFFh |
|        | SA118 | 01101111XXX | 32 | 378000h–37FFFFh |

| Bank | Sector | Sector Address (A22-A12) | Sector Size (Kwords) | Address Range (x16) |
|------|--------|--------------------------|----------------------|---------------------|
|------|--------|--------------------------|----------------------|---------------------|

Table 5. Am29PDL127H Sector Architecture (Continued)

|        |       |             |    |                 |
|--------|-------|-------------|----|-----------------|
| Bank B | SA119 | 01110000XXX | 32 | 380000h–387FFFh |
|        | SA120 | 01110001XXX | 32 | 388000h–38FFFFh |
|        | SA121 | 01110010XXX | 32 | 390000h–397FFFh |
|        | SA122 | 01110011XXX | 32 | 398000h–39FFFFh |
|        | SA123 | 01110100XXX | 32 | 3A0000h–3A7FFFh |
|        | SA124 | 01110101XXX | 32 | 3A8000h–3AFFFFh |
|        | SA125 | 01110110XXX | 32 | 3B0000h–3B7FFFh |
|        | SA126 | 01110111XXX | 32 | 3B8000h–3BFFFFh |
|        | SA127 | 01111000XXX | 32 | 3C0000h–3C7FFFh |
|        | SA128 | 01111001XXX | 32 | 3C8000h–3CFFFFh |
|        | SA129 | 01111010XXX | 32 | 3D0000h–3D7FFFh |
|        | SA130 | 01111011XXX | 32 | 3D8000h–3DFFFFh |
|        | SA131 | 01111100XXX | 32 | 3E0000h–3E7FFFh |
|        | SA132 | 01111101XXX | 32 | 3E8000h–3EFFFFh |
|        | SA133 | 01111110XXX | 32 | 3F0000h–3F7FFFh |
|        | SA134 | 01111111XXX | 32 | 3F8000h–3FFFFFh |
| Bank C | SA135 | 10000000XXX | 32 | 400000h–407FFFh |
|        | SA136 | 10000001XXX | 32 | 408000h–40FFFFh |
|        | SA137 | 10000010XXX | 32 | 410000h–417FFFh |
|        | SA138 | 10000011XXX | 32 | 418000h–41FFFFh |
|        | SA139 | 10000100XXX | 32 | 420000h–427FFFh |
|        | SA140 | 10000101XXX | 32 | 428000h–42FFFFh |
|        | SA141 | 10000110XXX | 32 | 430000h–437FFFh |
|        | SA142 | 10000111XXX | 32 | 438000h–43FFFFh |
|        | SA143 | 10001000XXX | 32 | 440000h–447FFFh |
|        | SA144 | 10001001XXX | 32 | 448000h–44FFFFh |
|        | SA145 | 10001010XXX | 32 | 450000h–457FFFh |
|        | SA146 | 10001011XXX | 32 | 458000h–45FFFFh |
|        | SA147 | 10001100XXX | 32 | 460000h–467FFFh |
|        | SA148 | 10001101XXX | 32 | 468000h–46FFFFh |
|        | SA149 | 10001110XXX | 32 | 470000h–477FFFh |
|        | SA150 | 10001111XXX | 32 | 478000h–47FFFFh |
|        | SA151 | 10010000XXX | 32 | 480000h–487FFFh |
|        | SA152 | 10010001XXX | 32 | 488000h–48FFFFh |
|        | SA153 | 10010010XXX | 32 | 490000h–497FFFh |
|        | SA154 | 10010011XXX | 32 | 498000h–49FFFFh |
|        | SA155 | 10010100XXX | 32 | 4A0000h–4A7FFFh |
|        | SA156 | 10010101XXX | 32 | 4A8000h–4AFFFFh |
|        | SA157 | 10010110XXX | 32 | 4B0000h–4B7FFFh |
|        | SA158 | 10010111XXX | 32 | 4B8000h–4BFFFFh |

| Bank | Sector | Sector Address (A22-A12) | Sector Size (Kwords) | Address Range (x16) |
|------|--------|--------------------------|----------------------|---------------------|
|------|--------|--------------------------|----------------------|---------------------|

Table 5. Am29PDL127H Sector Architecture (Continued)

|        |       |             |    |                  |
|--------|-------|-------------|----|------------------|
| Bank C | SA159 | 10011000XXX | 32 | 4C0000h–4C7FFFh  |
|        | SA160 | 10011001XXX | 32 | 4C8000h–4CFFFFh  |
|        | SA161 | 10011010XXX | 32 | 4D0000h–4D7FFFh  |
|        | SA162 | 10011011XXX | 32 | 4D8000h–4DFFFFh  |
|        | SA163 | 10011100XXX | 32 | 4E0000h–4E7FFFh  |
|        | SA164 | 10011101XXX | 32 | 4E8000h–4EFFFFh  |
|        | SA165 | 10011110XXX | 32 | 4F0000h–4F7FFFh  |
|        | SA166 | 10011111XXX | 32 | 4F8000h–4FFFFFFh |
|        | SA167 | 10100000XXX | 32 | 500000h–507FFFh  |
|        | SA168 | 10100001XXX | 32 | 508000h–50FFFFh  |
|        | SA169 | 10100010XXX | 32 | 510000h–517FFFh  |
|        | SA170 | 10100011XXX | 32 | 518000h–51FFFFh  |
|        | SA171 | 10100100XXX | 32 | 520000h–527FFFh  |
|        | SA172 | 10100101XXX | 32 | 528000h–52FFFFh  |
|        | SA173 | 10100110XXX | 32 | 530000h–537FFFh  |
|        | SA174 | 10100111XXX | 32 | 538000h–53FFFFh  |
|        | SA175 | 10101000XXX | 32 | 540000h–547FFFh  |
|        | SA176 | 10101001XXX | 32 | 548000h–54FFFFh  |
|        | SA177 | 10101010XXX | 32 | 550000h–557FFFh  |
|        | SA178 | 10101011XXX | 32 | 558000h–55FFFFh  |
|        | SA179 | 10101100XXX | 32 | 560000h–567FFFh  |
|        | SA180 | 10101101XXX | 32 | 568000h–56FFFFh  |
|        | SA181 | 10101110XXX | 32 | 570000h–577FFFh  |
|        | SA182 | 10101111XXX | 32 | 578000h–57FFFFh  |
|        | SA183 | 10110000XXX | 32 | 580000h–587FFFh  |
|        | SA184 | 10110001XXX | 32 | 588000h–58FFFFh  |
|        | SA185 | 10110010XXX | 32 | 590000h–597FFFh  |
|        | SA186 | 10110011XXX | 32 | 598000h–59FFFFh  |
|        | SA187 | 10110100XXX | 32 | 5A0000h–5A7FFFh  |
|        | SA188 | 10110101XXX | 32 | 5A8000h–5AFFFFh  |
|        | SA189 | 10110110XXX | 32 | 5B0000h–5B7FFFh  |
|        | SA190 | 10110111XXX | 32 | 5B8000h–5BFFFFh  |
|        | SA191 | 10111000XXX | 32 | 5C0000h–5C7FFFh  |
|        | SA192 | 10111001XXX | 32 | 5C8000h–5CFFFFh  |
|        | SA193 | 10111010XXX | 32 | 5D0000h–5D7FFFh  |
|        | SA194 | 10111011XXX | 32 | 5D8000h–5DFFFFh  |
|        | SA195 | 10111100XXX | 32 | 5E0000h–5E7FFFh  |
|        | SA196 | 10111101XXX | 32 | 5E8000h–5EFFFFh  |
|        | SA197 | 10111110XXX | 32 | 5F0000h–5F7FFFh  |
|        | SA198 | 10111111XXX | 32 | 5F8000h–5FFFFFFh |

| Bank | Sector | Sector Address (A22-A12) | Sector Size (Kwords) | Address Range (x16) |
|------|--------|--------------------------|----------------------|---------------------|
|------|--------|--------------------------|----------------------|---------------------|

**Table 5. Am29PDL127H Sector Architecture (Continued)**

|        |       |             |    |                 |
|--------|-------|-------------|----|-----------------|
| Bank C | SA199 | 11000000XXX | 32 | 600000h–607FFFh |
|        | SA200 | 11000001XXX | 32 | 608000h–60FFFFh |
|        | SA201 | 11000010XXX | 32 | 610000h–617FFFh |
|        | SA202 | 11000011XXX | 32 | 618000h–61FFFFh |
|        | SA203 | 11000100XXX | 32 | 620000h–627FFFh |
|        | SA204 | 11000101XXX | 32 | 628000h–62FFFFh |
|        | SA205 | 11000110XXX | 32 | 630000h–637FFFh |
|        | SA206 | 11000111XXX | 32 | 638000h–63FFFFh |
|        | SA207 | 11001000XXX | 32 | 640000h–647FFFh |
|        | SA208 | 11001001XXX | 32 | 648000h–64FFFFh |
|        | SA209 | 11001010XXX | 32 | 650000h–657FFFh |
|        | SA210 | 11001011XXX | 32 | 658000h–65FFFFh |
|        | SA211 | 11001100XXX | 32 | 660000h–667FFFh |
|        | SA212 | 11001101XXX | 32 | 668000h–66FFFFh |
|        | SA213 | 11001110XXX | 32 | 670000h–677FFFh |
|        | SA214 | 11001111XXX | 32 | 678000h–67FFFFh |
|        | SA215 | 11010000XXX | 32 | 680000h–687FFFh |
|        | SA216 | 11010001XXX | 32 | 688000h–68FFFFh |
|        | SA217 | 11010010XXX | 32 | 690000h–697FFFh |
|        | SA218 | 11010011XXX | 32 | 698000h–69FFFFh |
|        | SA219 | 11010100XXX | 32 | 6A0000h–6A7FFFh |
|        | SA220 | 11010101XXX | 32 | 6A8000h–6AFFFFh |
|        | SA221 | 11010110XXX | 32 | 6B0000h–6B7FFFh |
|        | SA222 | 11010111XXX | 32 | 6B8000h–6BFFFFh |
|        | SA223 | 11011000XXX | 32 | 6C0000h–6C7FFFh |
|        | SA224 | 11011001XXX | 32 | 6C8000h–6CFFFFh |
|        | SA225 | 11011010XXX | 32 | 6D0000h–6D7FFFh |
|        | SA226 | 11011011XXX | 32 | 6D8000h–6DFFFFh |
|        | SA227 | 11011100XXX | 32 | 6E0000h–6E7FFFh |
|        | SA228 | 11011101XXX | 32 | 6E8000h–6EFFFFh |
|        | SA229 | 11011110XXX | 32 | 6F0000h–6F7FFFh |
|        | SA230 | 11011111XXX | 32 | 6F8000h–6FFFFFh |

Table 5. Am29PDL127H Sector Architecture (Continued)

| Bank   | Sector | Sector Address (A22-A12) | Sector Size (Kwords) | Address Range (x16) |
|--------|--------|--------------------------|----------------------|---------------------|
| Bank D | SA231  | 11100000XXX              | 32                   | 700000h–707FFFh     |
|        | SA232  | 11100001XXX              | 32                   | 708000h–70FFFFh     |
|        | SA233  | 11100010XXX              | 32                   | 710000h–717FFFh     |
|        | SA234  | 11100011XXX              | 32                   | 718000h–71FFFFh     |
|        | SA235  | 11100100XXX              | 32                   | 720000h–727FFFh     |
|        | SA236  | 11100101XXX              | 32                   | 728000h–72FFFFh     |
|        | SA237  | 11100110XXX              | 32                   | 730000h–737FFFh     |
|        | SA238  | 11100111XXX              | 32                   | 738000h–73FFFFh     |
|        | SA239  | 11101000XXX              | 32                   | 740000h–747FFFh     |
|        | SA240  | 11101001XXX              | 32                   | 748000h–74FFFFh     |
|        | SA241  | 11101010XXX              | 32                   | 750000h–757FFFh     |
|        | SA242  | 11101011XXX              | 32                   | 758000h–75FFFFh     |
|        | SA243  | 11101100XXX              | 32                   | 760000h–767FFFh     |
|        | SA244  | 11101101XXX              | 32                   | 768000h–76FFFFh     |
|        | SA245  | 11101110XXX              | 32                   | 770000h–777FFFh     |
|        | SA246  | 11101111XXX              | 32                   | 778000h–77FFFFh     |
|        | SA247  | 11110000XXX              | 32                   | 780000h–787FFFh     |
|        | SA248  | 11110001XXX              | 32                   | 788000h–78FFFFh     |
|        | SA249  | 11110010XXX              | 32                   | 790000h–797FFFh     |
|        | SA250  | 11110011XXX              | 32                   | 798000h–79FFFFh     |
|        | SA251  | 11110100XXX              | 32                   | 7A0000h–7A7FFFh     |
|        | SA252  | 11110101XXX              | 32                   | 7A8000h–7AFFFFh     |
|        | SA253  | 11110110XXX              | 32                   | 7B0000h–7B7FFFh     |
|        | SA254  | 11110111XXX              | 32                   | 7B8000h–7BFFFFh     |
|        | SA255  | 11111000XXX              | 32                   | 7C0000h–7C7FFFh     |
|        | SA256  | 11111001XXX              | 32                   | 7C8000h–7CFFFFh     |
|        | SA257  | 11111010XXX              | 32                   | 7D0000h–7D7FFFh     |
|        | SA258  | 11111011XXX              | 32                   | 7D8000h–7DFFFFh     |
|        | SA259  | 11111100XXX              | 32                   | 7E0000h–7E7FFFh     |
|        | SA260  | 11111101XXX              | 32                   | 7E8000h–7EFFFFh     |
|        | SA261  | 11111110XXX              | 32                   | 7F0000h–7F7FFFh     |
|        | SA262  | 11111111000              | 4                    | 7F8000h–7F8FFFh     |
|        | SA263  | 11111111001              | 4                    | 7F9000h–7F9FFFh     |
|        | SA264  | 11111111010              | 4                    | 7FA000h–7FAFFFh     |
|        | SA265  | 11111111011              | 4                    | 7FB000h–7FBFFFh     |
|        | SA266  | 11111111100              | 4                    | 7FC000h–7FCFFFh     |
|        | SA267  | 11111111101              | 4                    | 7FD000h–7FDFFFh     |
|        | SA268  | 11111111110              | 4                    | 7FE000h–7FEFFFh     |
|        | SA269  | 11111111111              | 4                    | 7FF000h–7FFFFFFh    |

Table 6. Am29PDL129H Sector Architecture

| Bank   | Sector | CE#f1 | CE#f2 | Sector Address (A21-A12) | Sector Size (Kwords) | Address Range (x16) |
|--------|--------|-------|-------|--------------------------|----------------------|---------------------|
| Bank A | SA0    | 0     | 1     | 0000000000               | 4                    | 000000h-000FFFh     |
|        | SA1    | 0     | 1     | 0000000001               | 4                    | 001000h-001FFFh     |
|        | SA2    | 0     | 1     | 0000000010               | 4                    | 002000h-002FFFh     |
|        | SA3    | 0     | 1     | 0000000011               | 4                    | 003000h-003FFFh     |
|        | SA4    | 0     | 1     | 0000000100               | 4                    | 004000h-004FFFh     |
|        | SA5    | 0     | 1     | 0000000001               | 4                    | 005000h-005FFFh     |
|        | SA6    | 0     | 1     | 0000000010               | 4                    | 006000h-006FFFh     |
|        | SA7    | 0     | 1     | 0000000011               | 4                    | 007000h-007FFFh     |
|        | SA8    | 0     | 1     | 0000001XXX               | 32                   | 008000h-00FFFFh     |
|        | SA9    | 0     | 1     | 0000010XXX               | 32                   | 010000h-017FFFh     |
|        | SA10   | 0     | 1     | 0000011XXX               | 32                   | 018000h-01FFFFh     |
|        | SA11   | 0     | 1     | 0000100XXX               | 32                   | 020000h-027FFFh     |
|        | SA12   | 0     | 1     | 0000101XXX               | 32                   | 028000h-02FFFFh     |
|        | SA13   | 0     | 1     | 0000110XXX               | 32                   | 030000h-037FFFh     |
|        | SA14   | 0     | 1     | 0000111XXX               | 32                   | 038000h-03FFFFh     |
|        | SA15   | 0     | 1     | 0001000XXX               | 32                   | 040000h-047FFFh     |
|        | SA16   | 0     | 1     | 0001001XXX               | 32                   | 048000h-04FFFFh     |
|        | SA17   | 0     | 1     | 0001010XXX               | 32                   | 050000h-057FFFh     |
|        | SA18   | 0     | 1     | 0001011XXX               | 32                   | 058000h-05FFFFh     |
|        | SA19   | 0     | 1     | 0001100XXX               | 32                   | 060000h-067FFFh     |
|        | SA20   | 0     | 1     | 0001101XXX               | 32                   | 068000h-06FFFFh     |
|        | SA21   | 0     | 1     | 0001110XXX               | 32                   | 070000h-077FFFh     |
|        | SA22   | 0     | 1     | 0001111XXX               | 32                   | 078000h-07FFFFh     |
|        | SA23   | 0     | 1     | 0010000XXX               | 32                   | 080000h-087FFFh     |
|        | SA24   | 0     | 1     | 0010001XXX               | 32                   | 088000h-08FFFFh     |
|        | SA25   | 0     | 1     | 0010010XXX               | 32                   | 090000h-097FFFh     |
|        | SA26   | 0     | 1     | 0010011XXX               | 32                   | 098000h-09FFFFh     |
|        | SA27   | 0     | 1     | 0010100XXX               | 32                   | 0A0000h-0A7FFFh     |
|        | SA28   | 0     | 1     | 0010101XXX               | 32                   | 0A8000h-0AFFFFh     |
|        | SA29   | 0     | 1     | 0010110XXX               | 32                   | 0B0000h-0B7FFFh     |
|        | SA30   | 0     | 1     | 0010111XXX               | 32                   | 0B8000h-0BFFFFh     |
|        | SA31   | 0     | 1     | 0011000XXX               | 32                   | 0C0000h-0C7FFFh     |
|        | SA32   | 0     | 1     | 0011001XXX               | 32                   | 0C8000h-0CFFFFh     |
|        | SA33   | 0     | 1     | 0011010XXX               | 32                   | 0D0000h-0D7FFFh     |
|        | SA34   | 0     | 1     | 0011011XXX               | 32                   | 0D8000h-0DFFFFh     |
|        | SA35   | 0     | 1     | 0011100XXX               | 32                   | 0E0000h-0E7FFFh     |
|        | SA36   | 0     | 1     | 0011101XXX               | 32                   | 0E8000h-0EFFFFh     |
|        | SA37   | 0     | 1     | 0011110XXX               | 32                   | 0F0000h-0F7FFFh     |
|        | SA38   | 0     | 1     | 0011111XXX               | 32                   | 0F8000h-0FFFFFh     |
| Bank   | Sector | CE#f1 | CE#f2 | Sector Address (A21-A12) | Sector Size (Kwords) | Address Range (x16) |

Table 6. Am29PDL129H Sector Architecture (Continued)

|        |        |       |       |                             |                         |                     |
|--------|--------|-------|-------|-----------------------------|-------------------------|---------------------|
| Bank B | SA39   | 0     | 1     | 0100000XXX                  | 32                      | 100000h–107FFFh     |
|        | SA40   | 0     | 1     | 0100001XXX                  | 32                      | 108000h–10FFFFh     |
|        | SA41   | 0     | 1     | 0100010XXX                  | 32                      | 110000h–117FFFh     |
|        | SA42   | 0     | 1     | 0100011XXX                  | 32                      | 118000h–11FFFFh     |
|        | SA43   | 0     | 1     | 0100100XXX                  | 32                      | 120000h–127FFFh     |
|        | SA44   | 0     | 1     | 0100101XXX                  | 32                      | 128000h–12FFFFh     |
|        | SA45   | 0     | 1     | 0100110XXX                  | 32                      | 130000h–137FFFh     |
|        | SA46   | 0     | 1     | 0100111XXX                  | 32                      | 138000h–13FFFFh     |
|        | SA47   | 0     | 1     | 0101000XXX                  | 32                      | 140000h–147FFFh     |
|        | SA48   | 0     | 1     | 0101001XXX                  | 32                      | 148000h–14FFFFh     |
|        | SA49   | 0     | 1     | 0101010XXX                  | 32                      | 150000h–157FFFh     |
|        | SA50   | 0     | 1     | 0101011XXX                  | 32                      | 158000h–15FFFFh     |
|        | SA51   | 0     | 1     | 0101100XXX                  | 32                      | 160000h–167FFFh     |
|        | SA52   | 0     | 1     | 0101101XXX                  | 32                      | 168000h–16FFFFh     |
|        | SA53   | 0     | 1     | 0101110XXX                  | 32                      | 170000h–177FFFh     |
|        | SA54   | 0     | 1     | 0101111XXX                  | 32                      | 178000h–17FFFFh     |
|        | SA55   | 0     | 1     | 0110000XXX                  | 32                      | 180000h–187FFFh     |
|        | SA56   | 0     | 1     | 0110001XXX                  | 32                      | 188000h–18FFFFh     |
|        | SA57   | 0     | 1     | 0110010XXX                  | 32                      | 190000h–197FFFh     |
|        | SA58   | 0     | 1     | 0110011XXX                  | 32                      | 198000h–19FFFFh     |
|        | SA59   | 0     | 1     | 0110100XXX                  | 32                      | 1A0000h–1A7FFFh     |
|        | SA60   | 0     | 1     | 0110101XXX                  | 32                      | 1A8000h–1AFFFFh     |
|        | SA61   | 0     | 1     | 0110110XXX                  | 32                      | 1B0000h–1B7FFFh     |
|        | SA62   | 0     | 1     | 0110111XXX                  | 32                      | 1B8000h–1BFFFFh     |
|        | SA63   | 0     | 1     | 0111000XXX                  | 32                      | 1C0000h–1C7FFFh     |
|        | SA64   | 0     | 1     | 0111001XXX                  | 32                      | 1C8000h–1CFFFFh     |
|        | SA65   | 0     | 1     | 0111010XXX                  | 32                      | 1D0000h–1D7FFFh     |
|        | SA66   | 0     | 1     | 0111011XXX                  | 32                      | 1D8000h–1DFFFFh     |
|        | SA67   | 0     | 1     | 0111100XXX                  | 32                      | 1E0000h–1E7FFFh     |
|        | SA68   | 0     | 1     | 0111101XXX                  | 32                      | 1E8000h–1EFFFFh     |
|        | SA69   | 0     | 1     | 0111110XXX                  | 32                      | 1F0000h–1F7FFFh     |
|        | SA70   | 0     | 1     | 0111111XXX                  | 32                      | 1F8000h–1FFFFFh     |
|        | SA71   | 0     | 1     | 1000000XXX                  | 32                      | 200000h–207FFFh     |
|        | SA72   | 0     | 1     | 1000001XXX                  | 32                      | 208000h–20FFFFh     |
|        | SA73   | 0     | 1     | 1000010XXX                  | 32                      | 210000h–217FFFh     |
|        | SA74   | 0     | 1     | 1000011XXX                  | 32                      | 218000h–21FFFFh     |
|        | SA75   | 0     | 1     | 1000100XXX                  | 32                      | 220000h–227FFFh     |
|        | SA76   | 0     | 1     | 1000101XXX                  | 32                      | 228000h–22FFFFh     |
|        | SA77   | 0     | 1     | 1000110XXX                  | 32                      | 230000h–237FFFh     |
|        | SA78   | 0     | 1     | 1000111XXX                  | 32                      | 238000h–23FFFFh     |
| Bank   | Sector | CE#f1 | CE#f2 | Sector Address<br>(A21-A12) | Sector Size<br>(Kwords) | Address Range (x16) |

Table 6. Am29PDL129H Sector Architecture (Continued)

|        |        |       |       |                          |                      |                     |
|--------|--------|-------|-------|--------------------------|----------------------|---------------------|
| Bank B | SA79   | 0     | 1     | 1001000XXX               | 32                   | 240000h–247FFFh     |
|        | SA80   | 0     | 1     | 1001001XXX               | 32                   | 248000h–24FFFFh     |
|        | SA81   | 0     | 1     | 1001010XXX               | 32                   | 250000h–257FFFh     |
|        | SA82   | 0     | 1     | 1001011XXX               | 32                   | 258000h–25FFFFh     |
|        | SA83   | 0     | 1     | 1001100XXX               | 32                   | 260000h–267FFFh     |
|        | SA84   | 0     | 1     | 1001101XXX               | 32                   | 268000h–26FFFFh     |
|        | SA85   | 0     | 1     | 1001110XXX               | 32                   | 270000h–277FFFh     |
|        | SA86   | 0     | 1     | 1001111XXX               | 32                   | 278000h–27FFFFh     |
|        | SA87   | 0     | 1     | 1010000XXX               | 32                   | 280000h–287FFFh     |
|        | SA88   | 0     | 1     | 1010001XXX               | 32                   | 288000h–28FFFFh     |
|        | SA89   | 0     | 1     | 1010010XXX               | 32                   | 290000h–297FFFh     |
|        | SA90   | 0     | 1     | 1010011XXX               | 32                   | 298000h–29FFFFh     |
|        | SA91   | 0     | 1     | 1010100XXX               | 32                   | 2A0000h–2A7FFFh     |
|        | SA92   | 0     | 1     | 1010101XXX               | 32                   | 2A8000h–2AFFFFh     |
|        | SA93   | 0     | 1     | 1010110XXX               | 32                   | 2B0000h–2B7FFFh     |
|        | SA94   | 0     | 1     | 1010111XXX               | 32                   | 2B8000h–2BFFFFh     |
|        | SA95   | 0     | 1     | 1011000XXX               | 32                   | 2C0000h–2C7FFFh     |
|        | SA96   | 0     | 1     | 1011001XXX               | 32                   | 2C8000h–2CFFFFh     |
|        | SA97   | 0     | 1     | 1011010XXX               | 32                   | 2D0000h–2D7FFFh     |
|        | SA98   | 0     | 1     | 1011011XXX               | 32                   | 2D8000h–2DFFFFh     |
|        | SA99   | 0     | 1     | 1011100XXX               | 32                   | 2E0000h–2E7FFFh     |
|        | SA100  | 0     | 1     | 1011101XXX               | 32                   | 2E8000h–2EFFFFh     |
|        | SA101  | 0     | 1     | 1011110XXX               | 32                   | 2F0000h–2F7FFFh     |
|        | SA102  | 0     | 1     | 1011111XXX               | 32                   | 2F8000h–2FFFFFh     |
|        | SA103  | 0     | 1     | 1100000XXX               | 32                   | 300000h–307FFFh     |
|        | SA104  | 0     | 1     | 1100001XXX               | 32                   | 308000h–30FFFFh     |
|        | SA105  | 0     | 1     | 1100010XXX               | 32                   | 310000h–317FFFh     |
|        | SA106  | 0     | 1     | 1100011XXX               | 32                   | 318000h–31FFFFh     |
|        | SA107  | 0     | 1     | 1100100XXX               | 32                   | 320000h–327FFFh     |
|        | SA108  | 0     | 1     | 1100101XXX               | 32                   | 328000h–32FFFFh     |
|        | SA109  | 0     | 1     | 1100110XXX               | 32                   | 330000h–337FFFh     |
|        | SA110  | 0     | 1     | 1100111XXX               | 32                   | 338000h–33FFFFh     |
|        | SA111  | 0     | 1     | 1101000XXX               | 32                   | 340000h–347FFFh     |
|        | SA112  | 0     | 1     | 1101001XXX               | 32                   | 348000h–34FFFFh     |
|        | SA113  | 0     | 1     | 1101010XXX               | 32                   | 350000h–357FFFh     |
|        | SA114  | 0     | 1     | 1101011XXX               | 32                   | 358000h–35FFFFh     |
|        | SA115  | 0     | 1     | 1101100XXX               | 32                   | 360000h–367FFFh     |
|        | SA116  | 0     | 1     | 1101101XXX               | 32                   | 368000h–36FFFFh     |
|        | SA117  | 0     | 1     | 1101110XXX               | 32                   | 370000h–377FFFh     |
|        | SA118  | 0     | 1     | 1101111XXX               | 32                   | 378000h–37FFFFh     |
| Bank   | Sector | CE#f1 | CE#f2 | Sector Address (A21-A12) | Sector Size (Kwords) | Address Range (x16) |

Table 6. Am29PDL129H Sector Architecture (Continued)

|        |       |   |   |            |    |                 |
|--------|-------|---|---|------------|----|-----------------|
| Bank B | SA119 | 0 | 1 | 1110000XXX | 32 | 380000h–387FFFh |
|        | SA120 | 0 | 1 | 1110001XXX | 32 | 388000h–38FFFFh |
|        | SA121 | 0 | 1 | 1110010XXX | 32 | 390000h–397FFFh |
|        | SA122 | 0 | 1 | 1110011XXX | 32 | 398000h–39FFFFh |
|        | SA123 | 0 | 1 | 1110100XXX | 32 | 3A0000h–3A7FFFh |
|        | SA124 | 0 | 1 | 1110101XXX | 32 | 3A8000h–3AFFFFh |
|        | SA125 | 0 | 1 | 1110110XXX | 32 | 3B0000h–3B7FFFh |
|        | SA126 | 0 | 1 | 1110111XXX | 32 | 3B8000h–3BFFFFh |
|        | SA127 | 0 | 1 | 1111000XXX | 32 | 3C0000h–3C7FFFh |
|        | SA128 | 0 | 1 | 1111001XXX | 32 | 3C8000h–3CFFFFh |
|        | SA129 | 0 | 1 | 1111010XXX | 32 | 3D0000h–3D7FFFh |
|        | SA130 | 0 | 1 | 1111011XXX | 32 | 3D8000h–3DFFFFh |
|        | SA131 | 0 | 1 | 1111100XXX | 32 | 3E0000h–3E7FFFh |
|        | SA132 | 0 | 1 | 1111101XXX | 32 | 3E8000h–3EFFFFh |
|        | SA133 | 0 | 1 | 1111110XXX | 32 | 3F0000h–3F7FFFh |
|        | SA134 | 0 | 1 | 1111111XXX | 32 | 3F8000h–3FFFFFh |

Table 6. Am29PDL129H Sector Architecture (Continued)

| Bank C | SA135  | 1     | 0     | 0000000XXX                  | 32                      | 000000h-007FFFh     |
|--------|--------|-------|-------|-----------------------------|-------------------------|---------------------|
|        | SA136  | 1     | 0     | 0000001XXX                  | 32                      | 008000h-00FFFFh     |
|        | SA137  | 1     | 0     | 0000010XXX                  | 32                      | 010000h-017FFFh     |
|        | SA138  | 1     | 0     | 0000011XXX                  | 32                      | 018000h-01FFFFh     |
|        | SA139  | 1     | 0     | 0000100XXX                  | 32                      | 020000h-027FFFh     |
|        | SA140  | 1     | 0     | 0000101XXX                  | 32                      | 028000h-02FFFFh     |
|        | SA141  | 1     | 0     | 0000110XXX                  | 32                      | 030000h-037FFFh     |
|        | SA142  | 1     | 0     | 0000111XXX                  | 32                      | 038000h-03FFFFh     |
|        | SA143  | 1     | 0     | 0001000XXX                  | 32                      | 040000h-047FFFh     |
|        | SA144  | 1     | 0     | 0001001XXX                  | 32                      | 048000h-04FFFFh     |
|        | SA145  | 1     | 0     | 0001010XXX                  | 32                      | 050000h-057FFFh     |
|        | SA146  | 1     | 0     | 0001011XXX                  | 32                      | 058000h-05FFFFh     |
|        | SA147  | 1     | 0     | 0001100XXX                  | 32                      | 060000h-067FFFh     |
|        | SA148  | 1     | 0     | 0001101XXX                  | 32                      | 068000h-06FFFFh     |
|        | SA149  | 1     | 0     | 0001110XXX                  | 32                      | 070000h-077FFFh     |
|        | SA150  | 1     | 0     | 0001111XXX                  | 32                      | 078000h-07FFFFh     |
|        | SA151  | 1     | 0     | 0010000XXX                  | 32                      | 080000h-087FFFh     |
|        | SA152  | 1     | 0     | 0010001XXX                  | 32                      | 088000h-08FFFFh     |
|        | SA153  | 1     | 0     | 0010010XXX                  | 32                      | 090000h-097FFFh     |
|        | SA154  | 1     | 0     | 0010011XXX                  | 32                      | 098000h-09FFFFh     |
|        | SA155  | 1     | 0     | 0010100XXX                  | 32                      | 0A0000h-0A7FFFh     |
|        | SA156  | 1     | 0     | 0010101XXX                  | 32                      | 0A8000h-0AFFFFh     |
|        | SA157  | 1     | 0     | 0010110XXX                  | 32                      | 0B0000h-0B7FFFh     |
|        | SA158  | 1     | 0     | 0010111XXX                  | 32                      | 0B8000h-0BFFFFh     |
| Bank   | Sector | CE#f1 | CE#f2 | Sector Address<br>(A21-A12) | Sector Size<br>(Kwords) | Address Range (x16) |

Table 6. Am29PDL129H Sector Architecture (Continued)

|                    |        |       |       |                          |                      |                     |
|--------------------|--------|-------|-------|--------------------------|----------------------|---------------------|
| Bank C (continued) | SA159  | 1     | 0     | 0011000XXX               | 32                   | 0C0000h–0C7FFFh     |
|                    | SA160  | 1     | 0     | 0011001XXX               | 32                   | 0C8000h–0CFFFFh     |
|                    | SA161  | 1     | 0     | 0011010XXX               | 32                   | 0D0000h–0D7FFFh     |
|                    | SA162  | 1     | 0     | 0011011XXX               | 32                   | 0D8000h–0DFFFFh     |
|                    | SA163  | 1     | 0     | 0011100XXX               | 32                   | 0E0000h–0E7FFFh     |
|                    | SA164  | 1     | 0     | 0011101XXX               | 32                   | 0E8000h–0EFFFFh     |
|                    | SA165  | 1     | 0     | 0011110XXX               | 32                   | 0F0000h–0F7FFFh     |
|                    | SA166  | 1     | 0     | 0011111XXX               | 32                   | 0F8000h–0FFFFFh     |
|                    | SA167  | 1     | 0     | 0100000XXX               | 32                   | 100000h–107FFFh     |
|                    | SA168  | 1     | 0     | 0100001XXX               | 32                   | 108000h–10FFFFh     |
|                    | SA169  | 1     | 0     | 0100010XXX               | 32                   | 110000h–117FFFh     |
|                    | SA170  | 1     | 0     | 0100011XXX               | 32                   | 118000h–11FFFFh     |
|                    | SA171  | 1     | 0     | 0100100XXX               | 32                   | 120000h–127FFFh     |
|                    | SA172  | 1     | 0     | 0100101XXX               | 32                   | 128000h–12FFFFh     |
|                    | SA173  | 1     | 0     | 0100110XXX               | 32                   | 130000h–137FFFh     |
|                    | SA174  | 1     | 0     | 0100111XXX               | 32                   | 138000h–13FFFFh     |
|                    | SA175  | 1     | 0     | 0101000XXX               | 32                   | 140000h–147FFFh     |
|                    | SA176  | 1     | 0     | 0101001XXX               | 32                   | 148000h–14FFFFh     |
|                    | SA177  | 1     | 0     | 0101010XXX               | 32                   | 150000h–157FFFh     |
|                    | SA178  | 1     | 0     | 0101011XXX               | 32                   | 158000h–15FFFFh     |
|                    | SA179  | 1     | 0     | 0101100XXX               | 32                   | 160000h–167FFFh     |
|                    | SA180  | 1     | 0     | 0101101XXX               | 32                   | 168000h–16FFFFh     |
|                    | SA181  | 1     | 0     | 0101110XXX               | 32                   | 170000h–177FFFh     |
|                    | SA182  | 1     | 0     | 0101111XXX               | 32                   | 178000h–17FFFFh     |
|                    | SA183  | 1     | 0     | 0110000XXX               | 32                   | 180000h–187FFFh     |
|                    | SA184  | 1     | 0     | 0110001XXX               | 32                   | 188000h–18FFFFh     |
|                    | SA185  | 1     | 0     | 0110010XXX               | 32                   | 190000h–197FFFh     |
|                    | SA186  | 1     | 0     | 0110011XXX               | 32                   | 198000h–19FFFFh     |
|                    | SA187  | 1     | 0     | 0110100XXX               | 32                   | 1A0000h–1A7FFFh     |
|                    | SA188  | 1     | 0     | 0110101XXX               | 32                   | 1A8000h–1AFFFFh     |
|                    | SA189  | 1     | 0     | 0110110XXX               | 32                   | 1B0000h–1B7FFFh     |
|                    | SA190  | 1     | 0     | 0110111XXX               | 32                   | 1B8000h–1BFFFFh     |
|                    | SA191  | 1     | 0     | 0111000XXX               | 32                   | 1C0000h–1C7FFFh     |
|                    | SA192  | 1     | 0     | 0111001XXX               | 32                   | 1C8000h–1CFFFFh     |
|                    | SA193  | 1     | 0     | 0111010XXX               | 32                   | 1D0000h–1D7FFFh     |
|                    | SA194  | 1     | 0     | 0111011XXX               | 32                   | 1D8000h–1DFFFFh     |
|                    | SA195  | 1     | 0     | 0111100XXX               | 32                   | 1E0000h–1E7FFFh     |
|                    | SA196  | 1     | 0     | 0111101XXX               | 32                   | 1E8000h–1EFFFFh     |
|                    | SA197  | 1     | 0     | 0111110XXX               | 32                   | 1F0000h–1F7FFFh     |
|                    | SA198  | 1     | 0     | 0111111XXX               | 32                   | 1F8000h–1FFFFFh     |
| Bank               | Sector | CE#f1 | CE#f2 | Sector Address (A21-A12) | Sector Size (Kwords) | Address Range (x16) |

Table 6. Am29PDL129H Sector Architecture (Continued)

| Bank C (continued) | SA199  | 1     | 0     | 1000000XXX                  | 32                      | 200000h–207FFFh     |
|--------------------|--------|-------|-------|-----------------------------|-------------------------|---------------------|
|                    | SA200  | 1     | 0     | 1000001XXX                  | 32                      | 208000h–20FFFFh     |
|                    | SA201  | 1     | 0     | 1000010XXX                  | 32                      | 210000h–217FFFh     |
|                    | SA202  | 1     | 0     | 1000011XXX                  | 32                      | 218000h–21FFFFh     |
|                    | SA203  | 1     | 0     | 1000100XXX                  | 32                      | 220000h–227FFFh     |
|                    | SA204  | 1     | 0     | 1000101XXX                  | 32                      | 228000h–22FFFFh     |
|                    | SA205  | 1     | 0     | 1000110XXX                  | 32                      | 230000h–237FFFh     |
|                    | SA206  | 1     | 0     | 1000111XXX                  | 32                      | 238000h–23FFFFh     |
|                    | SA207  | 1     | 0     | 1001000XXX                  | 32                      | 240000h–247FFFh     |
|                    | SA208  | 1     | 0     | 1001001XXX                  | 32                      | 248000h–24FFFFh     |
|                    | SA209  | 1     | 0     | 1001010XXX                  | 32                      | 250000h–257FFFh     |
|                    | SA210  | 1     | 0     | 1001011XXX                  | 32                      | 258000h–25FFFFh     |
|                    | SA211  | 1     | 0     | 1001100XXX                  | 32                      | 260000h–267FFFh     |
|                    | SA212  | 1     | 0     | 1001101XXX                  | 32                      | 268000h–26FFFFh     |
|                    | SA213  | 1     | 0     | 1001110XXX                  | 32                      | 270000h–277FFFh     |
|                    | SA214  | 1     | 0     | 1001111XXX                  | 32                      | 278000h–27FFFFh     |
|                    | SA215  | 1     | 0     | 1010000XXX                  | 32                      | 280000h–287FFFh     |
|                    | SA216  | 1     | 0     | 1010001XXX                  | 32                      | 288000h–28FFFFh     |
|                    | SA217  | 1     | 0     | 1010010XXX                  | 32                      | 290000h–297FFFh     |
|                    | SA218  | 1     | 0     | 1010011XXX                  | 32                      | 298000h–29FFFFh     |
|                    | SA219  | 1     | 0     | 1010100XXX                  | 32                      | 2A0000h–2A7FFFh     |
|                    | SA220  | 1     | 0     | 1010101XXX                  | 32                      | 2A8000h–2AFFFFh     |
|                    | SA221  | 1     | 0     | 1010110XXX                  | 32                      | 2B0000h–2B7FFFh     |
|                    | SA222  | 1     | 0     | 1010111XXX                  | 32                      | 2B8000h–2BFFFFh     |
|                    | SA223  | 1     | 0     | 1011000XXX                  | 32                      | 2C0000h–2C7FFFh     |
|                    | SA224  | 1     | 0     | 1011001XXX                  | 32                      | 2C8000h–2CFFFFh     |
|                    | SA225  | 1     | 0     | 1011010XXX                  | 32                      | 2D0000h–2D7FFFh     |
|                    | SA226  | 1     | 0     | 1011011XXX                  | 32                      | 2D8000h–2DFFFFh     |
|                    | SA227  | 1     | 0     | 1011100XXX                  | 32                      | 2E0000h–2E7FFFh     |
|                    | SA228  | 1     | 0     | 1011101XXX                  | 32                      | 2E8000h–2EFFFFh     |
|                    | SA229  | 1     | 0     | 1011110XXX                  | 32                      | 2F0000h–2F7FFFh     |
|                    | SA230  | 1     | 0     | 1011111XXX                  | 32                      | 2F8000h–2FFFFFh     |
| Bank               | Sector | CE#f1 | CE#f2 | Sector Address<br>(A21-A12) | Sector Size<br>(Kwords) | Address Range (x16) |

Table 6. Am29PDL129H Sector Architecture (Continued)

|        |       |   |   |            |    |                 |
|--------|-------|---|---|------------|----|-----------------|
| Bank D | SA231 | 1 | 0 | 1100000XXX | 32 | 300000h–307FFFh |
|        | SA232 | 1 | 0 | 1100001XXX | 32 | 308000h–30FFFFh |
|        | SA233 | 1 | 0 | 1100010XXX | 32 | 310000h–317FFFh |
|        | SA234 | 1 | 0 | 1100011XXX | 32 | 318000h–31FFFFh |
|        | SA235 | 1 | 0 | 1100100XXX | 32 | 320000h–327FFFh |
|        | SA236 | 1 | 0 | 1100101XXX | 32 | 328000h–32FFFFh |
|        | SA237 | 1 | 0 | 1100110XXX | 32 | 330000h–337FFFh |
|        | SA238 | 1 | 0 | 1100111XXX | 32 | 338000h–33FFFFh |
|        | SA239 | 1 | 0 | 1101000XXX | 32 | 340000h–347FFFh |
|        | SA240 | 1 | 0 | 1101001XXX | 32 | 348000h–34FFFFh |
|        | SA241 | 1 | 0 | 1101010XXX | 32 | 350000h–357FFFh |
|        | SA242 | 1 | 0 | 1101011XXX | 32 | 358000h–35FFFFh |
|        | SA243 | 1 | 0 | 1101100XXX | 32 | 360000h–367FFFh |
|        | SA244 | 1 | 0 | 1101101XXX | 32 | 368000h–36FFFFh |
|        | SA245 | 1 | 0 | 1101110XXX | 32 | 370000h–377FFFh |
|        | SA246 | 1 | 0 | 1101111XXX | 32 | 378000h–37FFFFh |
|        | SA247 | 1 | 0 | 1110000XXX | 32 | 380000h–387FFFh |
|        | SA248 | 1 | 0 | 1110001XXX | 32 | 388000h–38FFFFh |
|        | SA249 | 1 | 0 | 1110010XXX | 32 | 390000h–397FFFh |
|        | SA250 | 1 | 0 | 1110011XXX | 32 | 398000h–39FFFFh |
|        | SA251 | 1 | 0 | 1110100XXX | 32 | 3A0000h–3A7FFFh |
|        | SA252 | 1 | 0 | 1110101XXX | 32 | 3A8000h–3AFFFFh |
|        | SA253 | 1 | 0 | 1110110XXX | 32 | 3B0000h–3B7FFFh |
|        | SA254 | 1 | 0 | 1110111XXX | 32 | 3B8000h–3BFFFFh |
|        | SA255 | 1 | 0 | 1111000XXX | 32 | 3C0000h–3C7FFFh |
|        | SA256 | 1 | 0 | 1111001XXX | 32 | 3C8000h–3CFFFFh |
|        | SA257 | 1 | 0 | 1111010XXX | 32 | 3D0000h–3D7FFFh |
|        | SA258 | 1 | 0 | 1111011XXX | 32 | 3D8000h–3DFFFFh |
|        | SA259 | 1 | 0 | 1111100XXX | 32 | 3E0000h–3E7FFFh |
|        | SA260 | 1 | 0 | 1111101XXX | 32 | 3E8000h–3EFFFFh |
|        | SA261 | 1 | 0 | 1111110XXX | 32 | 3F0000h–3F7FFFh |
|        | SA262 | 1 | 0 | 1111111000 | 32 | 3F8000h–3F8FFFh |
|        | SA263 | 1 | 0 | 1111111001 | 4  | 3F9000h–3F9FFFh |
|        | SA264 | 1 | 0 | 1111111010 | 4  | 3FA000h–3FAFFFh |
|        | SA265 | 1 | 0 | 1111111011 | 4  | 3FB000h–3FBFFFh |
|        | SA266 | 1 | 0 | 1111111100 | 4  | 3FC000h–3FCFFFh |
|        | SA267 | 1 | 0 | 1111111101 | 4  | 3FD000h–3FDFFFh |
|        | SA268 | 1 | 0 | 1111111110 | 4  | 3FE000h–3FEFFFh |
|        | SA269 | 1 | 0 | 1111111111 | 4  | 3FF000h–3FFFFFh |

Table 7. SecSi™ Sector Addresses

| SecSi Sector Area   | Sector Size | Address Range   |
|---------------------|-------------|-----------------|
| Factory-Locked Area | 64 words    | 000000h–00003Fh |

| SecSi Sector Area      | Sector Size | Address Range   |
|------------------------|-------------|-----------------|
| Customer-Lockable Area | 64 words    | 000040h–00007Fh |

**Table 8. Am29PDL127H Boot Sector/Sector Block Addresses for Protection/Unprotection**

| Sector      | A22-A12                                   | Sector/<br>Sector Block Size |
|-------------|-------------------------------------------|------------------------------|
| SA0         | 00000000000                               | 4 Kwords                     |
| SA1         | 00000000001                               | 4 Kwords                     |
| SA2         | 00000000010                               | 4 Kwords                     |
| SA3         | 00000000011                               | 4 Kwords                     |
| SA4         | 00000000100                               | 4 Kwords                     |
| SA5         | 00000000101                               | 4 Kwords                     |
| SA6         | 00000000110                               | 4 Kwords                     |
| SA7         | 00000000111                               | 4 Kwords                     |
| SA8–SA10    | 00000001XXX<br>00000010XXX<br>00000011XXX | 96 (3x32) Kwords             |
| SA11–SA14   | 000001XXXXX                               | 128 (4x32) Kwords            |
| SA15–SA18   | 000010XXXXX                               | 128 (4x32) Kwords            |
| SA19–SA22   | 000011XXXXX                               | 128 (4x32) Kwords            |
| SA23–SA26   | 000100XXXXX                               | 128 (4x32) Kwords            |
| SA27–SA30   | 000101XXXXX                               | 128 (4x32) Kwords            |
| SA31–SA34   | 000110XXXXX                               | 128 (4x32) Kwords            |
| SA35–SA38   | 000111XXXXX                               | 128 (4x32) Kwords            |
| SA39–SA42   | 001000XXXXX                               | 128 (4x32) Kwords            |
| SA43–SA46   | 001001XXXXX                               | 128 (4x32) Kwords            |
| SA47–SA50   | 001010XXXXX                               | 128 (4x32) Kwords            |
| SA51–SA54   | 001011XXXXX                               | 128 (4x32) Kwords            |
| SA55–SA58   | 001100XXXXX                               | 128 (4x32) Kwords            |
| SA59–SA62   | 001101XXXXX                               | 128 (4x32) Kwords            |
| SA63–SA66   | 001110XXXXX                               | 128 (4x32) Kwords            |
| SA67–SA70   | 001111XXXXX                               | 128 (4x32) Kwords            |
| SA71–SA74   | 010000XXXXX                               | 128 (4x32) Kwords            |
| SA75–SA78   | 010001XXXXX                               | 128 (4x32) Kwords            |
| SA79–SA82   | 010010XXXXX                               | 128 (4x32) Kwords            |
| SA83–SA86   | 010011XXXXX                               | 128 (4x32) Kwords            |
| SA87–SA90   | 010100XXXXX                               | 128 (4x32) Kwords            |
| SA91–SA94   | 010101XXXXX                               | 128 (4x32) Kwords            |
| SA95–SA98   | 010110XXXXX                               | 128 (4x32) Kwords            |
| SA99–SA102  | 010111XXXXX                               | 128 (4x32) Kwords            |
| SA103–SA106 | 011000XXXXX                               | 128 (4x32) Kwords            |
| SA107–SA110 | 011001XXXXX                               | 128 (4x32) Kwords            |
| SA111–SA114 | 011010XXXXX                               | 128 (4x32) Kwords            |
| SA115–SA118 | 011011XXXXX                               | 128 (4x32) Kwords            |
| SA119–SA122 | 011100XXXXX                               | 128 (4x32) Kwords            |
| SA123–SA126 | 011101XXXXX                               | 128 (4x32) Kwords            |
| SA127–SA130 | 011110XXXXX                               | 128 (4x32) Kwords            |

| Sector      | A22-A12     | Sector/<br>Sector Block Size |
|-------------|-------------|------------------------------|
| SA131–SA134 | 011111XXXXX | 128 (4x32) Kwords            |

|             |                                           |                   |
|-------------|-------------------------------------------|-------------------|
| SA135–SA138 | 100000XXXXX                               | 128 (4x32) Kwords |
| SA139–SA142 | 100001XXXXX                               | 128 (4x32) Kwords |
| SA143–SA146 | 100010XXXXX                               | 128 (4x32) Kwords |
| SA147–SA150 | 100011XXXXX                               | 128 (4x32) Kwords |
| SA151–SA154 | 100100XXXXX                               | 128 (4x32) Kwords |
| SA155–SA158 | 100101XXXXX                               | 128 (4x32) Kwords |
| SA159–SA162 | 100110XXXXX                               | 128 (4x32) Kwords |
| SA163–SA166 | 100111XXXXX                               | 128 (4x32) Kwords |
| SA167–SA170 | 101000XXXXX                               | 128 (4x32) Kwords |
| SA171–SA174 | 101001XXXXX                               | 128 (4x32) Kwords |
| SA175–SA178 | 101010XXXXX                               | 128 (4x32) Kwords |
| SA179–SA182 | 101011XXXXX                               | 128 (4x32) Kwords |
| SA183–SA186 | 101100XXXXX                               | 128 (4x32) Kwords |
| SA187–SA190 | 101101XXXXX                               | 128 (4x32) Kwords |
| SA191–SA194 | 101110XXXXX                               | 128 (4x32) Kwords |
| SA195–SA198 | 101111XXXXX                               | 128 (4x32) Kwords |
| SA199–SA202 | 110000XXXXX                               | 128 (4x32) Kwords |
| SA203–SA206 | 110001XXXXX                               | 128 (4x32) Kwords |
| SA207–SA210 | 110010XXXXX                               | 128 (4x32) Kwords |
| SA211–SA214 | 110011XXXXX                               | 128 (4x32) Kwords |
| SA215–SA218 | 110100XXXXX                               | 128 (4x32) Kwords |
| SA219–SA222 | 110101XXXXX                               | 128 (4x32) Kwords |
| SA223–SA226 | 110110XXXXX                               | 128 (4x32) Kwords |
| SA227–SA230 | 110111XXXXX                               | 128 (4x32) Kwords |
| SA231–SA234 | 111000XXXXX                               | 128 (4x32) Kwords |
| SA235–SA238 | 111001XXXXX                               | 128 (4x32) Kwords |
| SA239–SA242 | 111010XXXXX                               | 128 (4x32) Kwords |
| SA243–SA246 | 111011XXXXX                               | 128 (4x32) Kwords |
| SA247–SA250 | 111100XXXXX                               | 128 (4x32) Kwords |
| SA251–SA254 | 111101XXXXX                               | 128 (4x32) Kwords |
| SA255–SA258 | 111110XXXXX                               | 128 (4x32) Kwords |
| SA259–SA261 | 11111100XXX<br>11111101XXX<br>11111110XXX | 96 (3x32) Kwords  |
| SA262       | 11111111000                               | 4 Kwords          |
| SA263       | 11111111001                               | 4 Kwords          |
| SA264       | 11111111010                               | 4 Kwords          |
| SA265       | 11111111011                               | 4 Kwords          |
| SA266       | 11111111100                               | 4 Kwords          |
| SA267       | 11111111101                               | 4 Kwords          |
| SA268       | 11111111110                               | 4 Kwords          |
| SA269       | 11111111111                               | 4 Kwords          |

**Table 9. Am29PDL129H Boot Sector/Sector Block Addresses for Protection/Unprotection**

| Sector      | CE#f1 | CE#f2 | A21–A12                                | Sector/<br>Sector Block Size |
|-------------|-------|-------|----------------------------------------|------------------------------|
| SA0         | 0     | 1     | 0000000000                             | 4 Kwords                     |
| SA1         | 0     | 1     | 0000000001                             | 4 Kwords                     |
| SA2         | 0     | 1     | 0000000010                             | 4 Kwords                     |
| SA3         | 0     | 1     | 0000000011                             | 4 Kwords                     |
| SA4         | 0     | 1     | 0000000100                             | 4 Kwords                     |
| SA5         | 0     | 1     | 0000000101                             | 4 Kwords                     |
| SA6         | 0     | 1     | 0000000110                             | 4 Kwords                     |
| SA7         | 0     | 1     | 0000000111                             | 4 Kwords                     |
| SA8–SA10    | 0     | 1     | 0000001XXX<br>0000010XXX<br>0000011XXX | 96 (3x32) Kwords             |
| SA11–SA14   | 0     | 1     | 00001XXXXX                             | 128 (4x32) Kwords            |
| SA15–SA18   | 0     | 1     | 00010XXXXX                             | 128 (4x32) Kwords            |
| SA19–SA22   | 0     | 1     | 00011XXXXX                             | 128 (4x32) Kwords            |
| SA23–SA26   | 0     | 1     | 00100XXXXX                             | 128 (4x32) Kwords            |
| SA27–SA30   | 0     | 1     | 00101XXXXX                             | 128 (4x32) Kwords            |
| SA31–SA34   | 0     | 1     | 00110XXXXX                             | 128 (4x32) Kwords            |
| SA35–SA38   | 0     | 1     | 00111XXXXX                             | 128 (4x32) Kwords            |
| SA39–SA42   | 0     | 1     | 01000XXXXX                             | 128 (4x32) Kwords            |
| SA43–SA46   | 0     | 1     | 01001XXXXX                             | 128 (4x32) Kwords            |
| SA47–SA50   | 0     | 1     | 01010XXXXX                             | 128 (4x32) Kwords            |
| SA51–SA54   | 0     | 1     | 01011XXXXX                             | 128 (4x32) Kwords            |
| SA55–SA58   | 0     | 1     | 01100XXXXX                             | 128 (4x32) Kwords            |
| SA59–SA62   | 0     | 1     | 01101XXXXX                             | 128 (4x32) Kwords            |
| SA63–SA66   | 0     | 1     | 01110XXXXX                             | 128 (4x32) Kwords            |
| SA67–SA70   | 0     | 1     | 01111XXXXX                             | 128 (4x32) Kwords            |
| SA71–SA74   | 0     | 1     | 10000XXXXX                             | 128 (4x32) Kwords            |
| SA75–SA78   | 0     | 1     | 10001XXXXX                             | 128 (4x32) Kwords            |
| SA79–SA82   | 0     | 1     | 10010XXXXX                             | 128 (4x32) Kwords            |
| SA83–SA86   | 0     | 1     | 10011XXXXX                             | 128 (4x32) Kwords            |
| SA87–SA90   | 0     | 1     | 10100XXXXX                             | 128 (4x32) Kwords            |
| SA91–SA94   | 0     | 1     | 10101XXXXX                             | 128 (4x32) Kwords            |
| SA95–SA98   | 0     | 1     | 10110XXXXX                             | 128 (4x32) Kwords            |
| SA99–SA102  | 0     | 1     | 10111XXXXX                             | 128 (4x32) Kwords            |
| SA103–SA106 | 0     | 1     | 11000XXXXX                             | 128 (4x32) Kwords            |
| SA107–SA110 | 0     | 1     | 11001XXXXX                             | 128 (4x32) Kwords            |
| SA111–SA114 | 0     | 1     | 11010XXXXX                             | 128 (4x32) Kwords            |
| SA115–SA118 | 0     | 1     | 11011XXXXX                             | 128 (4x32) Kwords            |
| SA119–SA122 | 0     | 1     | 11100XXXXX                             | 128 (4x32) Kwords            |
| SA123–SA126 | 0     | 1     | 11101XXXXX                             | 128 (4x32) Kwords            |

| Sector      | CE#f1 | CE#f2 | A21–A12                                | Sector/<br>Sector Block Size |
|-------------|-------|-------|----------------------------------------|------------------------------|
| SA127–SA130 | 0     | 1     | 11110XXXXX                             | 128 (4x32) Kwords            |
| SA131–SA134 | 0     | 1     | 11111XXXXX                             | 128 (4x32) Kwords            |
| SA135–SA138 | 1     | 0     | 00000XXXXX                             | 128 (4x32) Kwords            |
| SA139–SA142 | 1     | 0     | 00001XXXXX                             | 128 (4x32) Kwords            |
| SA143–SA146 | 1     | 0     | 00010XXXXX                             | 128 (4x32) Kwords            |
| SA147–SA150 | 1     | 0     | 00011XXXXX                             | 128 (4x32) Kwords            |
| SA151–SA154 | 1     | 0     | 00100XXXXX                             | 128 (4x32) Kwords            |
| SA155–SA158 | 1     | 0     | 00101XXXXX                             | 128 (4x32) Kwords            |
| SA159–SA162 | 1     | 0     | 00110XXXXX                             | 128 (4x32) Kwords            |
| SA163–SA166 | 1     | 0     | 00111XXXXX                             | 128 (4x32) Kwords            |
| SA167–SA170 | 1     | 0     | 01000XXXXX                             | 128 (4x32) Kwords            |
| SA171–SA174 | 1     | 0     | 01001XXXXX                             | 128 (4x32) Kwords            |
| SA175–SA178 | 1     | 0     | 01010XXXXX                             | 128 (4x32) Kwords            |
| SA179–SA182 | 1     | 0     | 01011XXXXX                             | 128 (4x32) Kwords            |
| SA183–SA186 | 1     | 0     | 01100XXXXX                             | 128 (4x32) Kwords            |
| SA187–SA190 | 1     | 0     | 01101XXXXX                             | 128 (4x32) Kwords            |
| SA191–SA194 | 1     | 0     | 01110XXXXX                             | 128 (4x32) Kwords            |
| SA195–SA198 | 1     | 0     | 01111XXXXX                             | 128 (4x32) Kwords            |
| SA199–SA202 | 1     | 0     | 10000XXXXX                             | 128 (4x32) Kwords            |
| SA203–SA206 | 1     | 0     | 10001XXXXX                             | 128 (4x32) Kwords            |
| SA207–SA210 | 1     | 0     | 10010XXXXX                             | 128 (4x32) Kwords            |
| SA211–SA214 | 1     | 0     | 10011XXXXX                             | 128 (4x32) Kwords            |
| SA215–SA218 | 1     | 0     | 10100XXXXX                             | 128 (4x32) Kwords            |
| SA219–SA222 | 1     | 0     | 10101XXXXX                             | 128 (4x32) Kwords            |
| SA223–SA226 | 1     | 0     | 10110XXXXX                             | 128 (4x32) Kwords            |
| SA227–SA230 | 1     | 0     | 10111XXXXX                             | 128 (4x32) Kwords            |
| SA231–SA234 | 1     | 0     | 11000XXXXX                             | 128 (4x32) Kwords            |
| SA235–SA238 | 1     | 0     | 11001XXXXX                             | 128 (4x32) Kwords            |
| SA239–SA242 | 1     | 0     | 11010XXXXX                             | 128 (4x32) Kwords            |
| SA243–SA246 | 1     | 0     | 11011XXXXX                             | 128 (4x32) Kwords            |
| SA247–SA250 | 1     | 0     | 11100XXXXX                             | 128 (4x32) Kwords            |
| SA251–SA254 | 1     | 0     | 11101XXXXX                             | 128 (4x32) Kwords            |
| SA255–SA258 | 1     | 0     | 11110XXXXX                             | 128 (4x32) Kwords            |
| SA259–SA261 | 1     | 0     | 1111100XXX<br>1111101XXX<br>1111110XXX | 96 (3x32) Kwords             |
| SA262       | 1     | 0     | 1111111000                             | 4 Kwords                     |
| SA263       | 1     | 0     | 1111111001                             | 4 Kwords                     |
| SA264       | 1     | 0     | 1111111010                             | 4 Kwords                     |
| SA265       | 1     | 0     | 1111111011                             | 4 Kwords                     |
| SA266       | 1     | 0     | 1111111100                             | 4 Kwords                     |
| SA267       | 1     | 0     | 1111111101                             | 4 Kwords                     |
| SA268       | 1     | 0     | 1111111110                             | 4 Kwords                     |
| SA269       | 1     | 0     | 1111111111                             | 4 Kwords                     |

## SECTOR PROTECTION

The Am29PDL127H/Am29PDL129H features several levels of sector protection, which can disable both the program and erase operations in certain sectors or sector groups:

### **Persistent Sector Protection**

A command sector protection method that replaces the old 12 V controlled protection method.

### **Password Sector Protection**

A highly sophisticated protection method that requires a password before changes to certain sectors or sector groups are permitted.

### **WP# Hardware Protection**

A write protect pin that can prevent program or erase operations in sectors 0, 1, 268, and 269. The WP# Hardware Protection feature is always available, regardless of which of the other two methods are chosen.

### **Selecting a Sector Protection Mode**

The device defaults to the Persistent Sector Protection mode. However, to prevent a program or virus from later setting the Password Mode Locking Bit, which would cause an unexpected shift from the default Persistent Sector Protection Mode into the Password Protection Mode, it is recommended that either of two one-time programmable non-volatile bits that permanently define which sector protection method be set **before the device is first programmed**. The **Persistent Sector Protection Mode Locking Bit** permanently sets the device to the Persistent Sector Protection mode. The **Password Mode Locking Bit** permanently sets the device to the Password Sector Protection mode. It is not possible to switch between the two protection modes once a locking bit has been set.

The device is shipped with all sectors unprotected. AMD offers the option of programming and protecting sectors at the factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector is protected or unprotected. See [Autoselect Command Sequence](#) for details.

## Persistent Sector Protection

The Persistent Sector Protection method replaces the 12 V controlled protection method in previous AMD flash devices. This new method provides three different sector protection states:

- **Persistently Locked**—The sector is protected and cannot be changed.

- **Dynamically Locked**—The sector is protected and can be changed by a simple command.

- **Unlocked**—The sector is unprotected and can be changed by a simple command.

To achieve these states, three types of “bits” are used:

### **Persistent Protection Bit (PPB)**

A single Persistent (non-volatile) Protection Bit is assigned to a maximum four sectors (see the sector address tables for specific sector protection groupings). All 4 Kword boot-block sectors have individual sector Persistent Protection Bits (PPBs) for greater flexibility. Each PPB is individually modifiable through the **PPB Write Command**.

The device erases all PPBs in parallel. If any PPB requires erasure, the device must be instructed to pre-program all of the sector PPBs prior to PPB erasure. Otherwise, a previously erased sector PPBs can potentially be over-erased. **The flash device does not have a built-in means of preventing sector PPBs over-erasure.**

### **Persistent Protection Bit Lock (PPB Lock)**

The Persistent Protection Bit Lock (PPB Lock) is a global volatile bit. When set to “1”, the PPBs cannot be changed. When cleared (“0”), the PPBs are changeable. There is only one PPB Lock bit per device. The PPB Lock is cleared after power-up or hardware reset. There is no command sequence to unlock the PPB Lock.

### **Dynamic Protection Bit (DYB)**

A volatile protection bit is assigned for each sector. After power-up or hardware reset, the contents of all DYBs is “0”. Each DYB is individually modifiable through the DYB Write Command.

When the parts are first shipped, the PPBs are cleared, the DYBs are cleared, and PPB Lock is defaulted to power up in the cleared state – meaning the PPBs are changeable.

When the device is first powered on the DYBs power up cleared (sectors not protected). The Protection State for each sector is determined by the logical OR of the PPB and the DYB related to that sector. For the sectors that have the PPBs cleared, the DYBs control whether or not the sector is protected or unprotected. By issuing the DYB Write command sequences, the DYBs will be set or cleared, thus placing each sector in the protected or unprotected state. These are the so-called **Dynamic Locked or Unlocked** states. They are called dynamic states because it is very easy to switch back and forth between the protected and unprotected conditions. This allows software to easily protect sectors against inadvertent changes yet does

not prevent the easy removal of protection when changes are needed. The DYBs maybe set or cleared as often as needed.

The PPBs allow for a more static, and difficult to change, level of protection. The PPBs retain their state across power cycles because they are non-volatile. Individual PPBs are set with a command but must all be cleared as a group through a complex sequence of program and erasing commands. The PPBs are also limited to 100 erase cycles.

The PPB Lock bit adds an additional level of protection. Once all PPBs are programmed to the desired settings, the PPB Lock may be set to “1”. Setting the PPB Lock disables all program and erase commands to the non-volatile PPBs. In effect, the PPB Lock Bit locks the PPBs into their current state. The only way to clear the PPB Lock is to go through a power cycle. System boot code can determine if any changes to the PPB are needed; for example, to allow new system code to be downloaded. If no changes are needed then the boot code can set the PPB Lock to disable any further changes to the PPBs during system operation.

The WP#/ACC write protect pin adds a final level of hardware protection to sectors 0, 1, 268, and 269. When this pin is low it is not possible to change the contents of these sectors. These sectors generally hold system boot code. The WP#/ACC pin can prevent any changes to the boot code that could override the choices made while setting up sector protection during system initialization.

It is possible to have sectors that have been persistently locked, and sectors that are left in the dynamic state. The sectors in the dynamic state are all unprotected. If there is a need to protect some of them, a simple DYB Write command sequence is all that is necessary. The DYB write command for the dynamic sectors switch the DYBs to signify protected and unprotected, respectively. If there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB Lock bit must be disabled by either putting the device through a power-cycle, or hardware reset. The PPBs can then be changed to reflect the desired settings. Setting the PPB lock bit once again will lock the PPBs, and the device operates normally again.

The best protection is achieved by executing the PPB lock bit set command early in the boot code, and protect the boot code by holding  $WP\#/ACC = V_{IL}$ .

**Table 10. Sector Protection Schemes**

| DYB | PPB | PPB Lock | Sector State                                      |
|-----|-----|----------|---------------------------------------------------|
| 0   | 0   | 0        | Unprotected—PPB and DYB are changeable            |
| 0   | 0   | 1        | Unprotected—PPB not changeable, DYB is changeable |
| 0   | 1   | 0        | Protected—PPB and DYB are changeable              |
| 1   | 0   | 0        |                                                   |
| 1   | 1   | 0        | Protected—PPB not changeable, DYB is changeable   |
| 0   | 1   | 1        |                                                   |
| 1   | 0   | 1        |                                                   |
| 1   | 1   | 1        |                                                   |

Table 10 contains all possible combinations of the DYB, PPB, and PPB lock relating to the status of the sector.

In summary, if the PPB is set, and the PPB lock is set, the sector is protected and the protection can not be removed until the next power cycle clears the PPB lock. If the PPB is cleared, the sector can be dynamically locked or unlocked. The DYB then controls whether or not the sector is protected or unprotected.

If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode. A program command to a protected sector enables status polling for approximately 1  $\mu$ s before the device returns to read mode without having modified the contents of the protected sector. An erase command to a protected sector enables status polling for approximately 50  $\mu$ s after which the device returns to read mode without having erased the protected sector.

The programming of the DYB, PPB, and PPB lock for a given sector can be verified by writing a DYB/PPB/PPB lock verify command to the device.

#### Persistent Sector Protection Mode Locking Bit

Like the password mode locking bit, a Persistent Sector Protection mode locking bit exists to guarantee that the device remain in software sector protection. Once set, the Persistent Sector Protection locking bit prevents programming of the password protection mode locking bit. This guarantees that a hacker could not place the device in password protection mode.

#### Password Protection Mode

The Password Sector Protection Mode method allows an even higher level of security than the Persistent Sector Protection Mode. There are two main differ-

ences between the Persistent Sector Protection and the Password Sector Protection Mode:

- When the device is first powered on, or comes out of a reset cycle, the PPB Lock bit set to the **locked state**, rather than cleared to the unlocked state.
- The only means to clear the PPB Lock bit is by writing a unique **64-bit Password** to the device.

The Password Sector Protection method is otherwise identical to the Persistent Sector Protection method.

A 64-bit password is the only additional tool utilized in this method.

Once the Password Mode Locking Bit is set, the password is permanently set with no means to read, program, or erase it. The password is used to clear the PPB Lock bit. The Password Unlock command must be written to the flash, along with a password. The flash device internally compares the given password with the pre-programmed password. If they match, the PPB Lock bit is cleared, and the PPBs can be altered. If they do not match, the flash device does nothing. There is a built-in 2  $\mu$ s delay for each “password check.” This delay is intended to thwart any efforts to run a program that tries all possible combinations in order to crack the password.

### Password and Password Mode Locking Bit

In order to select the Password sector protection scheme, the customer must first program the password. The password may be correlated to the unique Electronic Serial Number (ESN) of the particular flash device. Each ESN is different for every flash device; therefore each password should be different for every flash device. While programming in the password region, the customer may perform Password Verify operations.

Once the desired password is programmed in, the customer must then set the Password Mode Locking Bit. This operation achieves two objectives:

1. Permanently sets the device to operate using the Password Protection Mode. It is not possible to reverse this function.
2. Disables *all further commands* to the password region. All program, and read operations are ignored.

Both of these objectives are important, and if not carefully considered, may lead to unrecoverable errors. The user must be sure that the Password Protection method is desired when setting the Password Mode Locking Bit. More importantly, the user must be sure that the password is correct when the Password Mode Locking Bit is set. Due to the fact that read operations are disabled, there is no means to verify what the password is afterwards. If the password is lost after setting the Password Mode Locking Bit, there will be no way to clear the PPB Lock bit.

The Password Mode Locking Bit, once set, prevents reading the 64-bit password on the DQ bus and further password programming. The Password Mode Locking Bit is not erasable. Once Password Mode Locking Bit is programmed, the Persistent Sector Protection Locking Bit is disabled from programming, guaranteeing that no changes to the protection scheme are allowed.

### 64-bit Password

The 64-bit Password is located in its own memory space and is accessible through the use of the Password Program and Verify commands (see “Password Verify Command”). The password function works in conjunction with the Password Mode Locking Bit, which when set, prevents the Password Verify command from reading the contents of the password on the pins of the device.

### Write Protect (WP#)

The Write Protect feature provides a hardware method of protecting sectors 0, 1, 268, and 269 without using  $V_{ID}$ . This function is provided by the WP# pin and overrides the previously discussed High Voltage Sector Protection method.

If the system asserts  $V_{IL}$  on the WP#/ACC pin, the device disables program and erase functions in the two outermost 4 Kword sectors on both ends of the flash array independent of whether it was previously protected or unprotected.

If the system asserts  $V_{IH}$  on the WP#/ACC pin, the device reverts to whether sectors 0, 1, 268, and 269 were last set to be protected or unprotected. That is, sector protection or unprotection for these sectors depends on whether they were last protected or unprotected using the method described in High Voltage Sector Protection.

Note that the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

### Persistent Protection Bit Lock

The Persistent Protection Bit (PPB) Lock is a volatile bit that reflects the state of the Password Mode Locking Bit after power-up reset. If the Password Mode Lock Bit is also set after a hardware reset (RESET# asserted) or a power-up reset, the **ONLY** means for clearing the PPB Lock Bit in Password Protection Mode is to issue the Password Unlock command. Successful execution of the Password Unlock command clears the PPB Lock Bit, allowing for sector PPBs modifications. Asserting RESET#, taking the device through a power-on reset, or issuing the PPB Lock Bit Set command sets the PPB Lock Bit to a “1” when the Password Mode Lock Bit is not set.

If the Password Mode Locking Bit is not set, including Persistent Protection Mode, the PPB Lock Bit is cleared after power-up or hardware reset. The PPB Lock Bit is set by issuing the PPB Lock Bit Set command. Once set the only means for clearing the PPB Lock Bit is by issuing a hardware or power-up reset. The Password Unlock command is ignored in Persistent Protection Mode.

## High Voltage Sector Protection

Sector protection and unprotection may also be implemented using programming equipment. The procedure requires high voltage ( $V_{ID}$ ) to be placed on the RESET# pin. Refer to Figure 1 for details on this procedure. Note that for sector unprotect, all unprotected sectors must first be protected prior to the first sector write cycle.

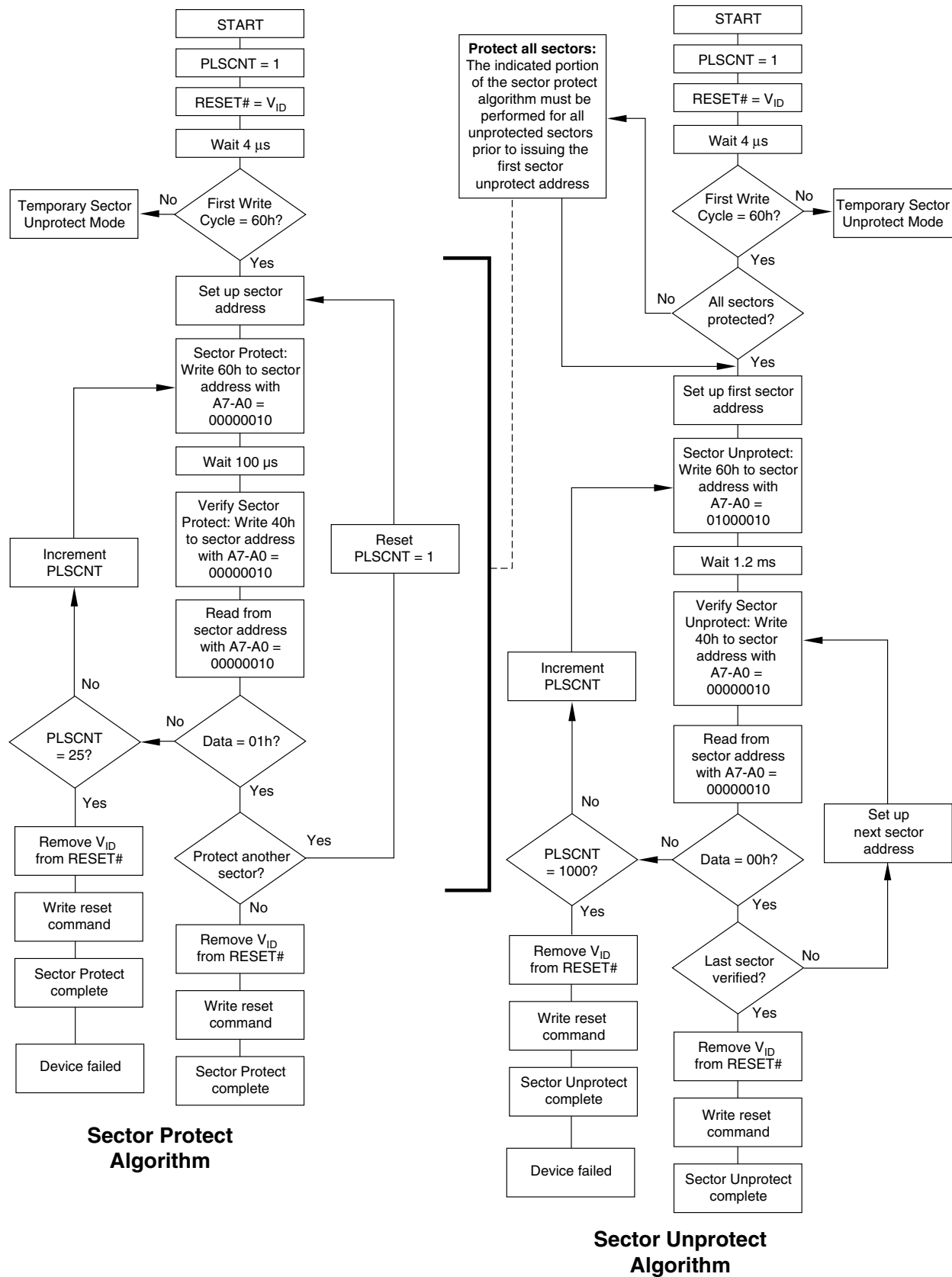
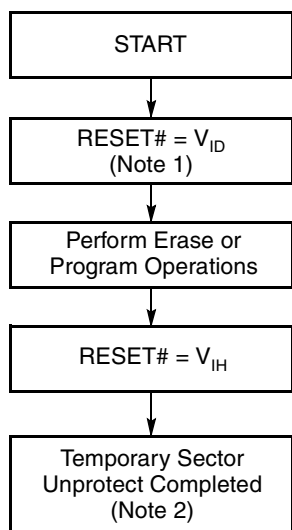


Figure 1. In-System Sector Protection/  
Sector Unprotection Algorithms

## Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to  $V_{ID}$ . During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once  $V_{ID}$  is removed from the RESET# pin, all the previously protected sectors are protected again. Figure 2 shows the algorithm, and Figure 24 shows the timing diagrams, for this feature. While PPB lock is set, the device cannot enter the Temporary Sector Unprotection Mode.



### Notes:

1. All protected sectors unprotected (If WP#/ACC =  $V_{IL}$ , sectors 0, 1, 268, 269 will remain protected).
2. All previously protected sectors are protected once again.

**Figure 2. Temporary Sector Unprotect Operation**

## SecSi™ (Secured Silicon) Sector Flash Memory Region

The SecSi (Secured Silicon) Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The 128-word SecSi sector is divided into 64 factory-lockable words that can be programmed and locked by the customer. The SecSi sector is located at addresses 000000h–00007Fh in both Persistent Protection mode and Password Protection mode. It uses

indicator bits (DQ6, DQ7) to indicate the factory-locked and customer-locked status of the part.

The system accesses the SecSi Sector through a command sequence (see “Enter SecSi™ Sector/Exit SecSi Sector Command Sequence”). After the system has written the Enter SecSi Sector command sequence, it may read the SecSi Sector by using the addresses normally occupied by the boot sectors. This mode of operation continues until the system issues the Exit SecSi Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to the normal address space.

### Factory-Locked Area (64 words)

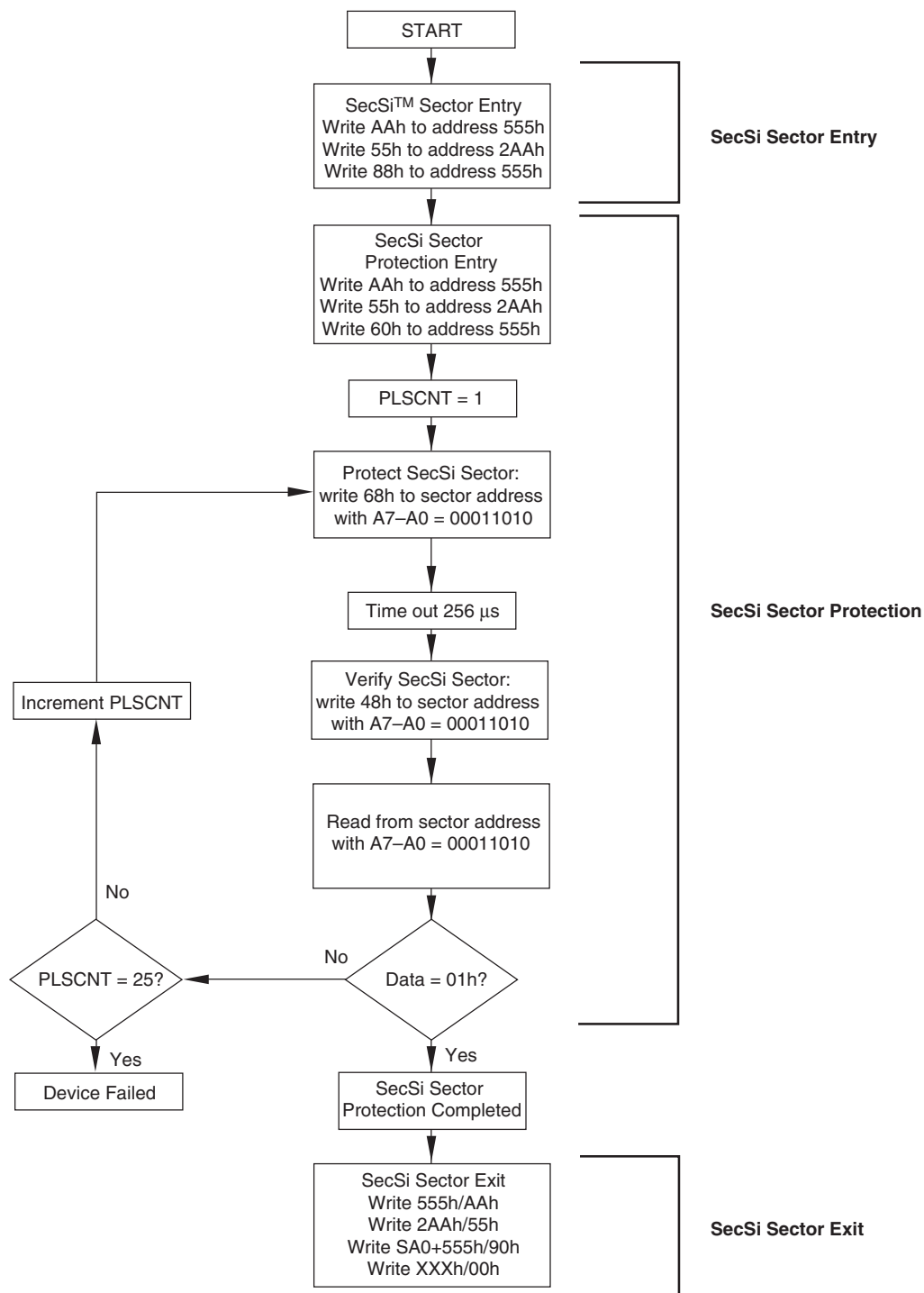
The factory-locked area of the SecSi Sector (000000h–00003Fh) is locked when the part is shipped, whether or not the area was programmed at the factory. The SecSi Sector Factory-locked Indicator Bit (DQ7) is permanently set to a “1”. AMD offers the ExpressFlash service to program the factory-locked area with a random ESN, a customer-defined code, or any combination of the two. Because only AMD can program and protect the factory-locked area, this method ensures the security of the ESN once the product is shipped to the field. Contact an AMD representative for details on using AMD’s ExpressFlash service. *Note that the ACC function and unlock bypass modes are not available when the SecSi Sector is enabled.*

### Customer-Lockable Area (64 words)

The customer-lockable area of the SecSi Sector (000040h–00007Fh) is shipped unprotected, which allows the customer to program and optionally lock the area as appropriate for the application. The SecSi Sector Customer-locked Indicator Bit (DQ6) is shipped as “0” and can be permanently locked to “1” by issuing the SecSi Protection Bit Program Command. The SecSi Sector can be read any number of times, but can be programmed and locked only once. Note that the accelerated programming (ACC) and unlock bypass functions are not available when programming the SecSi Sector.

The Customer-lockable SecSi Sector area can be protected using one of the following procedures:

- Follow the SecSi Sector protection algorithm as shown in Figure 3. This allows in-system protection of the SecSi Sector Region without raising any device pin to a high voltage. Note that this method is only applicable to the SecSi Sector.



**Figure 3. PDL127H/129H SecSi Sector Protection Algorithm**

- To verify the protect/unprotect status of the SecSi Sector, follow the algorithm shown in Figure 4.

Once the SecSi Sector is locked and verified, the system must write the Exit SecSi Sector Region command sequence to return to reading and writing the remainder of the array.

The SecSi Sector lock must be used with caution since, once locked, there is no procedure available for

unlocking the SecSi Sector area and none of the bits in the SecSi Sector memory space can be modified in any way.

#### SecSi Sector Protection Bits

The SecSi Sector Protection Bits prevent programming of the SecSi Sector memory area. Once set, the

SecSi Sector memory area contents are non-modifiable.

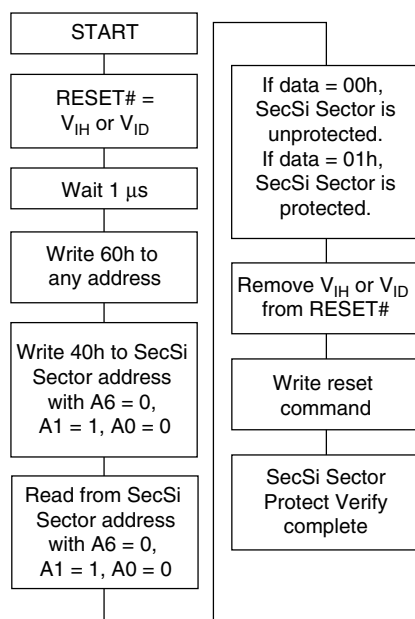


Figure 4. SecSi Sector Protect Verify

## Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes. In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during  $V_{CC}$  power-up and power-down transitions, or from system noise.

### Low $V_{CC}$ Write Inhibit

When  $V_{CC}$  is less than  $V_{LKO}$ , the device does not accept any write cycles. This protects data during  $V_{CC}$  power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until  $V_{CC}$  is greater than  $V_{LKO}$ . The system must provide the proper signals to the control pins to prevent unintentional writes when  $V_{CC}$  is greater than  $V_{LKO}$ .

### Write Pulse “Glitch” Protection

Noise pulses of less than 3 ns (typical) on OE#, CE#f1, CE#f2 or WE# do not initiate a write cycle.

### Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V<sub>IL</sub>, CE#f1 = CE#f2 = V<sub>IH</sub> or WE# = V<sub>IH</sub>. To initiate a write cycle, CE#f1/CE#f2 and WE# must be a logical zero while OE# is a logical one.

### Power-Up Write Inhibit

If WE# = CE#f1 = V<sub>IL</sub> and OE# = V<sub>IH</sub> during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

## COMMON FLASH MEMORY INTERFACE (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h, any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 11–14. To terminate reading CFI data, the system must write the reset command. The CFI Query mode is not accessible when the device is executing an Embedded Program or embedded Erase algorithm.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 11–14. The system must write the reset command to return the device to reading array data.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the World Wide Web at <http://www.amd.com/flash/cfi>. Alternatively, contact an AMD representative for copies of these documents.

Table 11. CFI Query Identification String

| Addresses         | Data                    | Description                                                  |
|-------------------|-------------------------|--------------------------------------------------------------|
| 10h<br>11h<br>12h | 0051h<br>0052h<br>0059h | Query Unique ASCII string "QRY"                              |
| 13h<br>14h        | 0002h<br>0000h          | Primary OEM Command Set                                      |
| 15h<br>16h        | 0040h<br>0000h          | Address for Primary Extended Table                           |
| 17h<br>18h        | 0000h<br>0000h          | Alternate OEM Command Set (00h = none exists)                |
| 19h<br>1Ah        | 0000h<br>0000h          | Address for Alternate OEM Extended Table (00h = none exists) |

Table 12. System Interface String

| Addresses | Data  | Description                                                                         |
|-----------|-------|-------------------------------------------------------------------------------------|
| 1Bh       | 0027h | V <sub>CC</sub> Min. (write/erase)<br>D7–D4: volt, D3–D0: 100 millivolt             |
| 1Ch       | 0036h | V <sub>CC</sub> Max. (write/erase)<br>D7–D4: volt, D3–D0: 100 millivolt             |
| 1Dh       | 0000h | V <sub>PP</sub> Min. voltage (00h = no V <sub>PP</sub> pin present)                 |
| 1Eh       | 0000h | V <sub>PP</sub> Max. voltage (00h = no V <sub>PP</sub> pin present)                 |
| 1Fh       | 0004h | Typical timeout per single byte/word write 2 <sup>N</sup> μs                        |
| 20h       | 0000h | Typical timeout for Min. size buffer write 2 <sup>N</sup> μs (00h = not supported)  |
| 21h       | 0009h | Typical timeout per individual block erase 2 <sup>N</sup> ms                        |
| 22h       | 0000h | Typical timeout for full chip erase 2 <sup>N</sup> ms (00h = not supported)         |
| 23h       | 0005h | Max. timeout for byte/word write 2 <sup>N</sup> times typical                       |
| 24h       | 0000h | Max. timeout for buffer write 2 <sup>N</sup> times typical                          |
| 25h       | 0004h | Max. timeout per individual block erase 2 <sup>N</sup> times typical                |
| 26h       | 0000h | Max. timeout for full chip erase 2 <sup>N</sup> times typical (00h = not supported) |

Table 13. Device Geometry Definition

| Addresses                | Data                             | Description                                                                                 |
|--------------------------|----------------------------------|---------------------------------------------------------------------------------------------|
| 27h                      | 0018h                            | Device Size = $2^N$ byte                                                                    |
| 28h<br>29h               | 0001h<br>0000h                   | Flash Device Interface description (refer to CFI publication 100)                           |
| 2Ah<br>2Bh               | 0000h<br>0000h                   | Max. number of byte in multi-byte write = $2^N$<br>(00h = not supported)                    |
| 2Ch                      | 0003h                            | Number of Erase Block Regions within device                                                 |
| 2Dh<br>2Eh<br>2Fh<br>30h | 0007h<br>0000h<br>0020h<br>0000h | Erase Block Region 1 Information<br>(refer to the CFI specification or CFI publication 100) |
| 31h<br>32h<br>33h<br>34h | 00FDh<br>0000h<br>0000h<br>0001h | Erase Block Region 2 Information<br>(refer to the CFI specification or CFI publication 100) |
| 35h<br>36h<br>37h<br>38h | 0007h<br>0000h<br>0020h<br>0000h | Erase Block Region 3 Information<br>(refer to the CFI specification or CFI publication 100) |
| 39h<br>3Ah<br>3Bh<br>3Ch | 0000h<br>0000h<br>0000h<br>0000h | Erase Block Region 4 Information<br>(refer to the CFI specification or CFI publication 100) |

**Table 14. Primary Vendor-Specific Extended Query**

| Addresses         | Data                    | Description                                                                                                                     |
|-------------------|-------------------------|---------------------------------------------------------------------------------------------------------------------------------|
| 40h<br>41h<br>42h | 0050h<br>0052h<br>0049h | Query-unique ASCII string "PRI"                                                                                                 |
| 43h               | 0031h                   | Major version number, ASCII (reflects modifications to the silicon)                                                             |
| 44h               | 0033h                   | Minor version number, ASCII (reflects modifications to the CFI table)                                                           |
| 45h               | 000Ch                   | Address Sensitive Unlock (Bits 1-0)<br>0 = Required, 1 = Not Required<br>Silicon Revision Number (Bits 7-2)                     |
| 46h               | 0002h                   | Erase Suspend<br>0 = Not Supported, 1 = To Read Only, 2 = To Read & Write                                                       |
| 47h               | 0001h                   | Sector Protect<br>0 = Not Supported, X = Number of sectors in per group                                                         |
| 48h               | 0001h                   | Sector Temporary Unprotect<br>00 = Not Supported, 01 = Supported                                                                |
| 49h               | 0007h                   | Sector Protect/Unprotect scheme<br>01 = 29F040 mode, 02 = 29F016 mode, 03 = 29F400, 04 = 29LV800 mode                           |
| 4Ah               | 00E7h                   | Simultaneous Operation<br>00 = Not Supported, X = Number of Sectors excluding Bank 1                                            |
| 4Bh               | 0000h                   | Burst Mode Type<br>00 = Not Supported, 01 = Supported                                                                           |
| 4Ch               | 0002h                   | Page Mode Type<br>00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page                                                        |
| 4Dh               | 0085h                   | ACC (Acceleration) Supply Minimum<br>00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV                                            |
| 4Eh               | 0095h                   | ACC (Acceleration) Supply Maximum<br>00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV                                            |
| 4Fh               | 0001h                   | Top/Bottom Boot Sector Flag<br>00h = Uniform device, 02h = Bottom Boot Device, 03h = Top Boot Device, 04h = Both Top and Bottom |
| 50h               | 0001h                   | Program Suspend<br>0 = Not supported, 1 = Supported                                                                             |
| 57h               | 0004h                   | Bank Organization<br>00 = Data at 4Ah is zero, X = Number of Banks                                                              |
| 58h               | 0027h                   | Bank 1 Region Information<br>X = Number of Sectors in Bank 1                                                                    |
| 59h               | 0060h                   | Bank 2 Region Information<br>X = Number of Sectors in Bank 2                                                                    |
| 5Ah               | 0060h                   | Bank 3 Region Information<br>X = Number of Sectors in Bank 3                                                                    |
| 5Bh               | 0027h                   | Bank 4 Region Information<br>X = Number of Sectors in Bank 4                                                                    |

## COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Table 15 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** may place the device in an unknown state. A reset command is then required to return the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#f1/CE#f2 (PDL129H only), whichever happens later. All data is latched on the rising edge of WE# or CE#f1/CE#f2 (PDL129H only), whichever happens first. Refer to the [Flash AC Characteristics](#) section for timing diagrams.

### Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. Each bank is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector within the same bank. The system can read array data using the standard read timing, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See the Erase Suspend/Erase Resume Commands section for more information.

The system *must* issue the reset command to return a bank to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the bank is in the autoselect mode. See the next section, Reset Command, for more information.

See also [Requirements for Reading Array Data](#) in the [MCP Device Bus Operations](#) section for more information. The [Read-Only Operations – Am29PDL127H](#) and [Read-Only Operations – Am29PDL129H](#) tables provide the read parameters, and [Figure 14](#) shows the timing diagram.

### Reset Command

Writing the reset command resets the banks to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before

erasing begins. This resets the bank to which the system was writing to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the bank to which the system was writing to the read mode. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the banks to the read mode (or erase-suspend-read mode if that bank was in Erase Suspend).

### Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. The autoselect command sequence may be written to an address within a bank that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the other bank.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. The bank then enters the autoselect mode. The system may read any number of autoselect codes without reinitiating the command sequence.

Table 15 shows the address and data requirements. To determine sector protection information, the system must write to the appropriate bank address (BA) and sector address (SA). [Table 4](#) shows the address range and bank number associated with each sector.

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the bank was previously in Erase Suspend).

## Enter SecSi™ Sector/Exit SecSi Sector Command Sequence

The SecSi Sector region provides a secured data area containing a random, eight word electronic serial number (ESN). The system can access the SecSi Sector region by issuing the three-cycle Enter SecSi Sector command sequence. The device continues to access the SecSi Sector region until the system issues the four-cycle Exit SecSi Sector command sequence. The Exit SecSi Sector command sequence returns the device to normal operation. The SecSi Sector is not accessible when the device is executing an Embedded Program or embedded Erase algorithm. Table 15 shows the address and data requirements for both command sequences. See also “SecSi™ (Secured Silicon) Sector Flash Memory Region” for further information. *Note that the ACC function and unlock bypass modes are not available when the SecSi Sector is enabled.*

## Word Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 15 shows the address and data requirements for the program command sequence.

When the Embedded Program algorithm is complete, that bank then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. Refer to the Write Operation Status section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the program operation. *Note that the SecSi sector, autoselect, and CFI functions are unavailable when the SecSi Sector is enabled.* The program command sequence should be reinitiated once that bank has returned to the read mode, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from “0” back to a “1.”** Attempting to do so may cause that bank to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still “0.” Only erase operations can convert a “0” to a “1.”

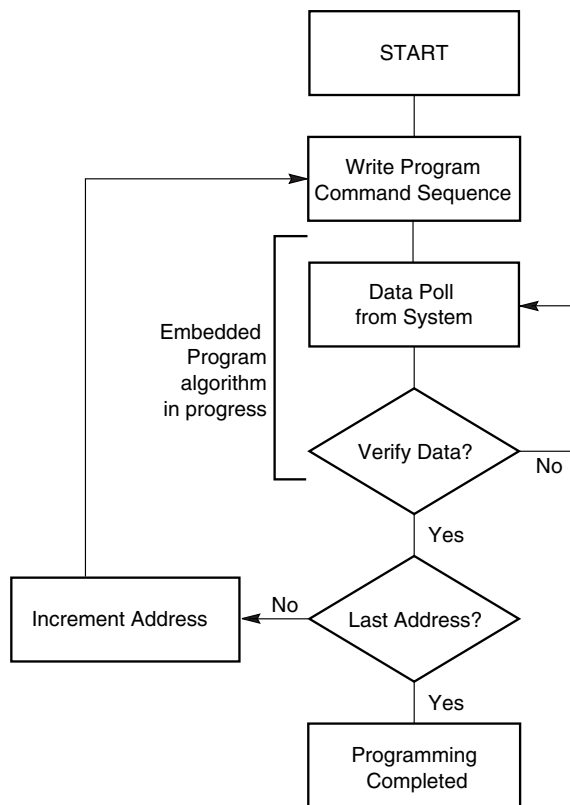
## Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program data to a bank faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. That bank then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 15 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence.

The device offers accelerated program operations through the WP#/ACC pin. When the system asserts  $V_{HH}$  on the WP#/ACC pin, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the WP#/ACC pin to accelerate the operation. *Note that the WP#/ACC pin must not be at  $V_{HH}$  any operation other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.*

Figure 5 illustrates the algorithm for the program operation. Refer to the [Erase and Program Operations](#) table in the AC Characteristics section for parameters, and Figures 17 and 18 for timing diagrams.



**Note:** See Table 15 for program command sequence.

**Figure 5. Program Operation**

## Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 15 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. Refer to the Write Operation Status section for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. *Note that the SecSi sector, autoselect, and CFI functions are un-*

*available when the SecSi Sector is enabled.* If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 6 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 19 for timing diagrams.

## Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 15 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50  $\mu$ s occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50  $\mu$ s, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **Any command other than Sector Erase or Erase Suspend during the time-out period resets that bank to the read mode.** *Note that the SecSi sector, autoselect, and CFI functions are unavailable when the SecSi Sector is enabled.* The system must rewrite the command sequence and any additional addresses and commands.

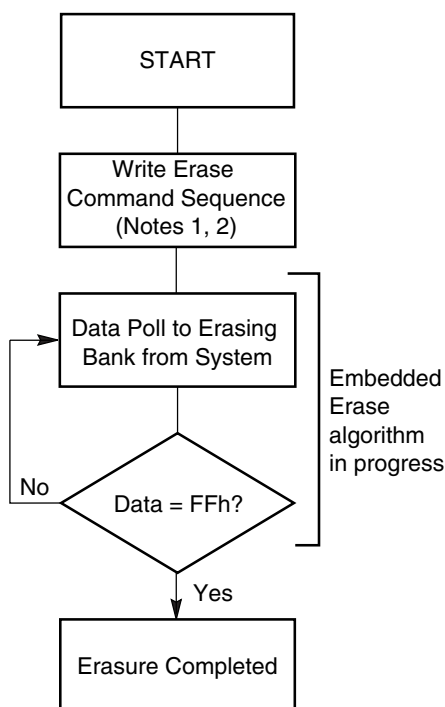
The system can monitor DQ3 to determine if the sector erase timer has timed out (See the section on DQ3: Sector Erase Timer). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing bank. The system can determine the status of the erase operation by reading

DQ7, DQ6, DQ2, or RY/BY# in the erasing bank. Refer to the Write Operation Status section for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 6 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 19 section for timing diagrams.



**Notes:**

1. See Table 15 for erase command sequence.
2. See the section on DQ3 for information on the sector erase timer.

**Figure 6. Erase Operation**

## Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. The bank address is required when writing this command. This command is valid only during the sector erase operation, including the 80  $\mu$ s time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written dur-

ing the chip erase operation or Embedded Program algorithm.

When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of 20  $\mu$ s to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation. Addresses are “don’t-cares” when writing the Erase suspend command.

After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Write Operation Status section for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard Word Program operation. Refer to the Write Operation Status section for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. Refer to the [Autoselect Command Sequence](#) sections for details.

To resume the sector erase operation, the system must write the Erase Resume command (address bits are don’t care). The bank address of the erase-suspended bank is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

## Password Program Command

The Password Program Command permits programming the password that is used as part of the hardware protection scheme. The actual password is 64-bits long. Four Password Program commands are required to program the password. The system must enter the unlock cycle, password program command (38h) and the program address/data for each portion of the password when programming. There are no provisions for entering the 2-cycle unlock cycle, the pass-

word program command, and all the password data. There is no special addressing order required for programming the password. Also, when the password is undergoing programming, Simultaneous Operation is disabled. Read operations to any memory location will return the programming status. Once programming is complete, the user must issue a Read/Reset command to return the device to normal operation. Once the Password is written and verified, the Password Mode Locking Bit must be set in order to prevent verification. The Password Program Command is only capable of programming “0”s. Programming a “1” after a cell is programmed as a “0” results in a time-out by the Embedded Program Algorithm™ with the cell remaining as a “0”. The password is all ones when shipped from the factory. All 64-bit password combinations are valid as a password.

### Password Verify Command

The Password Verify Command is used to verify the Password. The Password is verifiable only when the Password Mode Locking Bit is not programmed. If the Password Mode Locking Bit is programmed and the user attempts to verify the Password, the device will always drive all F's onto the DQ data bus.

The Password Verify command is permitted if the SecSi sector is enabled. Also, the device will not operate in Simultaneous Operation when the Password Verify command is executed. Only the password is returned regardless of the bank address. The lower two address bits (A1-A0) are valid during the Password Verify. Writing the Read/Reset command returns the device back to normal operation.

### Password Protection Mode Locking Bit Program Command

The Password Protection Mode Locking Bit Program Command programs the Password Protection Mode Locking Bit, which prevents further verifies or updates to the Password. Once programmed, the Password Protection Mode Locking Bit cannot be erased! If the Password Protection Mode Locking Bit is verified as program without margin, the Password Protection Mode Locking Bit Program command can be executed to improve the program margin. Once the Password Protection Mode Locking Bit is programmed, the Persistent Sector Protection Locking Bit program circuitry is disabled, thereby forcing the device to remain in the Password Protection mode. Exiting the Mode Locking Bit Program command is accomplished by writing the Read/Reset command.

### Persistent Sector Protection Mode Locking Bit Program Command

The Persistent Sector Protection Mode Locking Bit Program Command programs the Persistent Sector

Protection Mode Locking Bit, which prevents the Password Mode Locking Bit from ever being programmed. *If the Persistent Sector Protection Mode Locking Bit is verified as programmed without margin, the Persistent Sector Protection Mode Locking Bit Program Command should be reissued to improve program margin.* By disabling the program circuitry of the Password Mode Locking Bit, the device is forced to remain in the Persistent Sector Protection mode of operation, once this bit is set. Exiting the Persistent Protection Mode Locking Bit Program command is accomplished by writing the Read/Reset command.

### SecSi Sector Protection Bit Program Command

The SecSi Sector Protection Bit Program Command programs the SecSi Sector Protection Bit, which prevents the SecSi sector memory from being cleared. *If the SecSi Sector Protection Bit is verified as programmed without margin, the SecSi Sector Protection Bit Program Command should be reissued to improve program margin.* Exiting the V<sub>CC</sub>-level SecSi Sector Protection Bit Program Command is accomplished by writing the Read/Reset command.

### PPB Lock Bit Set Command

The PPB Lock Bit Set command is used to set the PPB Lock bit if it is cleared either at reset or if the Password Unlock command was successfully executed. There is no PPB Lock Bit Clear command. Once the PPB Lock Bit is set, it cannot be cleared unless the device is taken through a power-on clear or the Password Unlock command is executed. Upon setting the PPB Lock Bit, the PPBs are latched into the DYBs. If the Password Mode Locking Bit is set, the PPB Lock Bit status is reflected as set, even after a power-on reset cycle. Exiting the PPB Lock Bit Set command is accomplished by writing the Read/Reset command (only in the Persistent Protection Mode).

### DYB Write Command

The DYB Write command is used to set or clear a DYB for a given sector. The high order address bits A22–A12 for PDL127 and A21–A12 for PDL129H are issued at the same time as the code 01h or 00h on DQ7–DQ0. All other DQ data bus pins are ignored during the data write cycle. The DYBs are modifiable at any time, regardless of the state of the PPB or PPB Lock Bit. The DYBs are cleared at power-up or hardware reset. Exiting the DYB Write command is accomplished by writing the Read/Reset command.

### Password Unlock Command

The Password Unlock command is used to clear the PPB Lock Bit so that the PPBs can be unlocked for modification, thereby allowing the PPBs to become ac-

cessible for modification. The exact password must be entered in order for the unlocking function to occur. This command cannot be issued any faster than 2  $\mu$ s at a time to prevent a hacker from running through all 64-bit combinations in an attempt to correctly match a password. If the command is issued before the 2  $\mu$ s execution window for each portion of the unlock, the command will be ignored.

Once the Password Unlock command is entered, the RY/BY# indicates that the device is busy. Approximately 1  $\mu$ s is required for each portion of the unlock. Once the first portion of the password unlock completes (RY/BY# is not low or DQ6 does not toggle when read), the next part of the password is written. The system must thus monitor RY/BY# or the status bits to confirm when to write the next portion of the password. Seven cycles are required to successfully clear the PPB Lock Bit.

### PPB Program Command

The PPB Program command is used to program, or set, a given PPB. Each PPB is individually programmed (but is bulk erased with the other PPBs). The specific sector address (A21–A12) are written at the same time as the program command 60h with A6 = 0. If the PPB Lock Bit is set and the corresponding PPB is set for the sector, the PPB Program command will not execute and the command will time-out without programming the PPB.

*After programming a PPB, two additional cycles are needed to determine whether the PPB has been programmed with margin. If the PPB has been programmed without margin, the program command should be reissued to improve the program margin. Also note that the total number of PPB program/erase cycles is limited to 100 cycles. Cycling the PPBs beyond 100 cycles is not guaranteed.*

The PPB Program command does not follow the Embedded Program algorithm.

### All PPB Erase Command

The All PPB Erase command is used to erase all PPBs in bulk. There is no means for individually erasing a specific PPB. Unlike the PPB program, no specific sector address is required. However, when the PPB erase command is written all Sector PPBs are erased in parallel. If the PPB Lock Bit is set the ALL PPB Erase command will not execute and the command will time-out without erasing the PPBs. After erasing the PPBs, two additional cycles are needed to determine whether the PPB has been erased with margin. If the PPBs has been erased without margin,

the erase command should be reissued to improve the program margin.

It is the responsibility of the user to preprogram all PPBs prior to issuing the All PPB Erase command. If the user attempts to erase a cleared PPB, over-erase may occur making it difficult to program the PPB at a later time. Also note that the total number of PPB program/erase cycles is limited to 100 cycles. Cycling the PPBs beyond 100 cycles is not guaranteed.

### DYB Write Command

The DYB Write command is used for setting the DYB, which is a volatile bit that is cleared at reset. There is one DYB per sector. If the PPB is set, the sector is protected regardless of the value of the DYB. If the PPB is cleared, setting the DYB to a 1 protects the sector from programs or erases. Since this is a volatile bit, removing power or resetting the device will clear the DYBs. The bank address is latched when the command is written.

### PPB Lock Bit Set Command

The PPB Lock Bit set command is used for setting the DYB, which is a volatile bit that is cleared at reset. There is one DYB per sector. If the PPB is set, the sector is protected regardless of the value of the DYB. If the PPB is cleared, setting the DYB to a 1 protects the sector from programs or erases. Since this is a volatile bit, removing power or resetting the device will clear the DYBs. The bank address is latched when the command is written.

### PPB Status Command

The programming of the PPB for a given sector can be verified by writing a PPB status verify command to the device.

### PPB Lock Bit Status Command

The programming of the PPB Lock Bit for a given sector can be verified by writing a PPB Lock Bit status verify command to the device.

### Sector Protection Status Command

The programming of either the PPB or DYB for a given sector or sector group can be verified by writing a Sector Protection Status command to the device.

Note that there is no single command to independently verify the programming of a DYB for a given sector group.

## Command Definitions Tables

Table 15. Memory Array Command Definitions

| Command (Notes)            |                                  | Cycles | Bus Cycles (Notes 1–4) |      |      |      |      |      |         |               |         |           |         |      |
|----------------------------|----------------------------------|--------|------------------------|------|------|------|------|------|---------|---------------|---------|-----------|---------|------|
|                            |                                  |        | Addr                   | Data | Addr | Data | Addr | Data | Addr    | Data          | Addr    | Data      | Addr    | Data |
| Read (5)                   |                                  | 1      | RA                     | RD   |      |      |      |      |         |               |         |           |         |      |
| Reset (6)                  |                                  | 1      | XXX                    | F0   |      |      |      |      |         |               |         |           |         |      |
| Autoselect<br>(Note 7)     | Manufacturer ID                  | 4      | 555                    | AA   | 2AA  | 55   | 555  | 90   | (BA)X00 | 01            |         |           |         |      |
|                            | Device ID (10)                   | 6      | 555                    | AA   | 2AA  | 55   | 555  | 90   | (BA)X01 | 7E            | (BA)X0E | (Note 10) | (BA)X0F | 00   |
|                            | SecSi Sector Factory Protect (8) | 4      | 555                    | AA   | 2AA  | 55   | 555  | 90   | X03     | (see note 8)  |         |           |         |      |
|                            | Sector Group Protect Verify (9)  | 4      | 555                    | AAA  | 2AA  | 55   | 555  | 90   | (SA)X02 | XX00/<br>XX01 |         |           |         |      |
| Program                    |                                  | 4      | 555                    | AA   | 2AA  | 55   | 555  | A0   | PA      | PD            |         |           |         |      |
| Chip Erase                 |                                  | 6      | 555                    | AA   | 2AA  | 55   | 555  | 80   | 555     | AA            | 2AA     | 55        | 555     | 10   |
| Sector Erase               |                                  | 6      | 555                    | AA   | 2AA  | 55   | 555  | 80   | 555     | AA            | 2AA     | 55        | SA      | 30   |
| Program/Erase Suspend (11) |                                  | 1      | BA                     | B0   |      |      |      |      |         |               |         |           |         |      |
| Program/Erase Resume (12)  |                                  | 1      | BA                     | 30   |      |      |      |      |         |               |         |           |         |      |
| CFI Query (13)             |                                  | 1      | 55                     | 98   |      |      |      |      |         |               |         |           |         |      |
| Accelerated Program (15)   |                                  | 2      | XX                     | A0   | PA   | PD   |      |      |         |               |         |           |         |      |
| Unlock Bypass Entry (15)   |                                  | 3      | 555                    | AA   | 2AA  | 55   | 555  | 20   |         |               |         |           |         |      |
| Unlock Bypass Program (15) |                                  | 2      | XX                     | A0   | PA   | PD   |      |      |         |               |         |           |         |      |
| Unlock Bypass Erase (15)   |                                  | 2      | XX                     | 80   | XX   | 10   |      |      |         |               |         |           |         |      |
| Unlock Bypass CFI (13, 15) |                                  | 1      | XX                     | 98   |      |      |      |      |         |               |         |           |         |      |
| Unlock Bypass Reset (15)   |                                  | 2      | XXX                    | 90   | XXX  | 00   |      |      |         |               |         |           |         |      |

**Legend:**

BA = Address of bank switching to autoselect mode, bypass mode, or erase operation. Determined by A22:A20, (A21:A20 for PDL129) see Tables 4 and 7 for more detail.

PA = Program Address (A22:A0) (A21:A0 for PDL129). Addresses latch on falling edge of WE# or CE#1/CE#2 (PDL129 only) pulse, whichever happens later.

PD = Program Data (DQ15:DQ0) written to location PA. Data latches on rising edge of WE# or CE#1/CE#2 (PDL129 only) pulse, whichever happens first.

RA = Read Address (A22:A0) (A21:A0 for PDL129).

RD = Read Data (DQ15:DQ0) from location RA.

SA = Sector Address (A22:A12) (A21:A12 for PDL129) for verifying (in autoselect mode) or erasing.

WD = Write Data. See “Configuration Register” definition for specific write data. Data latched on rising edge of WE#.

X = Don't care

**Notes:**

- See Table 1 for description of bus operations.
- All values are in hexadecimal.
- Shaded cells in table denote read cycles. All other cycles are write operations.
- During unlock and command cycles, when lower address bits are 555 or 2AAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.
- No unlock or command cycles required when bank is reading array data.
- The Reset command is required to return to reading array (or to erase-suspend-read mode if previously in Erase Suspend) when bank is in autoselect mode, or if DQ5 goes high (while bank is providing status information).
- Fourth cycle of autoselect command sequence is a read cycle. System must provide bank address to obtain manufacturer ID or device ID information. See Autoselect Command Sequence section for more information.
- The data is C0h for factory or customer locked and 80h for factory locked.
- The data is 00h for an unprotected sector group and 01h for a protected sector group.
- Device ID must be read across cycles 4, 5, and 6. Data is 20 for Am29PDL127H and 21 for Am29PDL129H.
- System may read and program in non-erasing sectors, or enter autoselect mode, when in Program/Erase Suspend mode. Program/Erase Suspend command is valid only during a sector erase operation, and requires bank address.
- Program/Erase Resume command is valid only during Erase Suspend mode, and requires bank address.
- Command is valid when device is ready to read array data or when device is in autoselect mode.
- WP#/ACC must be at V<sub>ID</sub> during the entire operation of command.
- Unlock Bypass Entry command is required prior to any Unlock Bypass operation. Unlock Bypass Reset command is required to return to the reading array.

Table 16. Sector Protection Command Definitions

| Command (Notes)                     | Cycles | Bus Cycles (Notes 1-4) |      |      |      |      |      |          |          |        |        |        |        |        |        |
|-------------------------------------|--------|------------------------|------|------|------|------|------|----------|----------|--------|--------|--------|--------|--------|--------|
|                                     |        | Addr                   | Data | Addr | Data | Addr | Data | Addr     | Data     | Addr   | Data   | Addr   | Data   | Addr   | Data   |
| Reset                               | 1      | XXX                    | F0   |      |      |      |      |          |          |        |        |        |        |        |        |
| SecSi Sector Entry                  | 3      | 555                    | AA   | 2AA  | 55   | 555  | 88   |          |          |        |        |        |        |        |        |
| SecSi Sector Exit                   | 4      | 555                    | AA   | 2AA  | 55   | 555  | 90   | XX       | 00       |        |        |        |        |        |        |
| SecSi Protection Bit Program (5, 6) | 6      | 555                    | AA   | 2AA  | 55   | 555  | 60   | OW       | 68       | OW     | 48     | OW     | RD(0)  |        |        |
| SecSi Protection Bit Status         | 5      | 555                    | AA   | 2AA  | 55   | 555  | 60   | OW       | 48       | OW     | RD(0)  |        |        |        |        |
| Password Program (5, 7, 8)          | 4      | 555                    | AA   | 2AA  | 55   | 555  | 38   | XX[0-3]  | PD[0-3]  |        |        |        |        |        |        |
| Password Verify (6, 8, 9)           | 4      | 555                    | AA   | 2AA  | 55   | 555  | C8   | PWA[0-3] | PWD[0-3] |        |        |        |        |        |        |
| Password Unlock (7, 10, 11)         | 7      | 555                    | AA   | 2AA  | 55   | 555  | 28   | PWA[0]   | PWD[0]   | PWA[1] | PWD[1] | PWA[2] | PWD[2] | PWA[3] | PWD[3] |
| PPB Program (5, 6, 12, 17)          | 6      | 555                    | AA   | 2AA  | 55   | 555  | 60   | (SA)WP   | 68       | (SA)WP | 48     | (SA)WP | RD(0)  |        |        |
| PPB Status                          | 5      | 555                    | AA   | 2AA  | 55   | 555  | 60   | (SA)WP   | 48       | (SA)WP | RD(0)  |        |        |        |        |
| All PPB Erase (5, 6, 13, 14)        | 6      | 555                    | AA   | 2AA  | 55   | 555  | 60   | WP       | 60       | (SA)   | 40     | (SA)WP | RD(0)  |        |        |
| PPB Lock Bit Set (17)               | 3      | 555                    | AA   | 2AA  | 55   | 555  | 78   |          |          |        |        |        |        |        |        |
| PPB Lock Bit Status (15)            | 4      | 555                    | AA   | 2AA  | 55   | 555  | 58   | SA       | RD(1)    |        |        |        |        |        |        |
| DYB Write (7)                       | 4      | 555                    | AA   | 2AA  | 55   | 555  | 48   | SA       | X1       |        |        |        |        |        |        |
| DYB Erase (7)                       | 4      | 555                    | AA   | 2AA  | 55   | 555  | 48   | SA       | X0       |        |        |        |        |        |        |
| DYB Status (6, 18)                  | 4      | 555                    | AA   | 2AA  | 55   | 555  | 58   | SA       | RD(0)    |        |        |        |        |        |        |
| PPMLB Program (5, 6, 12)            | 6      | 555                    | AA   | 2AA  | 55   | 555  | 60   | PL       | 68       | PL     | 48     | PL     | RD(0)  |        |        |
| PPMLB Status (5)                    | 5      | 555                    | AA   | 2AA  | 55   | 555  | 60   | PL       | 48       | PL     | RD(0)  |        |        |        |        |
| SPMLB Program (5, 6, 12)            | 6      | 555                    | AA   | 2AA  | 55   | 555  | 60   | SL       | 68       | SL     | 48     | SL     | RD(0)  |        |        |
| SPMLB Status (5)                    | 5      | 555                    | AA   | 2AA  | 55   | 555  | 60   | SL       | 48       | SL     | RD(0)  |        |        |        |        |

**Legend:**

DYB = Dynamic Protection Bit

OW = Address (A7:A0) is (00011010)

PD[3:0] = Password Data (1 of 4 portions)

PPB = Persistent Protection Bit

PWA = Password Address. A1:A0 selects portion of password.

PWD = Password Data being verified.

PL = Password Protection Mode Lock Address (A7:A0) is (00001010)

RD(0) = Read Data DQ0 for protection indicator bit.

RD(1) = Read Data DQ1 for PPB Lock status.

SA = Sector Address where security command applies. Address bits A21:A12 uniquely select any sector.

SL = Persistent Protection Mode Lock Address (A7:A0) is (00010010)

WP = PPB Address (A7:A0) is (00000010) (Note 16)

X = Don't care

PPMLB = Password Protection Mode Locking Bit

SPMLB = Persistent Protection Mode Locking Bit

- See Table 1 for description of bus operations.
- All values are in hexadecimal.
- Shaded cells in table denote read cycles. All other cycles are write operations.
- During unlock and command cycles, when lower address bits are 555 or 2AAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.
- The reset command returns device to reading array.
- Cycle 4 programs the addressed locking bit. Cycles 5 and 6 validate bit has been fully programmed when DQ0 = 1. If DQ0 = 0 in cycle 6, program command must be issued and verified again.
- Data is latched on the rising edge of WE#.
- Entire command sequence must be entered for each portion of password.
- Command sequence returns FFh if PPMLB is set.
- The password is written over four consecutive cycles, at addresses 0-3.
- A 2  $\mu$ s timeout is required between any two portions of password.
- A 100  $\mu$ s timeout is required between cycles 4 and 5.
- A 1.2 ms timeout is required between cycles 4 and 5.
- Cycle 4 erases all PPBs. Cycles 5 and 6 validate bits have been fully erased when DQ0 = 0. If DQ0 = 1 in cycle 6, erase command must be issued and verified again. Before issuing erase command, all PPBs should be programmed to prevent PPB overerasure.
- DQ1 = 1 if PPB locked, 0 if unlocked.
- For PDL128G and PDL640G, the WP address is 0111010. The EP address (PPB Erase Address) is 1111010.
- Following the final cycle of the command sequence, the user must write the first three cycles of the Autoselect command and then write a Reset command.
- If checking the DYB status of sectors in multiple banks, the user must follow Note 17 before crossing a bank boundary.

## WRITE OPERATION STATUS

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 17 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

### DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1  $\mu$ s, then that bank returns to the read mode.

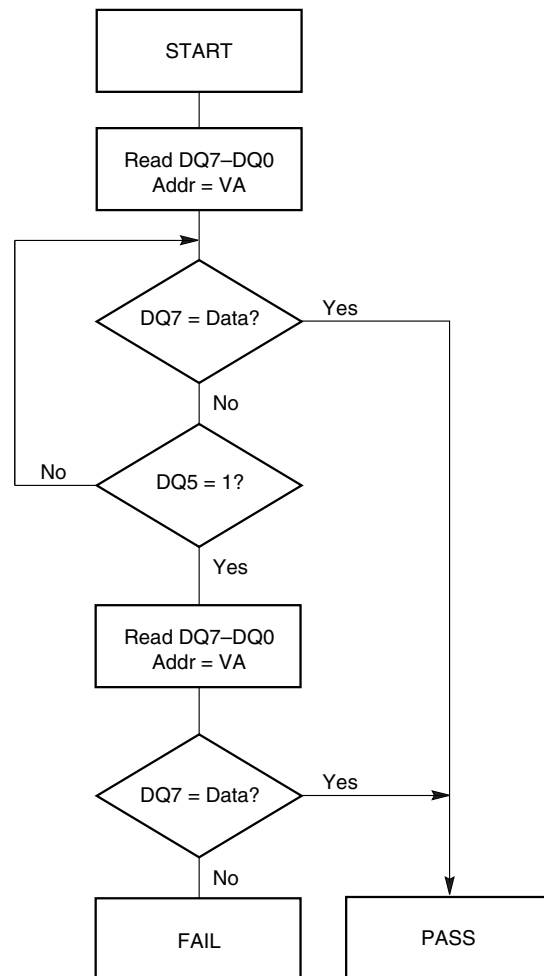
During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 400  $\mu$ s, then the bank returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ15–DQ0 on the following read cycles. Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ15–DQ0 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has com-

pleted the program or erase operation and DQ7 has valid data, the data outputs on DQ15–DQ0 may be still invalid. Valid data on DQ15–DQ0 will appear on successive read cycles.

Table 17 shows the outputs for Data# Polling on DQ7. Figure 7 shows the Data# Polling algorithm. Figure 7 in the Flash AC Characteristics section shows the Data# Polling timing diagram.



#### Notes:

1. VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.
2. DQ7 should be rechecked even if DQ5 = “1” because DQ7 may change simultaneously with DQ5.

**Figure 7. Data# Polling Algorithm**

## RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to  $V_{CC}$ .

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or one of the banks is in the erase-suspend-read mode.

Table 17 shows the outputs for RY/BY#.

## DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE#f1 to control the read cycles. When the operation is complete, DQ6 stops toggling.

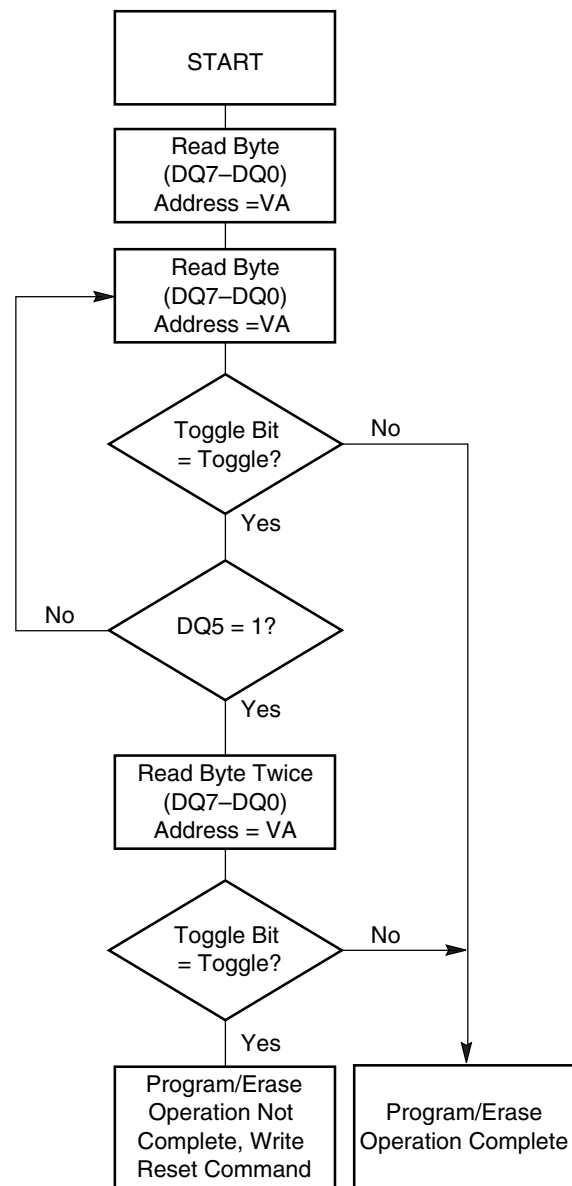
After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 400  $\mu$ s, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1  $\mu$ s after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 17 shows the outputs for Toggle Bit I on DQ6. Figure 8 shows the toggle bit algorithm. Figure 22 in the “Flash AC Characteristics” section shows the toggle bit timing diagrams. Figure 23 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2: Toggle Bit II.



**Note:** The system should recheck the toggle bit even if DQ5 = “1” because the toggle bit may stop toggling as DQ5 changes to “1.” See the subsections on DQ6 and DQ2 for more information.

Figure 8. Toggle Bit Algorithm

## DQ2: Toggle Bit II

The “Toggle Bit II” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE#1 to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 17 to compare outputs for DQ2 and DQ6.

Figure 8 shows the toggle bit algorithm in flowchart form, and the section “DQ2: Toggle Bit II” explains the algorithm. See also the DQ6: Toggle Bit I subsection. [Figure 22](#) shows the toggle bit timing diagram. Figure 23 shows the differences between DQ2 and DQ6 in graphical form.

## Reading Toggle Bits DQ6/DQ2

Refer to Figure 8 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 8).

## DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1,” indicating that the program or erase cycle was not successfully completed.

The device may output a “1” on DQ5 if the system tries to program a “1” to a location that was previously programmed to “0.” **Only an erase operation can change a “0” back to a “1.”** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a “1.”

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

## DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a “0” to a “1.” See also the Sector Erase Command Sequence section.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is “1,” the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is “0,” the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 17 shows the status of DQ3 relative to the other status bits.

Table 17. Write Operation Status

| Status             |                            |                            | DQ7<br>(Note 2) | DQ6       | DQ5<br>(Note 1) | DQ3  | DQ2<br>(Note 2) | RY/BY# |
|--------------------|----------------------------|----------------------------|-----------------|-----------|-----------------|------|-----------------|--------|
| Standard Mode      | Embedded Program Algorithm |                            | DQ7#            | Toggle    | 0               | N/A  | No toggle       | 0      |
|                    | Embedded Erase Algorithm   |                            | 0               | Toggle    | 0               | 1    | Toggle          | 0      |
| Erase Suspend Mode | Erase-Suspend-Read         | Erase Suspended Sector     | 1               | No toggle | 0               | N/A  | Toggle          | 1      |
|                    |                            | Non-Erase Suspended Sector | Data            | Data      | Data            | Data | Data            | 1      |
|                    | Erase-Suspend-Program      |                            | DQ7#            | Toggle    | 0               | N/A  | N/A             | 0      |

**Notes:**

1. DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.
2. DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
3. When reading write operation status bits, the system must always provide the bank address where the Embedded Algorithm is in progress. The device outputs array data if the system addresses a non-busy bank.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature

Plastic Packages . . . . .  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Ambient Temperature

with Power Applied. . . . .  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

Voltage with Respect to Ground

$V_{CCf}$ ,  $V_{CCS}$  (Note 1) . . . . .  $-0.5\text{ V}$  to  $+4.0\text{ V}$

RESET# (Note 2) . . . . .  $-0.5\text{ V}$  to  $+12.5\text{ V}$

WP#/ACC . . . . .  $-0.5\text{ V}$  to  $+10.5\text{ V}$

All other pins (Note 1) . . . . .  $-0.5\text{ V}$  to  $V_{CC} + 0.5\text{ V}$

Output Short Circuit Current (Note 3) . . . . . 200 mA

### Notes:

1. Minimum DC voltage on input or I/O pins is  $-0.5\text{ V}$ . During voltage transitions, input or I/O pins may overshoot  $V_{SS}$  to  $-2.0\text{ V}$  for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is  $V_{CC} + 0.5\text{ V}$ . See Figure 8. During voltage transitions, input or I/O pins may overshoot to  $V_{CC} + 2.0\text{ V}$  for periods up to 20 ns. See Figure 9.
2. Minimum DC input voltage on pins RESET#, and WP#/ACC is  $-0.5\text{ V}$ . During voltage transitions, WP#/ACC, and RESET# may overshoot  $V_{SS}$  to  $-2.0\text{ V}$  for periods of up to 20 ns. See Figure 8. Maximum DC input voltage on pin RESET# is  $+12.5\text{ V}$  which may overshoot to  $+14.0\text{ V}$  for periods up to 20 ns. Maximum DC input voltage on WP#/ACC is  $+9.5\text{ V}$  which may overshoot to  $+12.0\text{ V}$  for periods up to 20 ns.
3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

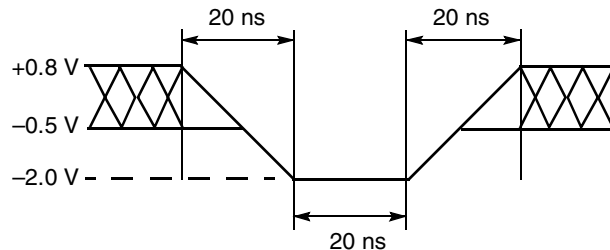


Figure 9. Maximum Negative Overshoot Waveform

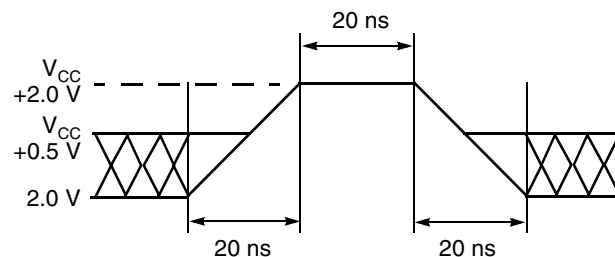


Figure 10. Maximum Positive Overshoot Waveform

## OPERATING RANGES

### Industrial (I) Devices

Ambient Temperature ( $T_A$ ) . . . . .  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

### $V_{CCf}/V_{CCS}$ Supply Voltages

$V_{CCf}/V_{CCS}$  for standard voltage range . .  $2.7\text{ V}$  to  $3.3\text{ V}$

Operating ranges define those limits between which the functionality of the device is guaranteed.

## ESD IMMUNITY

Spansion Flash memory Multi-Chip Products (MCPs) may contain component devices that are developed by FASL LLC ("Spansion components") and component

devices that are developed by a third party ("third-party components").

Spansion components are tested and guaranteed to the ESD immunity levels listed in the corresponding Spansion Flash memory Qualification Database. Third-party components are neither tested nor guaranteed by FASL LLC for ESD immunity. However, ESD test results for third-party components may be available from the component manufacturer. Component manufacturer contact information is listed in the Spansion MCP Qualification Report, when available.

The Spansion Flash memory Qualification Database and Spansion MCP Qualification Report are available from AMD and Fujitsu sales offices.

## DC CHARACTERISTICS

### CMOS Compatible

| Parameter Symbol | Parameter Description                                                 | Test Conditions                                                                 | Min    | Typ | Max            | Unit    |
|------------------|-----------------------------------------------------------------------|---------------------------------------------------------------------------------|--------|-----|----------------|---------|
| $I_{LI}$         | Input Load Current                                                    | $V_{IN} = V_{SS}$ to $V_{CC}$ ,<br>$V_{CC} = V_{CC\ max}$                       |        |     | $\pm 1.0$      | $\mu A$ |
| $I_{LIT}$        | A9, OE#, RESET# Input Load Current                                    | $V_{CC} = V_{CC\ max}$ ; $V_{ID} = 12.5\ V$                                     |        |     | 35             | $\mu A$ |
| $I_{LR}$         | Reset Leakage Current                                                 | $V_{CC} = V_{CC\ max}$ ; $V_{ID} = 12.5\ V$                                     |        |     | 35             | $\mu A$ |
| $I_{LO}$         | Output Leakage Current                                                | $V_{OUT} = V_{SS}$ to $V_{CC}$ ; OE# = $V_{IH}$<br>$V_{CC} = V_{CC\ max}$       |        |     | $\pm 1.0$      | $\mu A$ |
| $I_{CC1}$        | $V_{CC}$ Active Read Current (Notes 1, 2, 3)                          | OE# = $V_{IH}$ , $V_{CC} = V_{CC\ max}$<br>(Note 1)                             | 5 MHz  | 20  | 30             | mA      |
|                  |                                                                       |                                                                                 | 10 MHz | 45  | 55             |         |
| $I_{CC2}$        | $V_{CC}$ Active Write Current (Notes 1, 3, 4)                         | OE# = $V_{IH}$ , WE# = $V_{IL}$                                                 |        | 15  | 25             | mA      |
| $I_{CC3}$        | $V_{CC}$ Standby Current (Note 3)                                     | CE#f1, CE#f2 (PDL129 only),<br>RESET#, WP/ACC# = $V_{IO} \pm 0.3\ V$            |        | 1   | 5              | $\mu A$ |
| $I_{CC4}$        | $V_{CC}$ Reset Current (Note 3)                                       | RESET# = $V_{SS} \pm 0.3\ V$ , CE# = $V_{SS}$                                   |        | 1   | 5              | $\mu A$ |
| $I_{CC5}$        | Automatic Sleep Mode (Notes 3, 5)                                     | $V_{IH} = V_{IO} \pm 0.3\ V$ ;<br>$V_{IL} = V_{SS} \pm 0.3\ V$ , CE# = $V_{SS}$ |        | 1   | 5              | $\mu A$ |
| $I_{CC6}$        | $V_{CC}$ Active Read-While-Program Current (Notes 1, 2, 3)            | OE# = $V_{IH}$                                                                  | Word   | 21  | 45             | mA      |
| $I_{CC7}$        | $V_{CC}$ Active Read-While-Erase Current (Notes 1, 2, 3)              | OE# = $V_{IH}$                                                                  | Word   | 21  | 45             | mA      |
| $I_{CC8}$        | $V_{CC}$ Active Program-While-Erase-Suspended Current (Notes 1, 3, 6) | OE# = $V_{IH}$                                                                  |        | 17  | 25             | mA      |
| $V_{IL}$         | Input Low Voltage                                                     | $V_{IO} = 2.7\text{--}3.6\ V$                                                   | -0.5   |     | 0.8            | V       |
| $V_{IH}$         | Input High Voltage                                                    | $V_{IO} = 2.7\text{--}3.6\ V$                                                   | 2.0    |     | $V_{CC} + 0.3$ | V       |
| $V_{HH}$         | Voltage for ACC Program Acceleration                                  | $V_{CC} = 3.0\ V \pm 10\%$                                                      | 8.5    |     | 9.5            | V       |
| $V_{ID}$         | Voltage for Autoselect and Temporary Sector Unprotect                 | $V_{CC} = 3.0\ V \pm 10\%$                                                      | 11.5   |     | 12.5           | V       |
| $V_{OL}$         | Output Low Voltage                                                    | $I_{OL} = 2.0\ mA$ , $V_{CC} = V_{CC\ min}$                                     |        |     | 0.4            | V       |
| $V_{OH}$         | Output High Voltage                                                   | $I_{OH} = -2.0\ mA$ , $V_{CC} = V_{CC\ min}$                                    | 2.4    |     |                | V       |
| $V_{LKO}$        | Low $V_{CC}$ Lock-Out Voltage (Note 6)                                |                                                                                 | 2.3    |     | 2.5            | V       |

#### Notes:

- Valid CE#f1/CE#f2 conditions (PDL129 only): (CE#f1 =  $V_{IL}$ , CE#f2 =  $V_{IH}$ ) or (CE#f1 =  $V_{IH}$ , CE#f2 =  $V_{IL}$ )
- The  $I_{CC}$  current listed is typically less than 5 mA/MHz, with OE# at  $V_{IH}$ .
- Maximum  $I_{CC}$  specifications are tested with  $V_{CC} = V_{CC\ max}$ .
- $I_{CC}$  active while Embedded Erase or Embedded Program is in progress.
- Automatic sleep mode enables the low power mode when addresses remain stable for  $t_{ACC} + 150\ ns$ . Typical sleep mode current is 1  $\mu A$ .
- Not 100% tested.

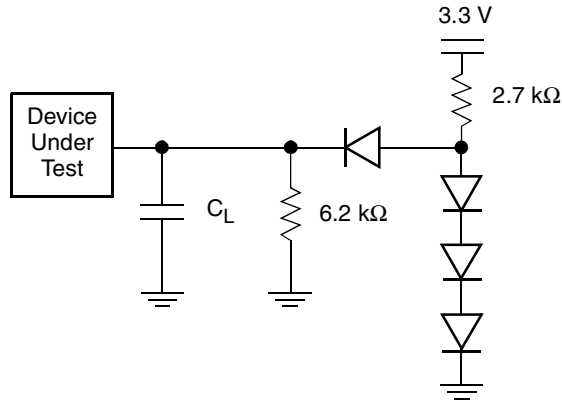
## pSRAM DC &amp; OPERATING CHARACTERISTICS

| Parameter Symbol | Parameter Description         | Test Conditions                                                                                                                           | Min              | Typ | Max                        | Unit    |
|------------------|-------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|------------------|-----|----------------------------|---------|
| $I_{LI}$         | Input Leakage Current         | $V_{IN} = V_{SS}$ to $V_{CC}$                                                                                                             | -1.0             |     | 1.0                        | $\mu A$ |
| $I_{LO}$         | Output Leakage Current        | CE#1ps = $V_{IH}$ , CE2ps = $V_{IL}$ or OE# = $V_{IH}$ or WE# = $V_{IL}$ , $V_{IO} = V_{SS}$ to $V_{CC}$                                  | -1.0             |     | 1.0                        | $\mu A$ |
| $I_{CC1S}$       | Operating Current             | Cycle time = Min., $I_{IO} = 0$ mA, 100% duty, CE#1ps = $V_{IL}$ , CE#2ps = $V_{IH}$ , $V_{IN} = V_{IL} = V_{IH}$ , $t_{RC} = \text{Min}$ |                  |     | 40                         | mA      |
| $I_{CC2S}$       | Page Access Operating Current | Cycle time = Min., $I_{IO} = 0$ mA, 100% duty, CE#1ps = $V_{IL}$ , CE#2ps = $V_{IH}$ , $V_{IN} = V_{IL} = V_{IH}$ , $t_{PC} = \text{Min}$ |                  |     | 25                         | mA      |
| $V_{OL}$         | Output Low Voltage            | $I_{OL} = 1.0$ mA                                                                                                                         |                  |     | 0.4                        | V       |
| $V_{OH}$         | Output High Voltage           | $I_{OH} = -0.5$ mA                                                                                                                        | 2                |     |                            | V       |
| $I_{SB}$         | Standby Current (CMOS)        | CE#f1 = $V_{CCS} - 0.2$ V,<br>CE2 = $V_{CCS} = 0.2$ V                                                                                     |                  |     | 70                         | $\mu A$ |
| $I_{DSB}$        | Deep Power-down Standby       | CE2 = 0.2 V                                                                                                                               |                  |     | 5                          | $\mu A$ |
| $V_{IL}$         | Input Low Voltage             |                                                                                                                                           | -0.3<br>(Note 1) |     | 0.4                        | V       |
| $V_{IH}$         | Input High Voltage            |                                                                                                                                           | 2.4              |     | $V_{CC} + 0.3$<br>(Note 2) | V       |

**Notes:**

1.  $V_{CC} - 1.0$  V for a 10 ns pulse width.
2.  $V_{CC} + 1.0$  V for a 10 ns pulse width.

## TEST CONDITIONS



**Note:** Diodes are IN3064 or equivalent

**Figure 11. Test Setup**

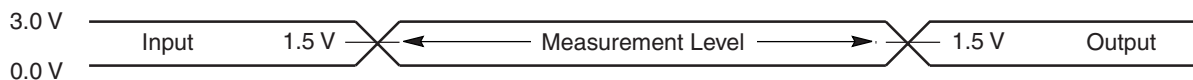
**Table 18. Test Specifications**

| Test Condition                                                | 66, 85     | Unit |
|---------------------------------------------------------------|------------|------|
| Output Load                                                   | 1 TTL gate |      |
| Output Load Capacitance, $C_L$<br>(including jig capacitance) | 30         | pF   |
| Input Rise and Fall Times                                     | 5          | ns   |
| Input Pulse Levels                                            | 0.0–3.0    | V    |
| Input timing measurement<br>reference levels                  | 1.5        | V    |
| Output timing measurement<br>reference levels                 | 1.5        | V    |

## KEY TO SWITCHING WAVEFORMS

| WAVEFORM | INPUTS                           | OUTPUTS                                      |
|----------|----------------------------------|----------------------------------------------|
|          | Steady                           |                                              |
|          | Changing from H to L             |                                              |
|          | Changing from L to H             |                                              |
|          | Don't Care, Any Change Permitted | Changing, State Unknown                      |
|          | Does Not Apply                   | Center Line is High Impedance State (High Z) |

KS000010-PAL



**Figure 12. Input Waveforms and Measurement Levels**

pSRAM AC CHARACTERISTICS

CE#1ps Timing

| Parameter |                  | Description         | Test Setup |     | All Speeds | Unit |
|-----------|------------------|---------------------|------------|-----|------------|------|
| JEDEC     | Std              |                     |            |     |            |      |
| —         | t <sub>CCR</sub> | CE#1ps Recover Time | —          | Min | 0          | ns   |

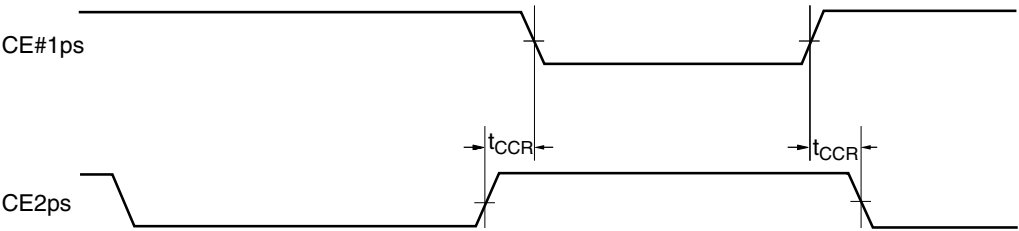


Figure 13. Timing Diagram for Alternating Between Pseudo SRAM and Flash

## FLASH AC CHARACTERISTICS

## Read-Only Operations – Am29PDL127H

| Parameter  |            | Description                                                                     | Test Setup               |     | Speed Options |    | Unit |
|------------|------------|---------------------------------------------------------------------------------|--------------------------|-----|---------------|----|------|
| JEDEC      | Std.       |                                                                                 |                          |     | 66            | 85 |      |
| $t_{AVAV}$ | $t_{RC}$   | Read Cycle Time (Note 1)                                                        |                          | Min | 65            | 85 | ns   |
| $t_{AVQV}$ | $t_{ACC}$  | Address to Output Delay                                                         | CE#f1, OE# = $V_{IL}$    | Max | 65            | 85 | ns   |
| $t_{ELQV}$ | $t_{CE}$   | Chip Enable to Output Delay                                                     | OE# = $V_{IL}$           | Max | 65            | 85 | ns   |
|            | $t_{PACC}$ | Page Access Time                                                                |                          | Max | 25            | 30 | ns   |
| $t_{GLQV}$ | $t_{OE}$   | Output Enable to Output Delay                                                   |                          | Max | 25            | 30 | ns   |
| $t_{EHQZ}$ | $t_{DF}$   | Chip Enable to Output High Z (Note 1, 3)                                        |                          | Max | 16            |    | ns   |
| $t_{GHQZ}$ | $t_{DF}$   | Output Enable to Output High Z (Notes 1, 3)                                     |                          | Max | 16            |    | ns   |
| $t_{AXQX}$ | $t_{OH}$   | Output Hold Time From Addresses, CE#f1 or OE#, Whichever Occurs First (Notes 3) |                          | Min | 5             |    | ns   |
|            | $t_{OEh}$  | Output Enable Hold Time (Note 1)                                                | Read                     | Min | 0             |    | ns   |
|            |            |                                                                                 | Toggle and Data# Polling | Min | 10            |    | ns   |

**Notes:**

1. Not 100% tested.
2. See Figure 11 and Table 18 for test specifications
3. Measurements performed by placing a 50 ohm termination on the data pin with a bias of  $V_{CC}/2$ . The time from OE# high to the data bus driven to  $V_{CC}/2$  is taken as  $t_{DF}$

## Read-Only Operations – Am29PDL129H

| Parameter  |            | Description                                                                              | Test Setup               |     | Speed Options |    | Unit |
|------------|------------|------------------------------------------------------------------------------------------|--------------------------|-----|---------------|----|------|
| JEDEC      | Std.       |                                                                                          |                          |     | 66            | 85 |      |
| $t_{AVAV}$ | $t_{RC}$   | Read Cycle Time (Note 1)                                                                 |                          | Min | 65            | 85 | ns   |
| $t_{AVQV}$ | $t_{ACC}$  | Address to Output Delay (Note 3)                                                         | CE#f1, OE# = $V_{IL}$    | Max | 65            | 85 | ns   |
| $t_{ELQV}$ | $t_{CE}$   | Chip Enable to Output Delay (Note 4)                                                     | OE# = $V_{IL}$           | Max | 65            | 85 | ns   |
|            | $t_{PACC}$ | Page Access Time                                                                         |                          | Max | 25            | 30 | ns   |
| $t_{GLQV}$ | $t_{OE}$   | Output Enable to Output Delay                                                            |                          | Max | 25            | 30 | ns   |
| $t_{EHQZ}$ | $t_{DF}$   | Chip Enable to Output High Z (Notes 1, 5, 6)                                             |                          | Max | 16            |    | ns   |
| $t_{GHQZ}$ | $t_{DF}$   | Output Enable to Output High Z (Notes 1, 5)                                              |                          | Max | 16            |    | ns   |
| $t_{AXQX}$ | $t_{OH}$   | Output Hold Time From Addresses, CE#f1/CE#f2 or OE#, Whichever Occurs First (Notes 5, 6) |                          | Min | 5             |    | ns   |
|            | $t_{OEh}$  | Output Enable Hold Time (Note 1)                                                         | Read                     | Min | 0             |    | ns   |
|            |            |                                                                                          | Toggle and Data# Polling | Min | 10            |    | ns   |

**Notes:**

1. Not 100% tested.
2. See Figure 11 and Table 18 for test specifications
3. Valid CE#f1/CE#f2 conditions: (CE#f1 =  $V_{IL}$ , CE#f2 =  $V_{IH}$ ) or (CE#f1 =  $V_{IH}$ , CE#f2 =  $V_{IL}$ ).
4. Valid CE#f1/CE#f2 transitions: (CE#f1 = CE#f2 =  $V_{IH}$ ) to (CE#f1 =  $V_{IL}$ , CE#f2 =  $V_{IH}$ ) or (CE#f1 =  $V_{IH}$ , CE#f2 =  $V_{IL}$ ).
5. Measurements performed by placing a 50 ohm termination on the data pin with a bias of  $V_{CC}/2$ . The time from OE# high to the data bus driven to  $V_{CC}/2$  is taken as  $t_{DF}$
6. Valid CE#f1/CE#f2 transitions: (CE#f1 =  $V_{IL}$ , CE#f2 =  $V_{IH}$ ) or (CE#f1 =  $V_{IH}$ , CE#f2 =  $V_{IL}$ ) to (CE#f1 = CE#f2 =  $V_{IH}$ ).

## FLASH AC CHARACTERISTICS

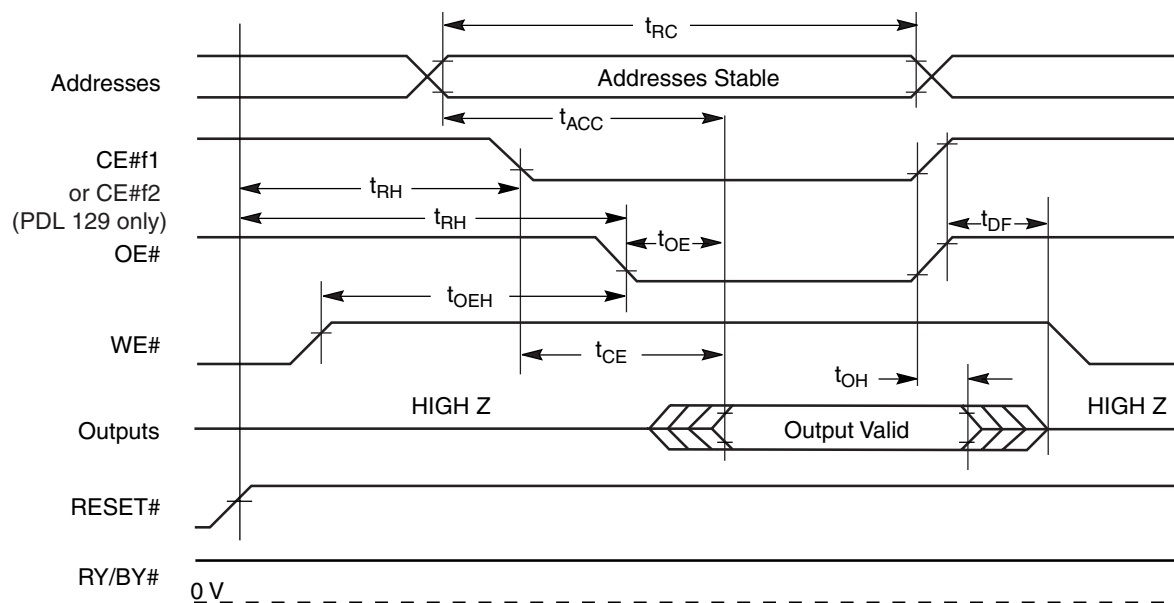


Figure 14. Read Operation Timings

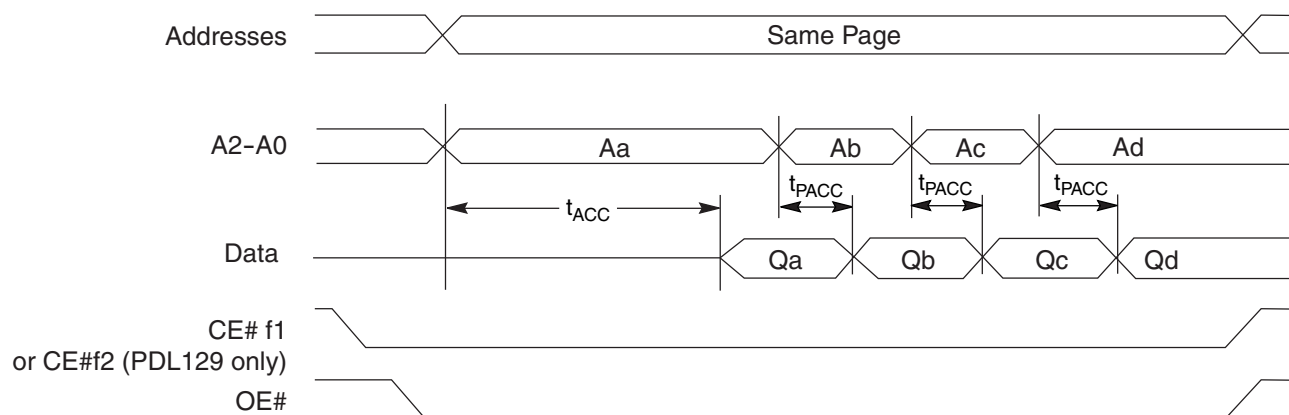


Figure 15. Page Read Operation Timings

**Notes:** During CE#f1 transitions, CE#f2=  $V_{IH}$ ; During CE#f2 transitions, CE#f1=  $V_{IH}$

## FLASH AC CHARACTERISTICS

### Hardware Reset (RESET#)

| Parameter |                    | Description                                                             |     | All Speed Options | Unit          |
|-----------|--------------------|-------------------------------------------------------------------------|-----|-------------------|---------------|
| JEDEC     | Std                |                                                                         |     |                   |               |
|           | $t_{\text{Ready}}$ | RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)     | Max | 20                | $\mu\text{s}$ |
|           | $t_{\text{Ready}}$ | RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note) | Max | 500               | ns            |
|           | $t_{\text{RP}}$    | RESET# Pulse Width                                                      | Min | 500               | ns            |
|           | $t_{\text{RH}}$    | Reset High Time Before Read (See Note)                                  | Min | 50                | ns            |
|           | $t_{\text{RPD}}$   | RESET# Low to Standby Mode                                              | Min | 20                | $\mu\text{s}$ |
|           | $t_{\text{RB}}$    | RY/BY# Recovery Time                                                    | Min | 0                 | ns            |

**Note:** Not 100% tested.

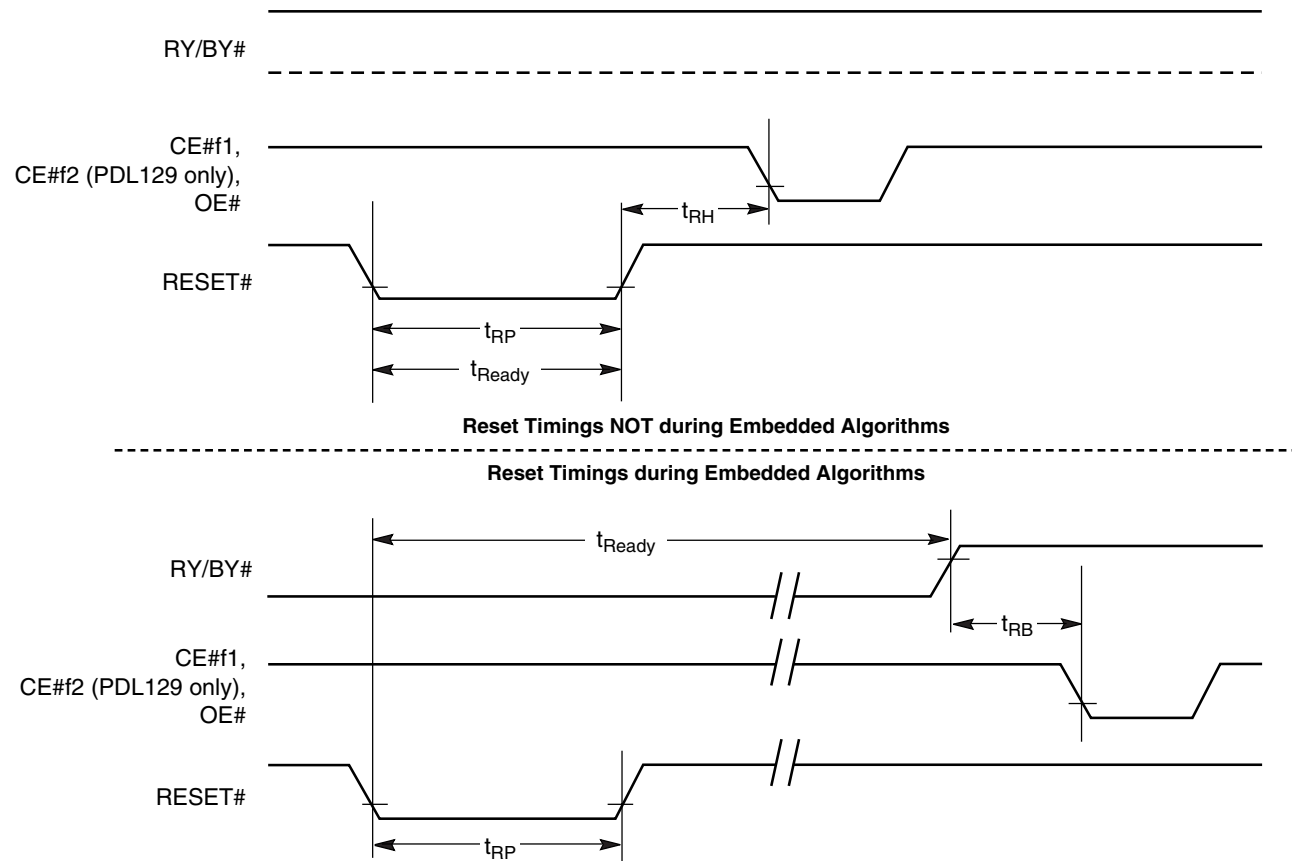


Figure 16. Reset Timings

## FLASH AC CHARACTERISTICS

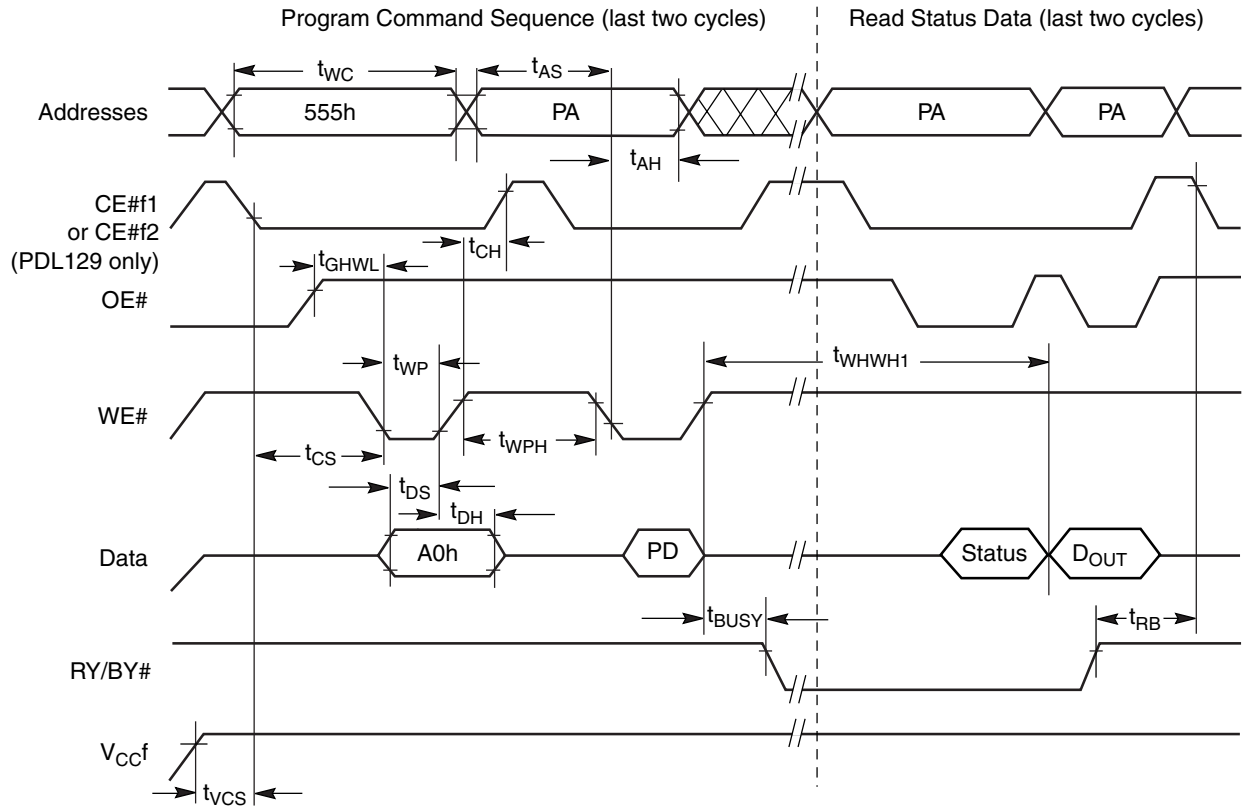
## Erase and Program Operations

| Parameter   |             | Description                                                        |      | Speed |     | Unit    |
|-------------|-------------|--------------------------------------------------------------------|------|-------|-----|---------|
| JEDEC       | Std         |                                                                    |      | 66    | 85  |         |
| $t_{AVAV}$  | $t_{WC}$    | Write Cycle Time (Note 1)                                          | Min  | 65    | 85  | ns      |
| $t_{AVWL}$  | $t_{AS}$    | Address Setup Time                                                 | Min  | 05    |     | ns      |
|             | $t_{ASO}$   | Address Setup Time to OE# low during toggle bit polling            | Min  | 15    |     | ns      |
| $t_{WLAX}$  | $t_{AH}$    | Address Hold Time                                                  | Min  | 35    |     | ns      |
|             | $t_{AHT}$   | Address Hold Time From CE#f1 or OE# high during toggle bit polling | Min  | 0     |     | ns      |
| $t_{DVWH}$  | $t_{DS}$    | Data Setup Time                                                    | Min  | 30    |     | ns      |
| $t_{WHDX}$  | $t_{DH}$    | Data Hold Time                                                     | Min  | 0     |     | ns      |
|             | $t_{OEPH}$  | Output Enable High during toggle bit polling                       | Min  | 10    |     | ns      |
| $t_{GHWL}$  | $t_{GHWL}$  | Read Recovery Time Before Write (OE# High to WE# Low)              | Min  | 0     |     | ns      |
| $t_{WLEL}$  | $t_{WS}$    | WE# Setup Time (CE#f1 to WE#)                                      | Min  | 0     |     | ns      |
| $t_{ELWL}$  | $t_{CS}$    | CE#f1 Setup Time                                                   | Min  | 0     |     | ns      |
| $t_{EHWH}$  | $t_{WH}$    | WE# Hold Time (CE#f1 to WE#)                                       | Min  | 0     |     | ns      |
| $t_{WHEH}$  | $t_{CH}$    | CE#f1 Hold Time                                                    | Min  | 0     |     | ns      |
| $t_{WLWH}$  | $t_{WP}$    | Write Pulse Width                                                  | Min  | 40    |     | ns      |
| $t_{WHDL}$  | $t_{WPH}$   | Write Pulse Width High                                             | Min  | 25    |     | ns      |
|             | $t_{SR/W}$  | Latency Between Read and Write Operations                          | Min  | 0     |     | ns      |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Programming Operation (Note 2)                                     | Word | Typ   | 6   | $\mu$ s |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Accelerated Programming Operation, Word or Byte (Note 2)           |      | Typ   | 4   | $\mu$ s |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation (Note 2)                                    |      | Typ   | 0.5 | sec     |
|             | $t_{VCS}$   | $V_{CC}$ Setup Time (Note 1)                                       | Min  | 50    |     | $\mu$ s |
|             | $t_{RB}$    | Write Recovery Time from RY/BY#                                    | Min  | 0     |     | ns      |
|             | $t_{BUSY}$  | Program/Erase Valid to RY/BY# Delay                                | Max  | 90    |     | ns      |

**Notes:**

1. Not 100% tested.
2. See the "Flash Erase And Programming Performance" section for more information.

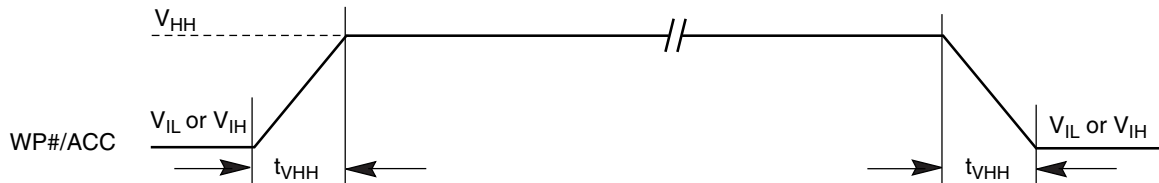
## FLASH AC CHARACTERISTICS



**Notes:**

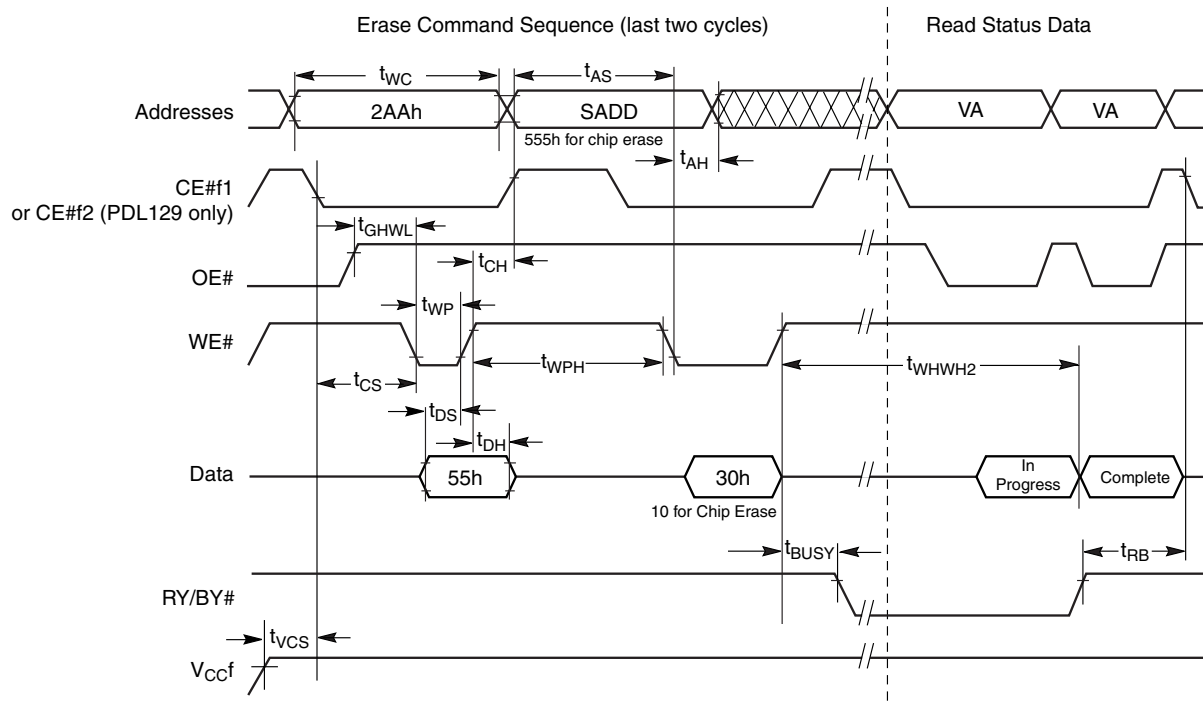
1. PA = program address, PD = program data,  $D_{OUT}$  is the true data at the program address.
2. Illustration shows device in word mode.
3. For PDL129 during CE#f1 transitions the other CE#f1 pin =  $V_{IH}$ .

**Figure 17. Program Operation Timings**



**Figure 18. Accelerated Program Timing Diagram**

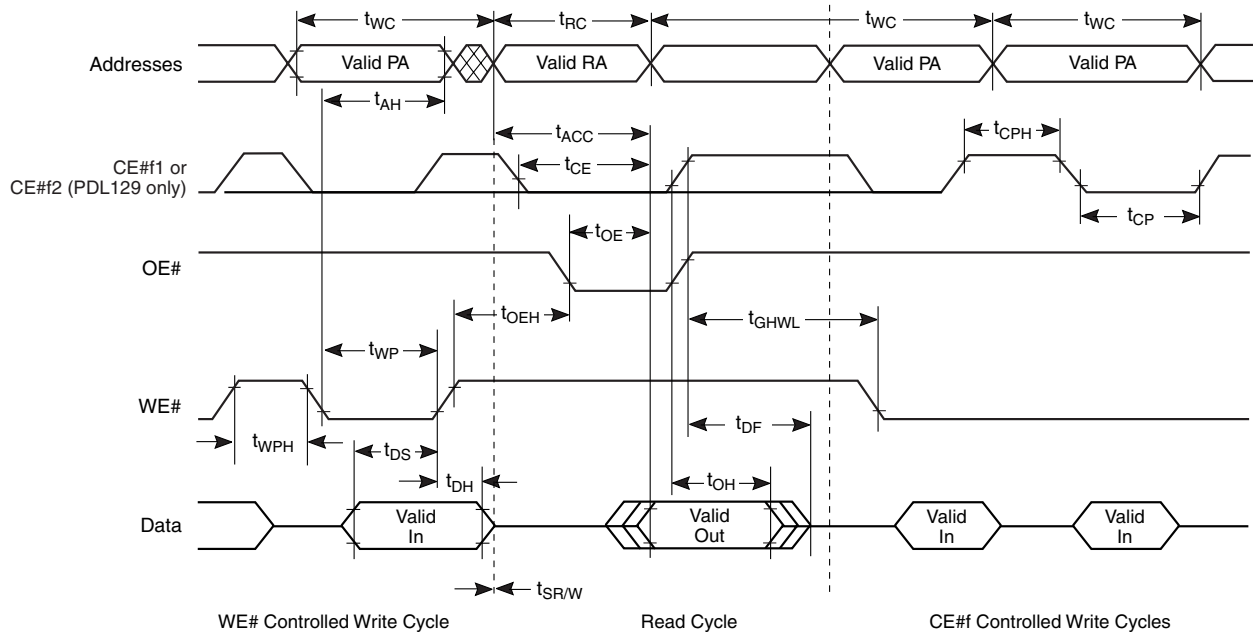
## FLASH AC CHARACTERISTICS

**Notes:**

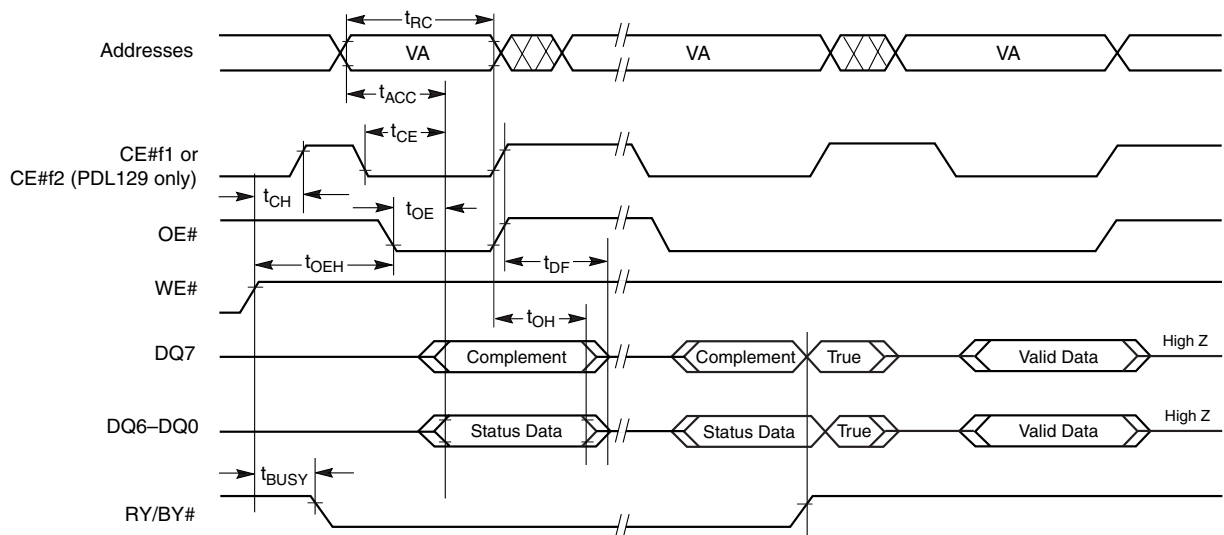
1. SADD = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Flash Write Operation Status").
2. For PDL129 during CE#f1 transitions the other CE#f1 pin = V<sub>IH</sub>.

**Figure 19. Chip/Sector Erase Operation Timings**

# FLASH AC CHARACTERISTICS



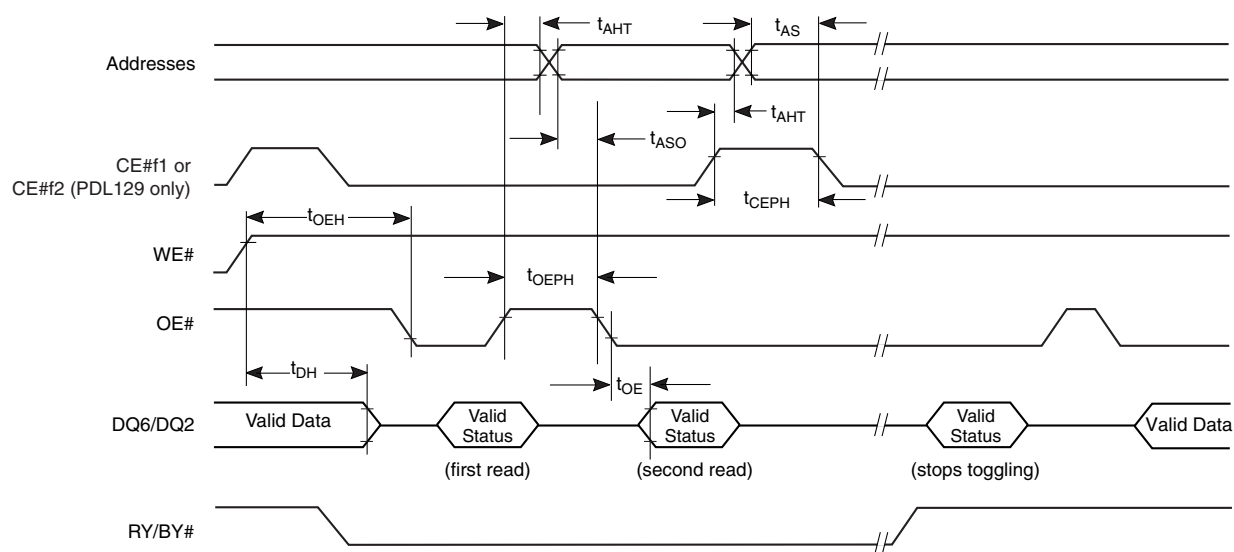
**Figure 20. Back-to-back Read/Write Cycle Timings**



**Note:** VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

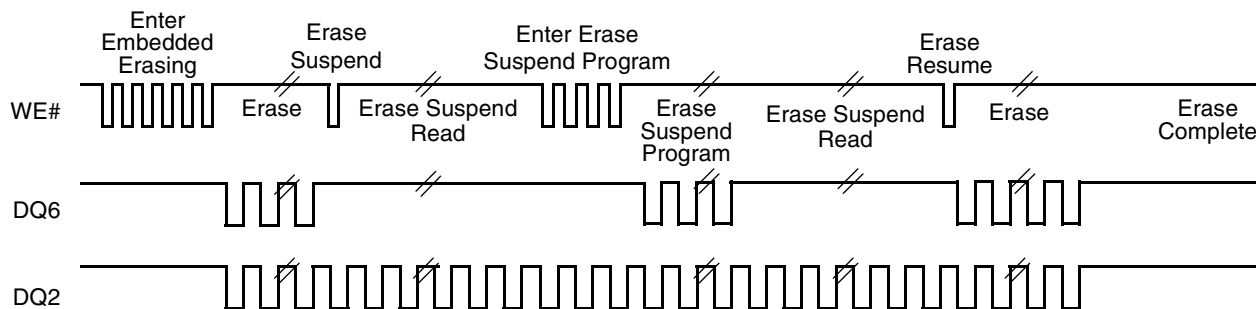
**Figure 21. Data# Polling Timings (During Embedded Algorithms)**

## FLASH AC CHARACTERISTICS



**Note:** VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

**Figure 22. Toggle Bit Timings (During Embedded Algorithms)**



**Note:** DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE#f1 to toggle DQ2 and DQ6.

**Figure 23. DQ2 vs. DQ6**

## FLASH AC CHARACTERISTICS

### Temporary Sector Unprotect

| Parameter |            | Description                                                      |     | All Speed Options | Unit    |
|-----------|------------|------------------------------------------------------------------|-----|-------------------|---------|
| JEDEC     | Std        |                                                                  |     |                   |         |
|           | $t_{VIDR}$ | $V_{ID}$ Rise and Fall Time (See Note)                           | Min | 500               | ns      |
|           | $t_{VHH}$  | $V_{HH}$ Rise and Fall Time (See Note)                           | Min | 250               | ns      |
|           | $t_{RSP}$  | RESET# Setup Time for Temporary Sector Unprotect                 | Min | 4                 | $\mu$ s |
|           | $t_{RRB}$  | RESET# Hold Time from RY/BY# High for Temporary Sector Unprotect | Min | 4                 | $\mu$ s |

**Note:** Not 100% tested.

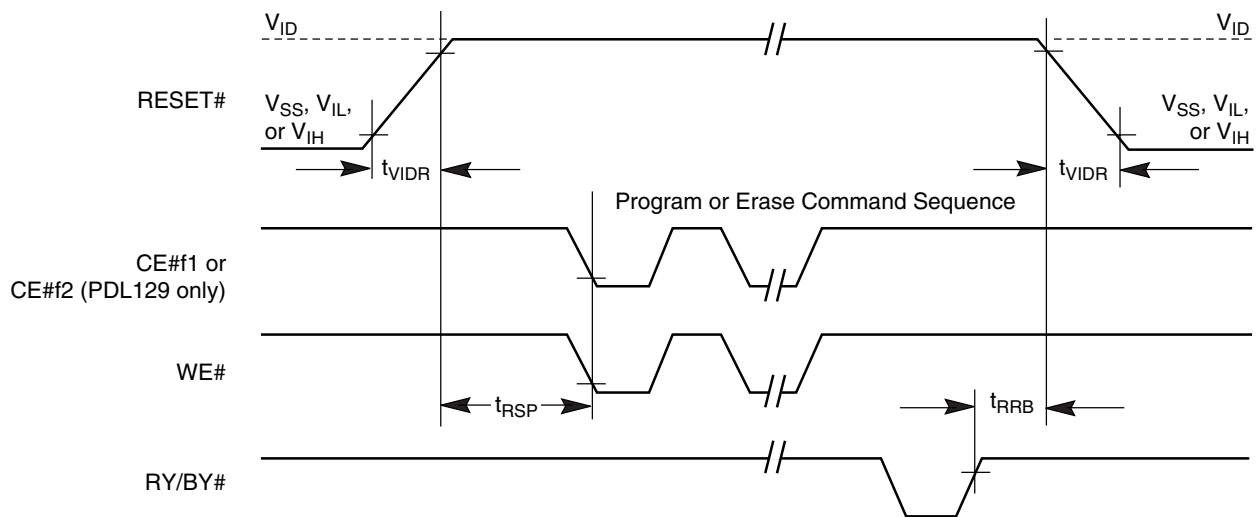
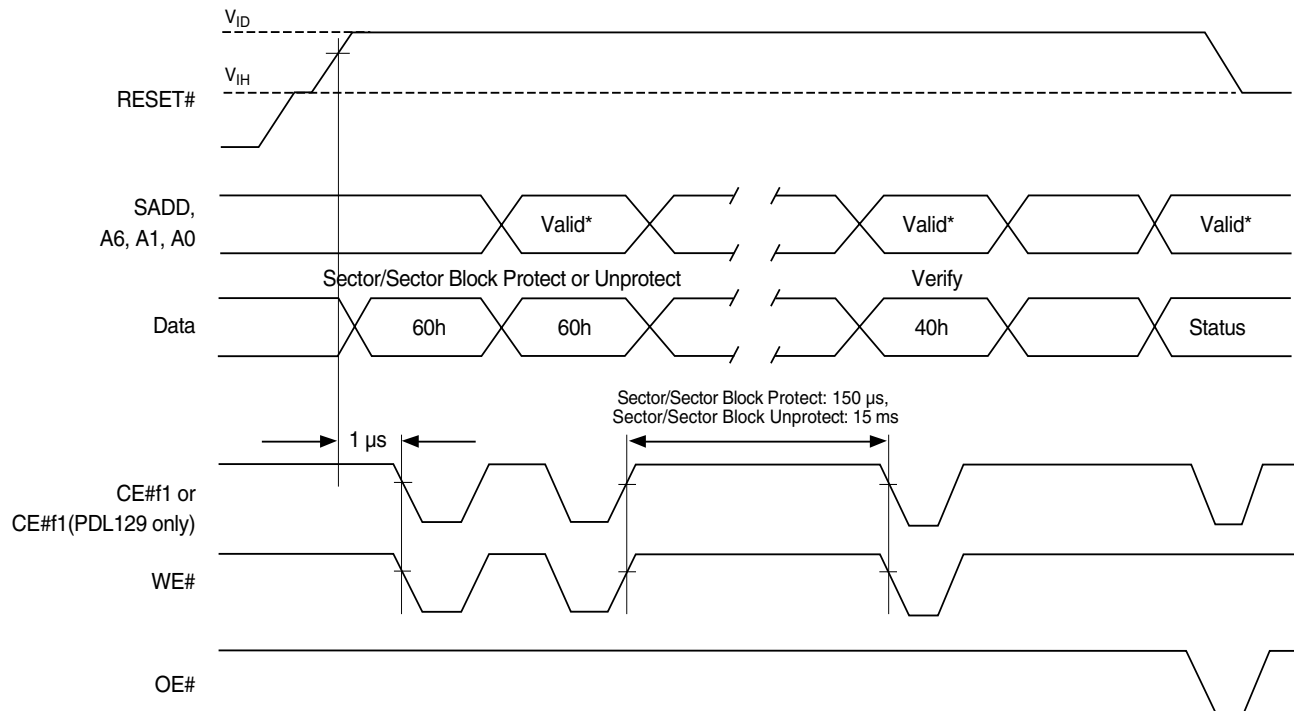


Figure 24. Temporary Sector Unprotect Timing Diagram

## FLASH AC CHARACTERISTICS



1. For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0, SADD = Sector Address.
2. For PDL129 during CE#f1 transitions the other CE#f1 pin = V<sub>IH</sub>.

**Figure 25. Sector/Block Protect and Unprotect Timing Diagram**

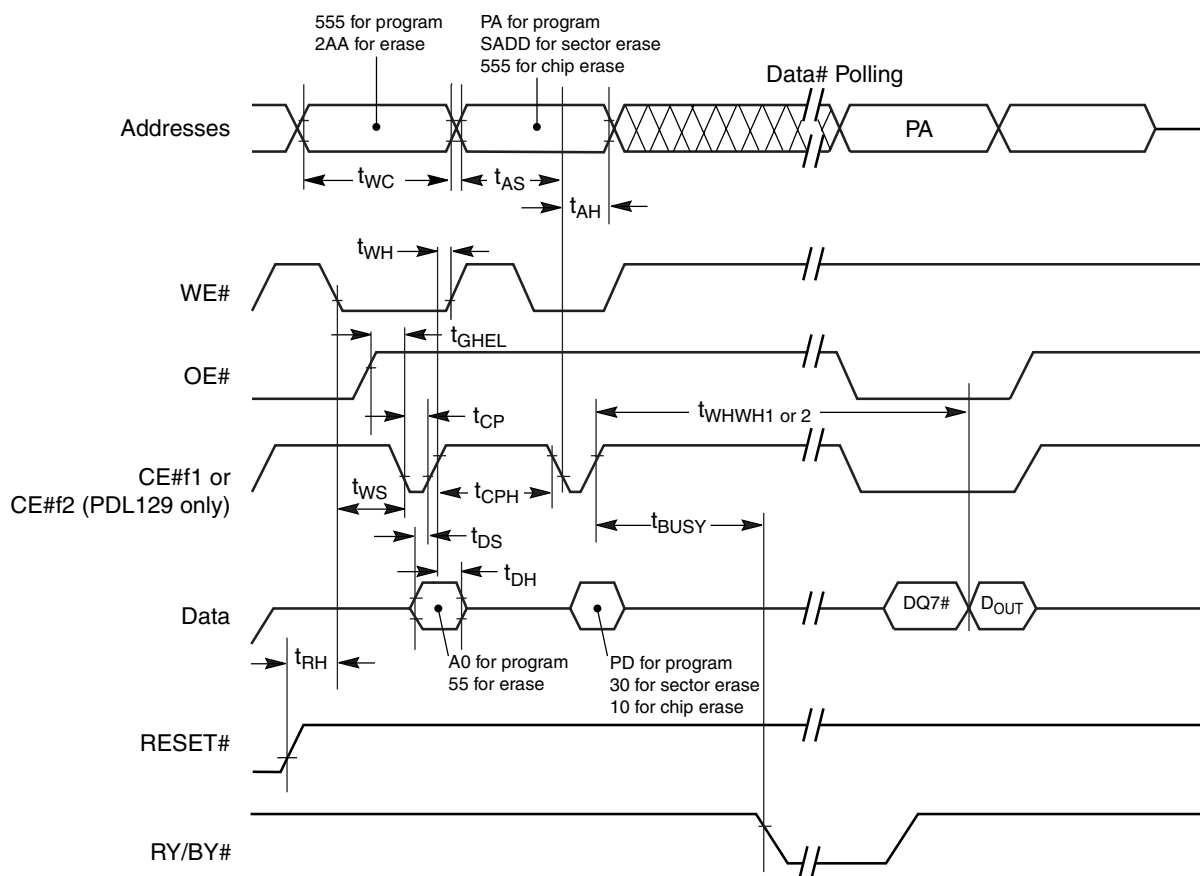
**FLASH AC CHARACTERISTICS****Alternate CE#f1 Controlled Erase and Program Operations**

| Parameter   |             | Description                                                 |     | Speed |    | Unit    |
|-------------|-------------|-------------------------------------------------------------|-----|-------|----|---------|
| JEDEC       | Std.        |                                                             |     | 66    | 85 |         |
| $t_{AVAV}$  | $t_{WC}$    | Write Cycle Time (Note 1)                                   | Min | 65    | 85 | ns      |
| $t_{AVWL}$  | $t_{AS}$    | Address Setup Time                                          | Min | 0     |    | ns      |
| $t_{ELAX}$  | $t_{AH}$    | Address Hold Time                                           | Min | 35    |    | ns      |
| $t_{DVEH}$  | $t_{DS}$    | Data Setup Time                                             | Min | 30    |    | ns      |
| $t_{EHDX}$  | $t_{DH}$    | Data Hold Time                                              | Min | 0     |    | ns      |
| $t_{GHEL}$  | $t_{GHEL}$  | Read Recovery Time Before Write<br>(OE# High to WE# Low)    | Min | 0     |    | ns      |
| $t_{WLEL}$  | $t_{WS}$    | WE# Setup Time                                              | Min | 0     |    | ns      |
| $t_{EHWH}$  | $t_{WH}$    | WE# Hold Time                                               | Min | 0     |    | ns      |
| $t_{ELEH}$  | $t_{CP}$    | CE#f1 Pulse Width                                           | Min | 40    |    | ns      |
| $t_{EHEL}$  | $t_{CPH}$   | CE#f1 Pulse Width High                                      | Min | 25    |    | ns      |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Word Programming Operation<br>(Note 2)                      | Typ | 6     |    | $\mu$ s |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Accelerated Programming Operation,<br>Word or Byte (Note 2) | Typ | 4     |    | $\mu$ s |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation (Note 2)                             | Typ | 0.4   |    | sec     |

**Notes:**

1. Not 100% tested.
2. See the "Flash Erase And Programming Performance" section for more information.

## FLASH AC CHARACTERISTICS

**Notes:**

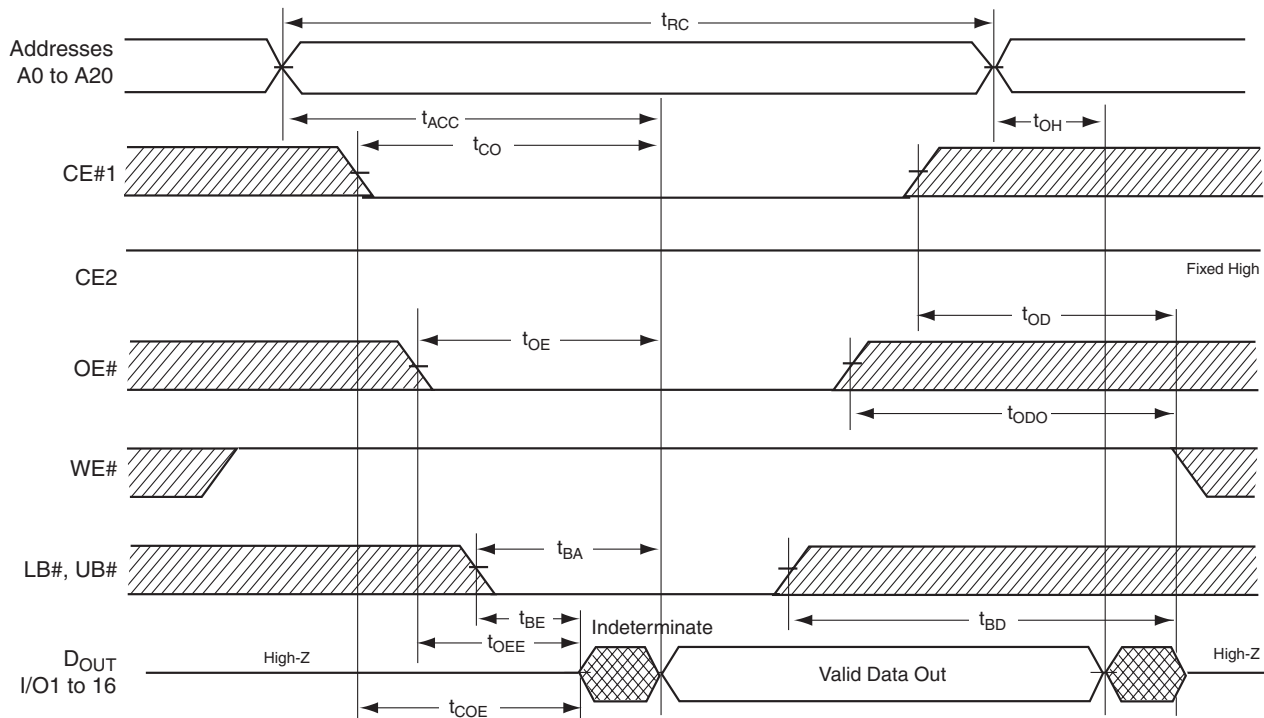
1. Figure indicates last two bus cycles of a program or erase operation.
2. PA = program address, SADD = sector address, PD = program data.
3.  $DQ7\#$  is the complement of the data written to the device.  $D_{OUT}$  is the data written to the device.

**Figure 26. Flash Alternate CE#f1 Controlled Write (Erase/Program) Operation Timings**

# pSRAM AC CHARACTERISTICS

## Read Cycle

| Parameter Symbol | Description                             |     | Speed |    | Unit |
|------------------|-----------------------------------------|-----|-------|----|------|
|                  |                                         |     | 66    | 85 |      |
| $t_{RC}$         | Read Cycle Time                         | Min | 70    | 85 | ns   |
| $t_{ACC}$        | Address Access Time                     | Max | 70    | 85 | ns   |
| $t_{CO}$         | Chip Enable Access Time                 | Max | 70    | 85 | ns   |
| $t_{OE}$         | Output Enable Access Time               | Max | 25    |    | ns   |
| $t_{BA}$         | Data Byte Control Access Time           | Max | 25    |    | ns   |
| $t_{COE}$        | Chip Enable Low to Output Active        | Min | 10    |    | ns   |
| $t_{OEE}$        | Output Enable Low to Output Active      | Min | 0     |    | ns   |
| $t_{BE}$         | Data Byte Control High to Output Active | Min | 0     |    | ns   |
| $t_{OD}$         | Chip Enable High to Output High-Z       | Max | 20    |    | ns   |
| $t_{ODO}$        | Output Enable High to Output High-Z     | Max | 20    |    | ns   |
| $t_{BD}$         | Data Byte Control High to Output High-Z | Max | 20    |    | ns   |
| $t_{OH}$         | Output Data Hold from Address Change    | Min | 10    |    | ns   |
| $t_{PM}$         | Page Mode Time                          | Min | 70    |    | ns   |
| $t_{PC}$         | Page Mode Cycle Time                    | Min | 30    |    | ns   |
| $t_{AA}$         | Page Mode Address Access Time           | Max | 30    |    | ns   |
| $t_{OH}$         | Page Output Data Hold Time              | Min | 10    |    | ns   |



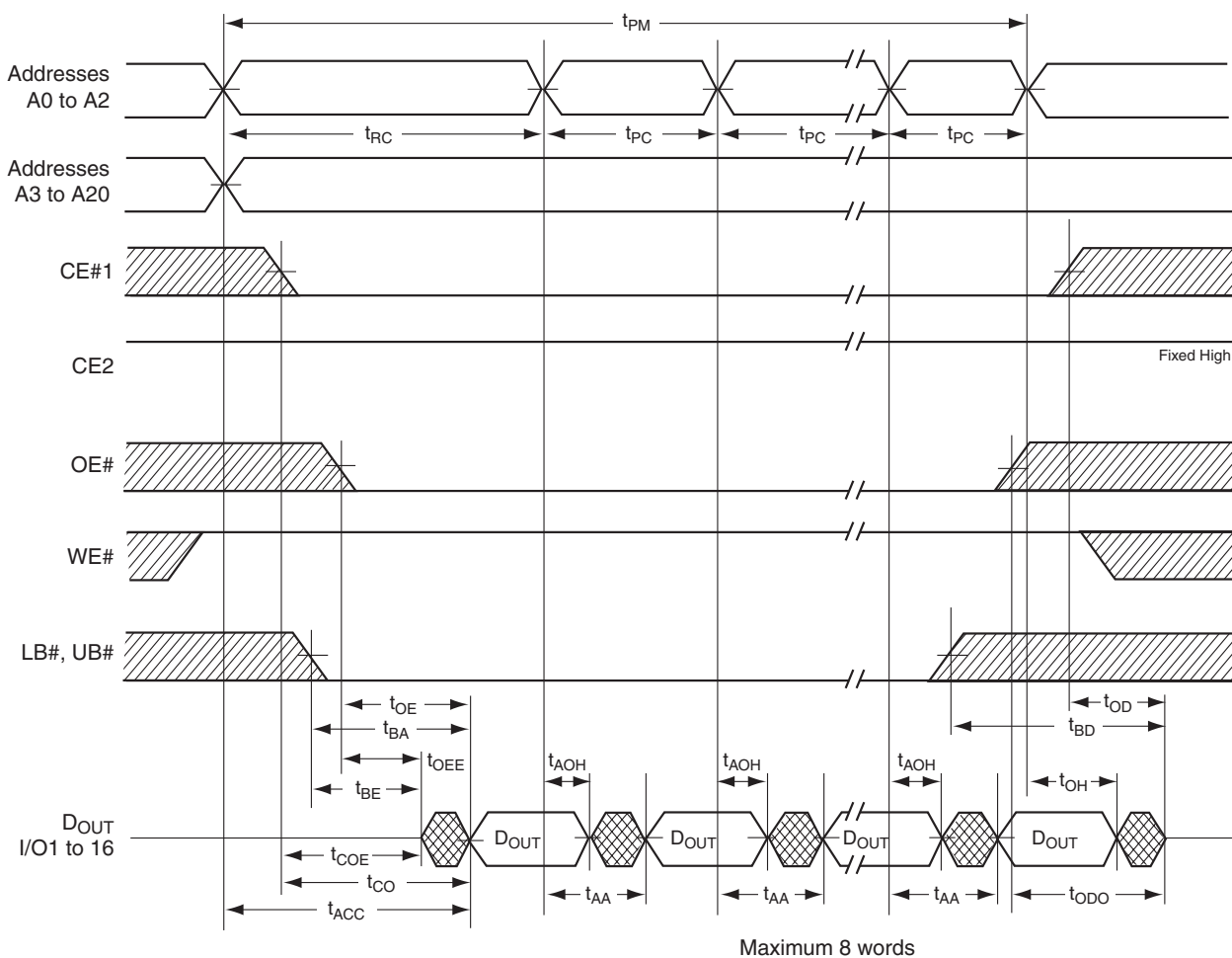
### Notes:

- $t_{OD}$ ,  $t_{ODO}$ ,  $t_{BD}$  and  $t_{ODW}$  are defined as the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
- If  $CE\#$ ,  $LB\#$ , or  $UB\#$  goes low at the same time or before  $WE\#$  goes high, the outputs will remain at high impedance.
- If  $CE\#$ ,  $LB\#$ , or  $UB\#$  goes low at the same time or after  $WE\#$  goes low, the outputs will remain at high impedance.

Figure 27. Pseudo SRAM Read Cycle

# pSRAM AC CHARACTERISTICS

## Read Cycle



**Figure 28. Page Read Timing**

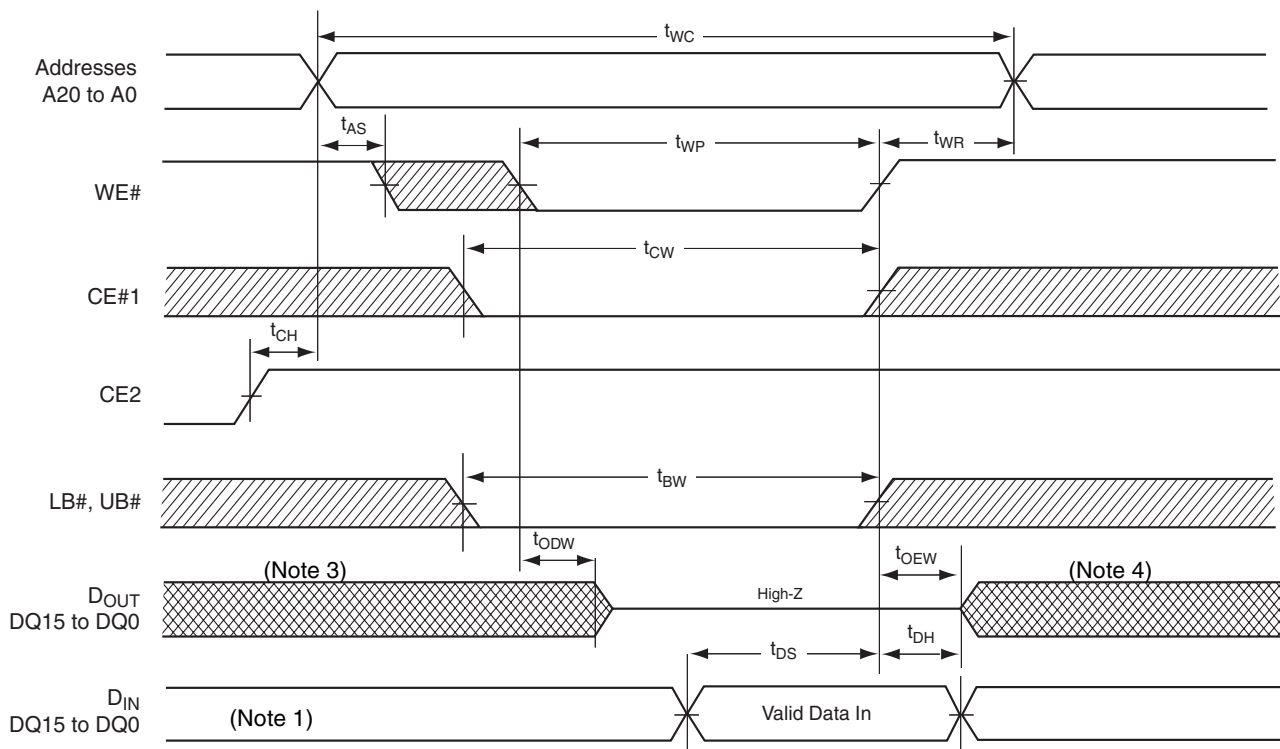
### Notes:

1.  $t_{OD}$ ,  $t_{ODD}$ ,  $t_{BD}$  and  $t_{ODW}$  are defined as the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
2. If CE#f1, LB#, or UB# goes low at the same time or before WE# goes high, the outputs will remain at high impedance.
3. If CE#f1, LB#, or UB# goes low at the same time or after WE# goes low, the outputs will remain at high impedance.

## pSRAM AC CHARACTERISTICS

### Write Cycle

| Parameter Symbol | Description                        |     | Speed |    | Unit    |
|------------------|------------------------------------|-----|-------|----|---------|
|                  |                                    |     | 66    | 85 |         |
| $t_{WC}$         | Write Cycle Time                   | Min | 70    | 85 | ns      |
| $t_{WP}$         | Write Pulse Time                   | Min | 50    | 60 | ns      |
| $t_{CW}$         | Chip Enable to End of Write        | Min | 60    | 70 | ns      |
| $t_{BW}$         | Data Byte Control to End of Write  | Min | 60    | 70 | ns      |
| $t_{AW}$         | Address Valid to End of Write      | Min | 60    | 70 | ns      |
| $t_{AS}$         | Address Setup Time                 | Min | 0     |    | ns      |
| $t_{WR}$         | Write Recovery Time                | Min | 0     |    | ns      |
| $t_{ODW}$        | WE# Low to Write to Output High-Z  | Max | 20    |    | ns      |
| $t_{OEW}$        | WE# High to Write to Output Active | Min | 0     |    | ns      |
| $t_{DS}$         | Data Set-up Time                   | Min | 30    |    |         |
| $t_{DH}$         | Data Hold from Write Time          | Min | 0     |    | ns      |
| $t_{CH}$         | CE2 Hold Time                      | Min | 300   |    | $\mu$ s |
| $t_{CEH}$        | Chip Enable High Pulse Width       | Min | 10    |    | ns      |
| $t_{WEH}$        | Write Enable High Pulse Width      | Min | 6     |    | ns      |

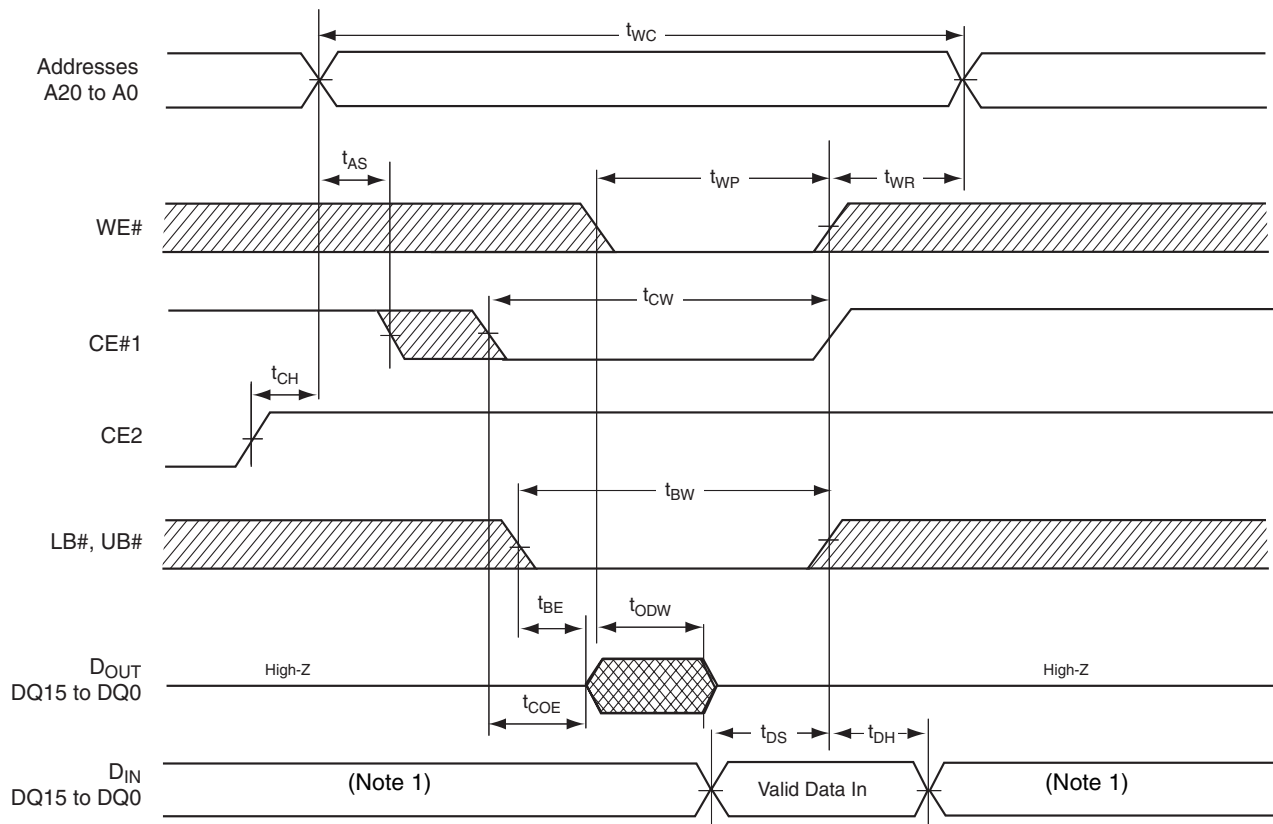


#### Notes:

1. If the device is using the I/Os to output data, input signals of reverse polarity must not be applied.
2. If OE# is high during the write cycle, the outputs will remain at high impedance.
3. If CE#1ps, LB# or UB# goes low at the same time or after WE# goes low, the outputs will remain at high impedance.
4. If CE#1ps, LB# or UB# goes high at the same time or before WE# goes high, the outputs will remain at high impedance.

Figure 29. Pseudo SRAM Write Cycle—WE# Control

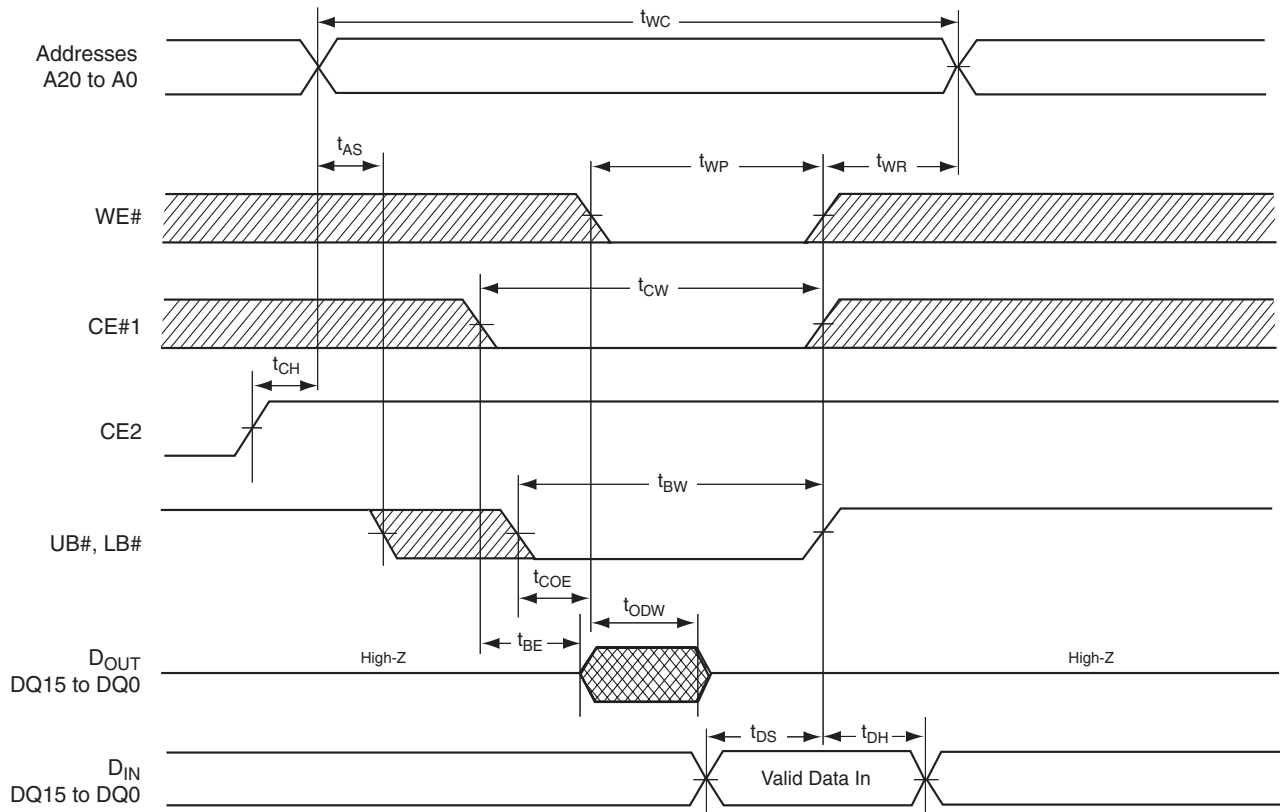
## pSRAM AC CHARACTERISTICS

**Notes:**

1. If the device is using the I/Os to output data, input signals of reverse polarity must not be applied.
2. If OE# is high during the write cycle, the outputs will remain at high impedance.

**Figure 30. Pseudo SRAM Write Cycle—CE1#s Control**

# pSRAM AC CHARACTERISTICS



## Notes:

1. If the device is using the I/Os to output data, input signals of reverse polarity must not be applied.
2. If OE# is high during the write cycle, the outputs will remain at high impedance.

**Figure 31. Pseudo SRAM Write Cycle—  
UB#s and LB#s Control**

## ERASE AND PROGRAMMING PERFORMANCE

| Parameter                     | Typ (Note 1) | Max (Note 2) | Unit    | Comments                                           |
|-------------------------------|--------------|--------------|---------|----------------------------------------------------|
| Sector Erase Time             | 0.4          | 5            | sec     | Excludes 00h programming prior to erasure (Note 4) |
| Chip Erase Time               | 108          |              | sec     |                                                    |
| Word Program Time             | 7            | 210          | $\mu$ s | Excludes system level overhead (Note 5)            |
| Accelerated Word Program Time | 4            | 120          | $\mu$ s |                                                    |
| Chip Program Time (Note 3)    | 50           | 200          | sec     |                                                    |

**Notes:**

1. Typical program and erase times assume the following conditions: 25°C, 3.0 V  $V_{CC}$ , 1,000,000 cycles. Additionally, programming typicals assume checkerboard pattern. All values are subject to change.
2. Under worst case conditions of 90°C,  $V_{CC} = 2.7$  V, 1,000,000 cycles. All values are subject to change.
3. The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.
4. In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.
5. System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Tables Table 15 for further information on command definitions.
6. The device has a minimum erase and program cycle endurance of 1,000,000 cycles.

## LATCHUP CHARACTERISTICS

| Description                                                                                        | Min     | Max              |
|----------------------------------------------------------------------------------------------------|---------|------------------|
| Input voltage with respect to $V_{SS}$ on all pins except I/O pins (including A9, OE#, and RESET#) | -1.0 V  | 12.5 V           |
| Input voltage with respect to $V_{SS}$ on all I/O pins                                             | -1.0 V  | $V_{CC} + 1.0$ V |
| $V_{CC}$ Current                                                                                   | -100 mA | +100 mA          |

**Note:** Includes all pins except  $V_{CC}$ . Test conditions:  $V_{CC} = 3.0$  V, one pin at a time.

## PACKAGE PIN CAPACITANCE

| Parameter Symbol | Parameter Description   | Test Setup    | Typ | Max | Unit |
|------------------|-------------------------|---------------|-----|-----|------|
| $C_{IN}$         | Input Capacitance       | $V_{IN} = 0$  | 11  | 14  | pF   |
| $C_{OUT}$        | Output Capacitance      | $V_{OUT} = 0$ | 12  | 16  | pF   |
| $C_{IN2}$        | Control Pin Capacitance | $V_{IN} = 0$  | 14  | 16  | pF   |
| $C_{IN3}$        | WP#/ACC Pin Capacitance | $V_{IN} = 0$  | 17  | 20  | pF   |

**Notes:**

1. Sampled, not 100% tested.
2. Test conditions  $T_A = 25^\circ\text{C}$ ,  $f = 1.0$  MHz.

## FLASH DATA RETENTION

| Parameter Description               | Test Conditions | Min | Unit  |
|-------------------------------------|-----------------|-----|-------|
| Minimum Pattern Data Retention Time | 150°C           | 10  | Years |
|                                     | 125°C           | 20  | Years |

## pSRAM DATA RETENTION

| Parameter Symbol | Parameter Description       | Test Setup                                                              | Min | Typ             | Max | Unit          |
|------------------|-----------------------------|-------------------------------------------------------------------------|-----|-----------------|-----|---------------|
| $V_{DR}$         | $V_{CC}$ for Data Retention | $CS1\#ps \geq V_{CC} - 0.2\text{ V}$ (Note 1)                           | 2.7 |                 | 3.3 | V             |
| $I_{DR}$         | Data Retention Current      | $V_{CC} = 3.0\text{ V}$ , $CE1\#ps \geq V_{CC} - 0.2\text{ V}$ (Note 1) |     | 1.0<br>(Note 2) | 70  | $\mu\text{A}$ |
| $t_{CS}$         | CE2 Setup Time              |                                                                         | 0   |                 |     | ns            |
| $t_{CH}$         | CE2 Hold Time               |                                                                         | 300 |                 |     | $\mu\text{s}$ |
| $t_{DPD}$        | CE2 Pulse Width             |                                                                         | 10  |                 |     | ms            |
| $t_{CHC}$        | CE2 Hold from CE#1          |                                                                         | 0   |                 |     | ns            |
| $t_{CHP}$        | CE2 Hold from Power On      |                                                                         | 30  |                 |     | $\mu\text{s}$ |

### Notes:

1.  $CE1\#ps \geq V_{CC} - 0.2\text{ V}$ ,  $CE2ps \geq V_{CC} - 0.2\text{ V}$  (CE1#s controlled) or  $CE2ps \leq 0.2\text{ V}$  (CE2ps controlled).
2. Typical values are not 100% tested.

## pSRAM POWER ON AND DEEP POWER DOWN

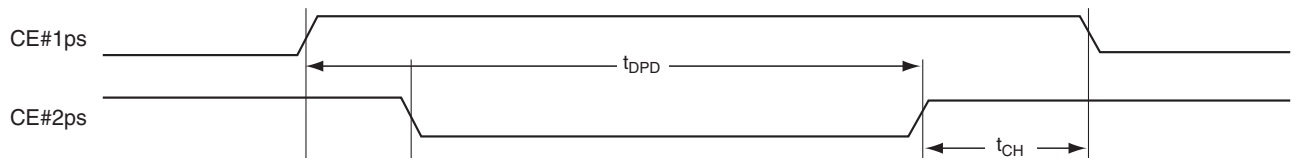


Figure 32. Deep Power-down Timing

**Note:** Data cannot be retained during deep power-down standby mode.

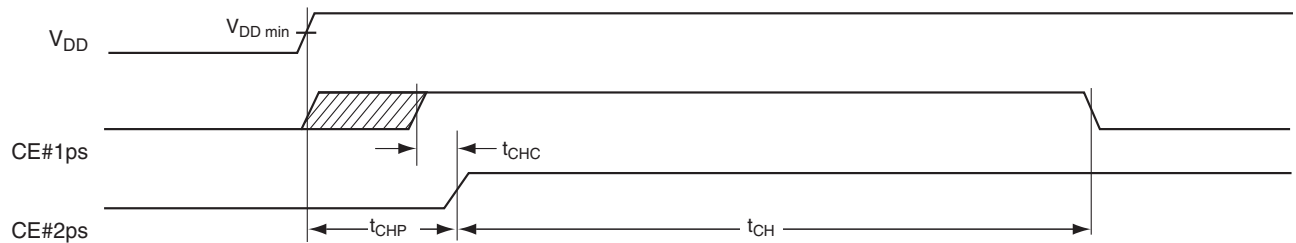


Figure 33. Power-on Timing

## pSRAM ADDRESS SKEW

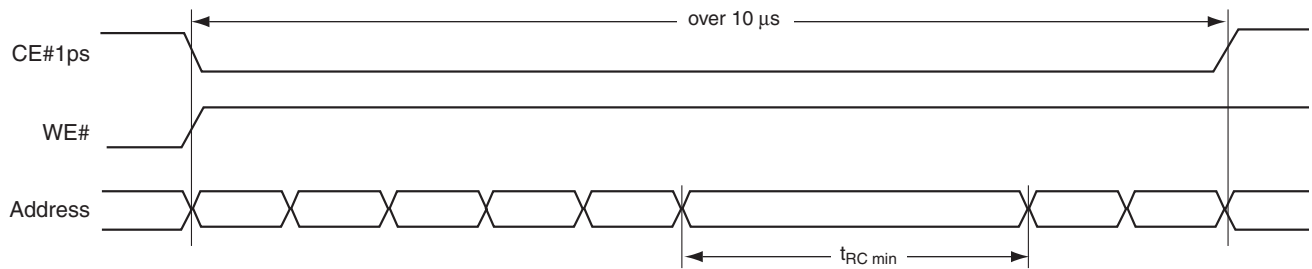


Figure 34. Read Address Skew

**Note:** If multiple invalid address cycles shorter than  $t_{RC\ min}$  occur for a period greater than 10 μs, at least one valid address cycle over  $t_{RC\ min}$  is required during that period.

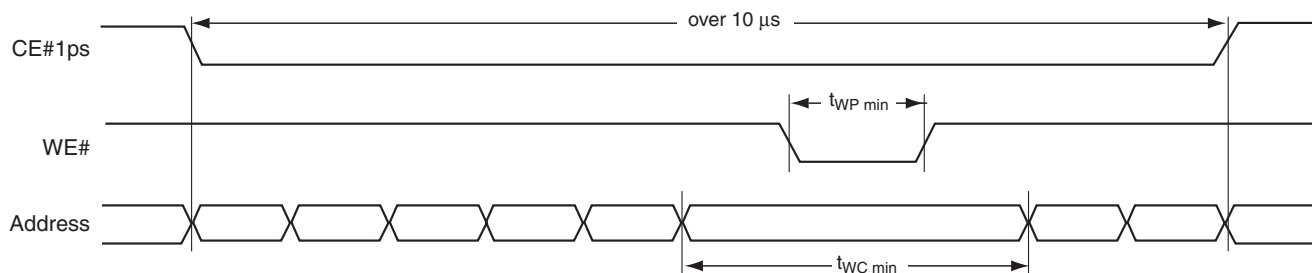
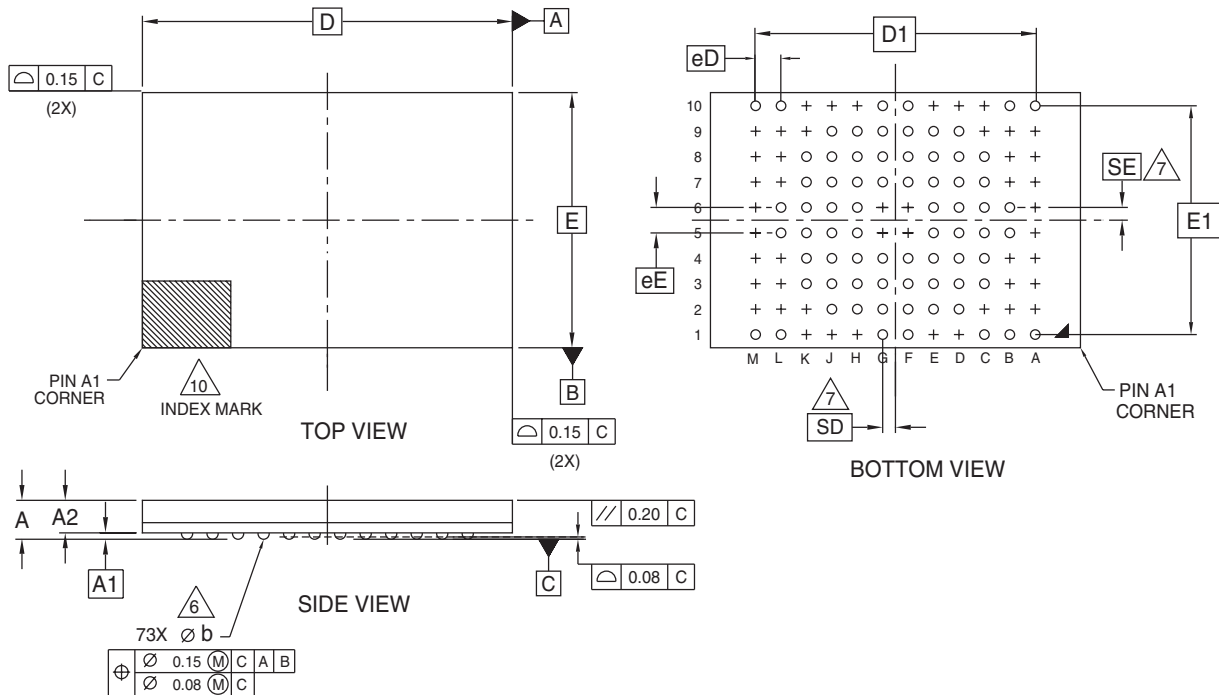


Figure 35. Write Address Skew

**Note:** If multiple invalid address cycles shorter than  $t_{WC\ min}$  occur for a period greater than 10 μs, at least one valid address cycle over  $t_{WC\ min}$ , in addition to  $t_{WP\ min}$ , is required during that period.

# PHYSICAL DIMENSIONS

## TLA073—73-Ball Fine-Pitch Grid Array 8 x 11.6 mm



|               |                                                                                                                                                                   |      |      |                          |
|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|--------------------------|
| PACKAGE       | TLA 073                                                                                                                                                           |      |      | NOTE                     |
| JEDEC         | N/A                                                                                                                                                               |      |      |                          |
|               | 11.60 mm X 8.00 mm PACKAGE                                                                                                                                        |      |      |                          |
| SYMBOL        | MIN.                                                                                                                                                              | NOM. | MAX. |                          |
| A             | ---                                                                                                                                                               | ---  | 1.20 | PROFILE                  |
| A1            | 0.20                                                                                                                                                              | ---  | ---  | BALL HEIGHT              |
| A2            | 0.81                                                                                                                                                              | ---  | 0.97 | BODY THICKNESS           |
| <div>D</div>  | 11.60 BSC                                                                                                                                                         |      |      | BODY SIZE                |
| <div>E</div>  | 8.00 BSC                                                                                                                                                          |      |      | BODY SIZE                |
| <div>D1</div> | 8.80 BSC                                                                                                                                                          |      |      | MATRIX FOOTPRINT         |
| <div>E1</div> | 7.20 BSC                                                                                                                                                          |      |      | MATRIX FOOTPRINT         |
| MD            | 12                                                                                                                                                                |      |      | MATRIX SIZE D DIRECTION  |
| ME            | 10                                                                                                                                                                |      |      | MATRIX SIZE E DIRECTION  |
| n             | 73                                                                                                                                                                |      |      | BALL COUNT               |
| Øb            | 0.33                                                                                                                                                              | ---  | 0.43 | BALL DIAMETER            |
| <div>eE</div> | 0.80 BSC                                                                                                                                                          |      |      | BALL PITCH               |
| <div>eD</div> | 0.80 BSC                                                                                                                                                          |      |      | BALL PITCH               |
| SD/SE         | 0.40 BSC                                                                                                                                                          |      |      | SOLDER BALL PLACEMENT    |
|               | A2,A3,A4,A5,A6,A7,A8,A9<br>B2,B3,B4,B7,B8,B9<br>C2,C9,C10,D1,D10,E1,E10<br>F5,F6,G5,G6,H1,H10,J1,J10<br>K1,K2,K9,K10,L2,L3,L4,L7,L8,L9<br>M2,M3,M4,M5,M6,M7,M8,M9 |      |      | DEPOPULATED SOLDER BALLS |

### NOTES:

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
- [e] REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE =  $\frac{E}{2}$
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- NOT USED.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

w053003-163814c

## REVISION SUMMARY

### Revision A (June 16, 2003)

Initial release.

### Revision A+1 (July 14, 2003)

#### Sector Protection

*Selecting a Sector Protection Mode:* Slightly modified text to improve readability.

#### Pin Description

Corrected typo in WP#/ACC pin name.

#### Flash AC Characteristics

*Read-only Operation tables (Am29PDL127H and Am29PDL129H):* Changed  $t_{OE}$  specification for the 66 speed option to 25 ns.

#### SRAM AC Characteristics

*Write Cycle table:* Added  $t_{AW}$ ,  $t_{CEH}$ , and  $t_{WEH}$  specifications to table. Changed  $t_{BW}$  minimum time for the 66 speed option to 65 ns.

*Figure 28, Pseudo SRAM Write Cycle—WE# Control:* Added  $t_{AW}$  and  $t_{WEH}$  to figure.

*Figure 29, Pseudo SRAM Write Cycle—CE#1ps Control:* Added  $t_{CEH}$  to figure.

### Revision A+2 (July 21, 2003)

#### DC Characteristics

*Zero Power Flash:* Deleted selection.

### Revision A+3 (December 16, 2003)

#### Lookahead Ballout Diagram

Added section and figure.

#### Figure 1, In-System Sector Protection/ Sector Unprotection Algorithms

Corrected command sequence to indicate writing 68h (for protect) and 48h (for verify) with A7–A0 set to 00011010b.

#### SecSi™ (Secured Silicon) Sector Flash Memory Region

*Customer-Lockable Area:* Added sector protection figure, modified text and changed figure reference in first bullet from Figure 1 to Figure 3.

#### Table 16, Sector Protection Command Definitions

Corrected number of cycles for SecSi Protection Bit Status, PPMLB Status, and SPMLB Status from 4 to 5 cycles. For these command sequences, inserted a cycle before the final read cycle (RD0).

#### ESD Immunity

Added section.

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