CMOS Low Voltage 2.5 Ω Dual SPDT Switch

ADG736

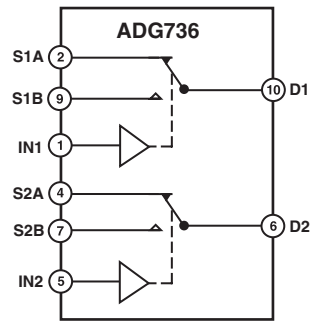
FEATURES

1.8 V to 5.5 V Single Supply
2.5 Ω (Typ) On Resistance
Low On Resistance Flatness
–3 dB Bandwidth >200 MHz
Rail-to-Rail Operation
10-Lead MSOP Package
Fast Switching Times
  t_{ON} 16 ns
  t_{OFF} 8 ns
Typical Power Consumption (<0.01 μW)
TTL/CMOS Compatible

APPLICATIONS

USB 1.1 Signal Switching Circuits
Cell Phones
PDAs
Battery-Powered Systems
Communication Systems
Sample-and-Hold Systems
Audio Signal Routing
Audio and Video Switching
Mechanical Reed Relay Replacement

FUNCTIONAL BLOCK DIAGRAM



SWITCHES SHOWN FOR A LOGIC 1 INPUT

GENERAL DESCRIPTION

The ADG736 is a monolithic device comprised of two independently selectable CMOS SPDT switches. These switches are designed on a submicron process that provides low power dissipation yet gives high switching speed, low on resistance, low leakage currents, and wide input signal bandwidth.

The on resistance profile is very flat over the full analog signal range. This ensures excellent linearity and low distortion when switching audio signals. Fast switching speed also makes the part suitable for video signal switching.

The ADG736 can operate from a single 1.8 V to 5.5 V supply, making it ideally suited to portable and battery-powered instruments.

Each switch conducts equally well in both directions when on and each has an input signal range that extends to the power supplies. The ADG736 exhibits break-before-make switching action.

The ADG736 is available in a 10-lead MSOP package.

PRODUCT HIGHLIGHTS

1. 1.8 V to 5.5 V Single-Supply Operation.
   The ADG736 offers high performance, including low on resistance and fast switching times and is fully specified and guaranteed with 3 V and 5 V supply rails.
2. Very Low R_{ON} (4.5 Ω Max at 5 V, 8 Ω Max at 3 V).
   At supply voltage of 1.8 V, R_{ON} is typically 35 Ω over the temperature range.
3. Low On Resistance Flatness.
4. –3 dB Bandwidth >200 MHz.
5. Low Power Dissipation.
   CMOS construction ensures low power dissipation.
6. Fast t_{ON}/t_{OFF}.
7. Break-Before-Make Switching Action.
8. 10-Lead MSOP Package.

REV. A

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ADG736–SPECIFICATIONS[1] (V_{DD} = 5 V ± 10%, GND = 0 V. All Specifications –40°C to +85°C, unless otherwise noted.)

Parameter	B Version 25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance (R_{ON})	2.5		Ω typ	V_S = 0 V to V_{DD}, I_{DS} = –10 mA;
	4	4.5	Ω max	Test Circuit 1
On Resistance Match between Channels (ΔR_{ON})		0.1	Ω typ	V_S = 0 V to V_{DD}, I_{DS} = –10 mA
		0.4	Ω max	
On Resistance Flatness ($R_{FLAT\ (ON)}$)	0.5		Ω typ	V_S = 0 V to V_{DD}, I_{DS} = –10 mA
		1.2	Ω max	
LEAKAGE CURRENTS				V_{DD} = 5.5 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_S = 4.5 V/1 V, V_D = 1 V/4.5 V;
	±0.1	±0.3	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	V_S = V_D = 1 V or 4.5 V;
	±0.1	±0.3	nA max	Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	12		ns typ	R_L = 300 Ω, C_L = 35 pF
		16	ns max	V_S = 3 V; Test Circuit 4
t_{OFF}	5		ns typ	R_L = 300 Ω, C_L = 35 pF
		8	ns max	V_S = 3 V; Test Circuit 4
Break-before-Make Time Delay, t_D	7		ns typ	R_L = 300 Ω, C_L = 35 pF
		1	ns min	V_{S1} = V_{S2} = 3 V; Test Circuit 5
Off Isolation	–62		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	–82		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 6
Channel-to-Channel Crosstalk	–62		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	–82		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
Bandwidth –3 dB	200		MHz typ	R_L = 50 Ω, C_L = 5 pF; Test Circuit 8
C_S (OFF)	9		pF typ	
C_D, C_S (ON)	32		pF typ	
POWER REQUIREMENTS				V_{DD} = 5.5 V Digital Inputs = 0 V or 5 V
I_{DD}	0.001		μA typ	
		1.0	μA max	

NOTES

[1]Temperature range is –40°C to +85°C for the B Version.

[2]Guaranteed by design not subject to production test.

Specifications subject to change without notice.

SPECIFICATIONS[1] (V_{DD} = 3 V ± 10%, GND = 0 V. All Specifications –40°C to +85°C, unless otherwise noted.)

Parameter	B Version 25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance (R_{ON})	5	5.5	Ω typ	V_S = 0 V to V_{DD}, I_{DS} = –10 mA;
		8	Ω max	Test Circuit 1
On Resistance Match between Channels (ΔR_{ON})	0.1		Ω typ	V_S = 0 V to V_{DD}, I_{DS} = –10 mA
		0.4	Ω max	
On Resistance Flatness ($R_{FLAT (ON)}$)		2.5	Ω typ	V_S = 0 V to V_{DD}, I_{DS} = –10 mA
LEAKAGE CURRENTS				V_{DD} = 3.3 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V;
	±0.1	±0.3	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	V_S = V_D = 1 V or 3 V;
	±0.1	±0.3	nA max	Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.4	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	14		ns typ	R_L = 300 Ω, C_L = 35 pF
		20	ns max	V_S = 2 V; Test Circuit 4
t_{OFF}	6		ns typ	R_L = 300 Ω, C_L = 35 pF
		10	ns max	V_S = 2 V; Test Circuit 4
Break-before-Make Time Delay, t_D	7		ns typ	R_L = 300 Ω, C_L = 35 pF
		1	ns min	V_{S1} = V_{S2} = 2 V; Test Circuit 5
Off Isolation	–62		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	–82		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 6
Channel-to-Channel Crosstalk	–62		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	–82		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
Bandwidth –3 dB	200		MHz typ	R_L = 50 Ω, C_L = 5 pF; Test Circuit 8
C_S (OFF)	9		pF typ	
C_D, C_S (ON)	32		pF typ	
POWER REQUIREMENTS				V_{DD} = 3.3 V Digital Inputs = 0 V or 3 V
I_{DD}	0.001		μA typ	
		1.0	μA max	

NOTES
[1]Temperature range is –40°C to +85°C for the B Version.
[2]Guaranteed by design not subject to production test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C, unless otherwise noted.)

V_{DD} to GND . . . . . –0.3 V to +6 V
Analog, Digital Inputs[2] . . . . . –0.3 V to V_{DD} + 0.3 V or 30 mA, Whichever Occurs First
Continuous Current, S or D . . . . . 30 mA
Peak Current, S or D . . . . . 100 mA
(Pulsed at 1 ms, 10% Duty Cycle Max)
Operating Temperature Range
Industrial (B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
MSOP Package, Power Dissipation . . . . . 315 mW
θ_{JA} Thermal Impedance . . . . . 205°C/W
Lead Temperature, Soldering (10 sec) . . . . . 300°C
IR Reflow, Peak Temperature (<20 sec) . . . . . 235°C
ESD . . . . . 2 kV

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

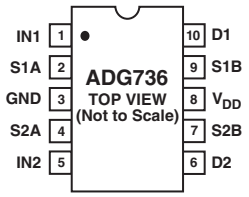
[2]Overvoltages at IN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

ORDERING GUIDE

Model	Temperature Range	Branding	Package Option*
ADG736BRM	–40°C to +85°C	SAB	RM-10
ADG736BRM-REEL	–40°C to +85°C	SAB	RM-10
ADG736BRM-REEL7	–40°C to +85°C	SAB	RM-10

*RM = MSOP

PIN CONFIGURATION (10-Lead MSOP)



TERMINOLOGY

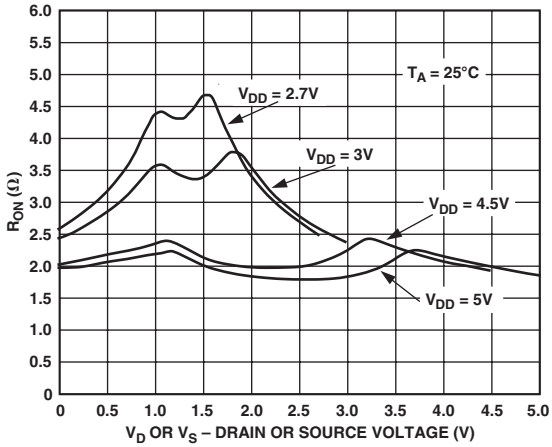
V_{DD}	Most positive power supply potential.
GND	Ground (0 V) reference.
S	Source terminal. May be an input or output.
D	Drain terminal. May be an input or output.
IN	Logic control input.
R_{ON}	Ohmic resistance between D and S.
ΔR_{ON}	On resistance match between any two channels i.e., R_{ON} max – R_{ON} min.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
I_S (OFF)	Source leakage current with the switch OFF.
I_D, I_S (ON)	Channel leakage current with the switch ON.
V_D (V_S)	Analog voltage on terminals D and S.
C_S (OFF)	OFF switch source capacitance.
C_D, C_S (ON)	ON switch capacitance.
t_{ON}	Delay between applying the digital control input and the output switching on. See Test Circuit 4.
t_{OFF}	Delay between applying the digital control input and the output switching off.
t_D	OFF time or ON time measured between the 90% points of both switches, when switching from one address state to another. See Test Circuit 5.
Crosstalk	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an OFF switch.
Bandwidth	The frequency at which the output is attenuated by –3 dBs.
On Response	The frequency response of the ON switch.
On Loss	The voltage drop across the ON switch, seen on the on response versus frequency plot as how many dBs the signal is away from 0 dB at very low frequencies.

Table I. Truth Table

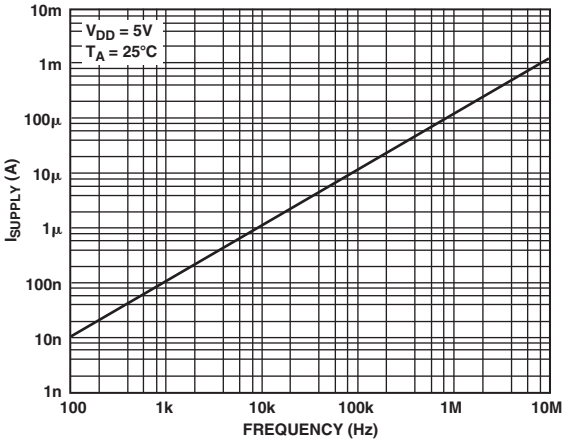
Logic	Switch A	Switch B
0	Off	On
1	On	Off

CAUTION

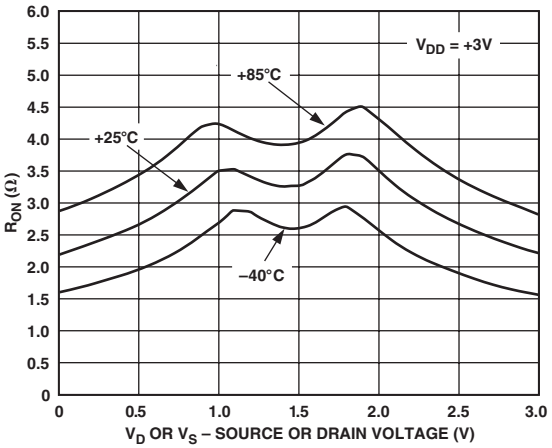
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG736 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



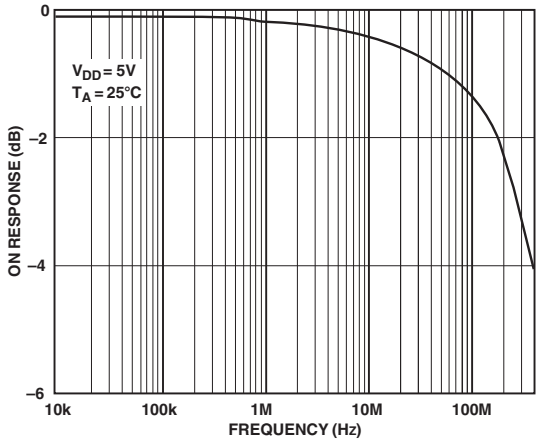
TPC 1. On Resistance as a Function of V_D (V_S) Single Supplies



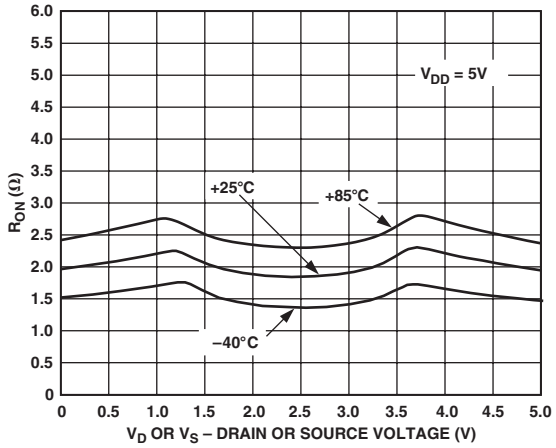
TPC 4. Supply Current vs. Input Switching Frequency



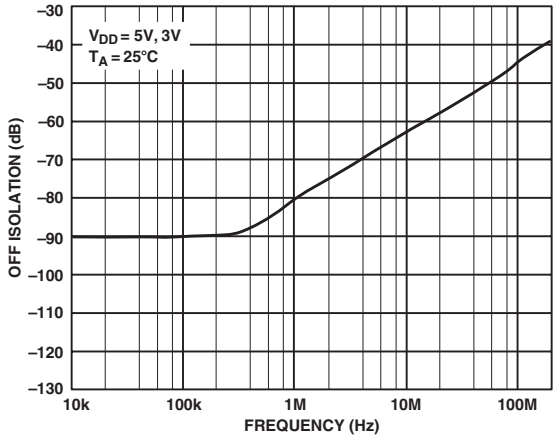
TPC 2. On Resistance as a Function of V_D (V_S) for Different Temperatures V_{DD} = 3 V



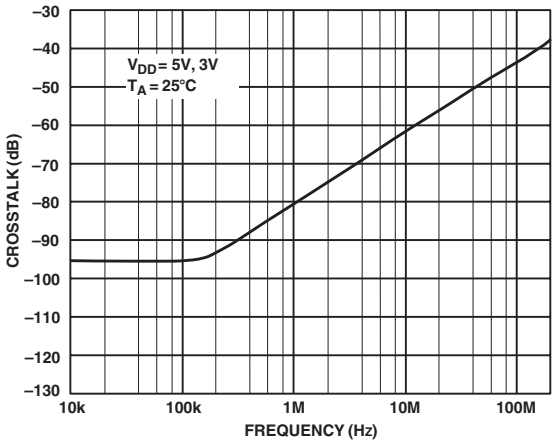
TPC 5. On Response vs. Frequency



TPC 3. On Resistance as a Function of V_D (V_S) for Different Temperatures V_{DD} = 5 V



TPC 6. Off Isolation vs. Frequency



TPC 7. Crosstalk vs. Frequency

APPLICATIONS

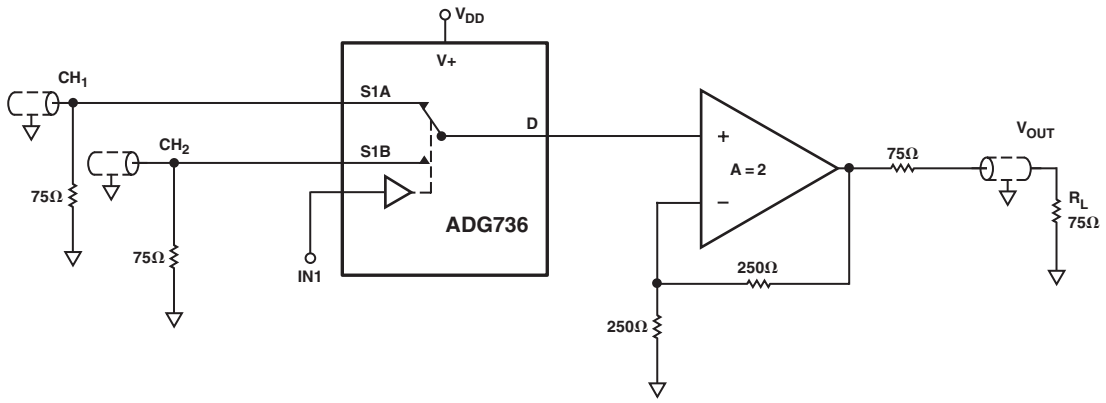
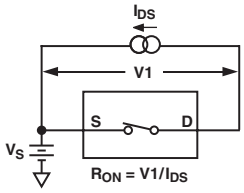
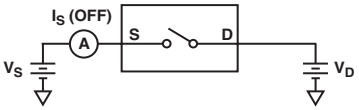


Figure 1. Using the ADG736 to Select between Two Video Signals

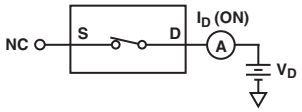
Test Circuits



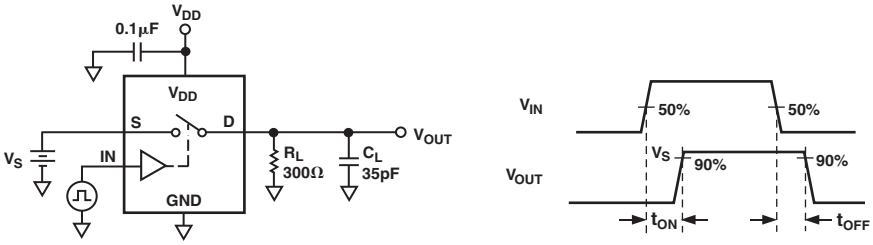
Test Circuit 1. On Resistance



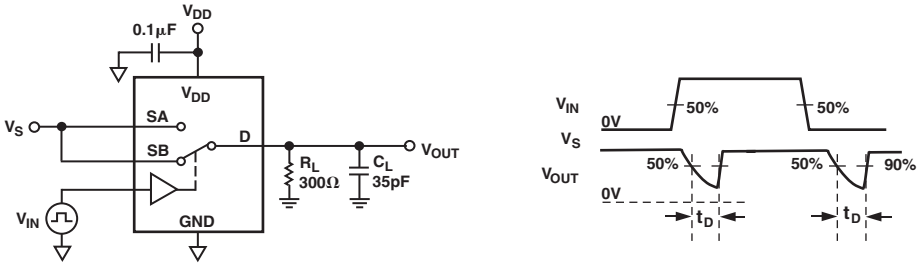
Test Circuit 2. Off Leakage



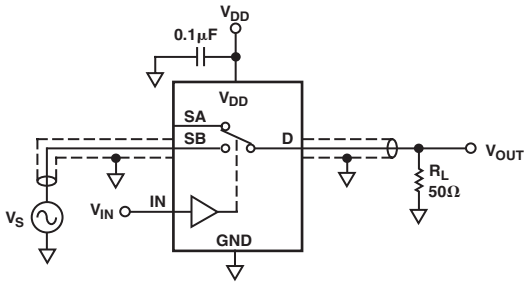
Test Circuit 3. On Leakage



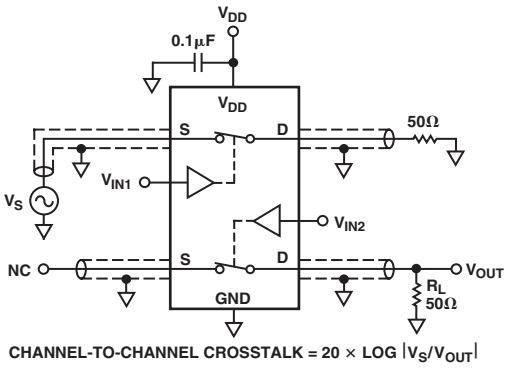
Test Circuit 4. Switching Times



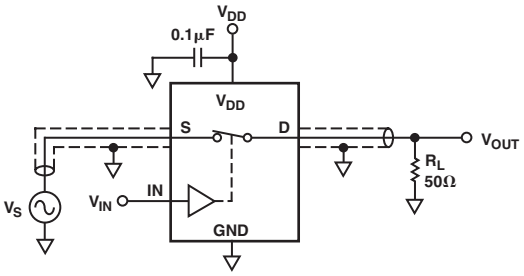
Test Circuit 5. Break-before-Make Time Delay, t_D



Test Circuit 6. Off Isolation



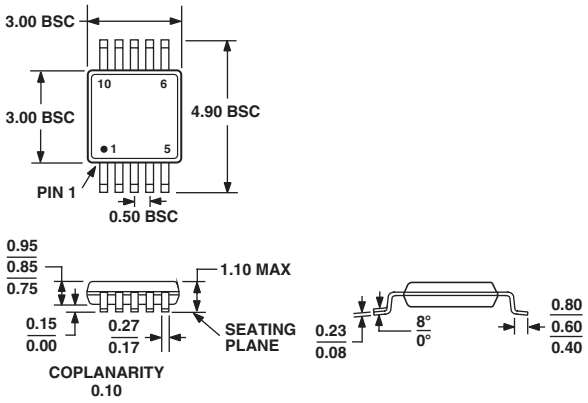
Test Circuit 7. Channel-to-Channel Crosstalk



Test Circuit 8. Bandwidth

OUTLINE DIMENSIONS

10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187BA

C00046–0–11/03(A)

Revision History

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Changes to Test Circuit 3	7
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