



**ANALOG
DEVICES**

**16-/32-Channel, 4 Ω
+1.8 V to +5.5 V, ± 2.5 V Analog Multiplexers**

ADG726/ADG732

FEATURES

1.8 V to 5.5 V Single Supply
 ± 2.5 V Dual-Supply Operation
 4 Ω On Resistance
 0.5 Ω On Resistance Flatness
 48-Lead TQFP or 48-Lead 7 mm $\times$ 7 mm CSP Packages
 Rail-to-Rail Operation
 30 ns Switching Times
 Single 32-to-1 Channel Multiplexer
 Dual/Differential 16-to-1 Channel Multiplexer
 TTL/CMOS Compatible Inputs
 For Functionally Equivalent Devices with Serial Interface
 See ADG725/ADG731

APPLICATIONS

Optical Applications
 Data Acquisition Systems
 Communication Systems
 Relay Replacement
 Audio and Video Switching
 Battery-Powered Systems
 Medical Instrumentation
 Automatic Test Equipment

GENERAL DESCRIPTION

The ADG726/ADG732 are monolithic CMOS 32-channel/dual 16-channel analog multiplexers. The ADG732 switches one of 32 inputs (S1-S32) to a common output, D, as determined by the 5-bit binary address lines A0, A1, A2, A3, and A4. The ADG726 switches one of 16 inputs as determined by the 4-bit binary address lines A0, A1, A2, and A3.

On-chip latches facilitate microprocessor interfacing. The ADG726 device may also be configured for differential operation by tying CSA and CSB together. An $\overline{\text{EN}}$ input is used to enable or disable the devices. When disabled, all channels are switched OFF.

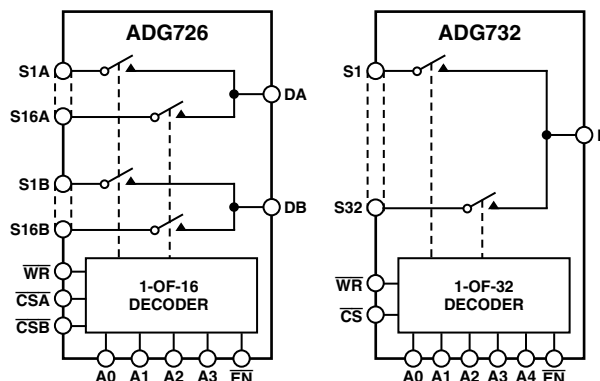
These multiplexers are designed on an enhanced submicron process that provides low power dissipation yet gives high switching speed, very low on resistance, and leakage currents. They operate from a single supply of +1.8 V to +5.5 V and a ± 2.5 V dual supply, making them ideally suited to a variety of applications. On resistance is in the region of a few ohms and is closely matched between switches and very flat over the full signal range. These parts can operate equally well as either multiplexers or demultiplexers and have an input signal range that extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All channels exhibit break-before-make switching action, preventing momentary shorting when switching channels.

They are available in either 48-lead CSP or TQFP packages.

REV. 0

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FUNCTIONAL BLOCK DIAGRAMS



PRODUCT HIGHLIGHTS

1. +1.8 V to +5.5 V single- or ± 2.5 V dual-supply operation. These parts are specified and guaranteed with +5 V $\pm$ 10%, +3 V $\pm$ 10% single-supply, and ± 2.5 V $\pm$ 10% dual-supply rails.
2. On resistance of 4 Ω
3. Guaranteed break-before-make switching action
4. 7 mm $\times$ 7 mm 48-lead chip scale package (CSP) or 48-lead TQFP package

ADG726/ADG732—SPECIFICATIONS¹ (V_{DD} = 5 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.)

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	–40°C to +85°C		
ANALOG SWITCH				
Analog Signal Range		0 V to V _{DD}	V	
On Resistance (R _{ON})	4		Ω typ	V _S = 0 V to V _{DD} , I _{DS} = 10 mA;
	5.5	6	Ω max	Test Circuit 1
On Resistance Match Between Channels (ΔR _{ON})		0.3	Ω typ	V _S = 0 V to V _{DD} , I _{DS} = 10 mA
		0.8	Ω max	
On Resistance Flatness (R _{FLAT(ON)})	0.5		Ω typ	V _S = 0 V to V _{DD} , I _{DS} = 10 mA
		1	Ω max	
LEAKAGE CURRENTS				
Source OFF Leakage I _S (OFF)	±0.01		nA typ	V _{DD} = 5.5 V
	±0.25	±1	nA max	V _D = 4.5 V/1 V, V _S = 1 V/4.5 V;
Drain OFF Leakage I _D (OFF)	±0.05		nA typ	Test Circuit 2
ADG726	±0.5	±2.5	nA max	V _D = 4.5 V/1 V, V _S = 1 V/4.5 V;
ADG732	±1	±5	nA max	Test Circuit 3
Channel ON Leakage I _D , I _S (ON)	±0.05		nA typ	V _D = V _S = 1 V, or 4.5 V;
ADG726	±0.5	±2.5	nA max	Test Circuit 4
ADG732	±1	±5	nA max	
DIGITAL INPUTS				
Input High Voltage, V _{INH}		2.4	V min	
Input Low Voltage, V _{INL}		0.8	V max	
Input Current				
I _{INL} or I _{INH}	0.005	±0.5	μA typ	V _{IN} = V _{INL} or V _{INH}
			μA max	
C _{IN} , Digital Input Capacitance	5		pF typ	
DYNAMIC CHARACTERISTICS ²				
t _{TRANSITION}	23		ns typ	R _L = 300 Ω, C _L = 35 pF, Test Circuit 5
	34	40	ns max	V _{S1} = 3 V/0 V, V _{S32} = 0 V/3 V
Break-Before-Make Time Delay, t _D	18		ns typ	R _L = 300 Ω, C _L = 35 pF;
	1		ns min	V _S = 3 V; Test Circuit 6
t _{ON} ($\overline{\text{CS}}$, $\overline{\text{WR}}$)	18		ns typ	V _S = 3 V; Test Circuit 7
	25	32	ns max	R _L = 300 Ω, C _L = 35 pF;
t _{OFF} ($\overline{\text{CS}}$, $\overline{\text{WR}}$)	17		ns typ	V _S = 3 V; Test Circuit 7
	23	29	ns max	R _L = 300 Ω, C _L = 35 pF;
t _{ON} ($\overline{\text{EN}}$)	24		ns typ	R _L = 300 Ω, C _L = 35 pF;
	32	40	ns max	V _S = 3 V; Test Circuit 8
t _{OFF} ($\overline{\text{EN}}$)	16		ns typ	R _L = 300 Ω, C _L = 35 pF;
	22	25	ns max	V _S = 3 V; Test Circuit 8
Charge Injection	5		pC typ	V _S = 2.5 V, R _S = 0 Ω, C _L = 1 nF;
				Test Circuit 9
OFF Isolation	–72		dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz;
				Test Circuit 10
Channel-to-Channel Crosstalk	–72		dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz;
				Test Circuit 11
–3 dB Bandwidth				R _L = 50 Ω, C _L = 5 pF; Test Circuit 12
ADG726	34		MHz typ	
ADG732	18		MHz typ	
C _S (OFF)	13		pF typ	f = 1 MHz
C _D (OFF)				
ADG726	170		pF typ	f = 1 MHz
ADG732	340		pF typ	f = 1 MHz
C _D , C _S (ON)				
ADG726	175		pF typ	f = 1 MHz
ADG732	350		pF typ	f = 1 MHz
POWER REQUIREMENTS				
I _{DD}	10		μA typ	V _{DD} = 5.5 V
		20	μA max	Digital Inputs = 0 V or 5.5 V

NOTES

¹Temperature range is as follows: B Version: –40°C to +85°C.

²Guaranteed by design; not subject to production test.

Specifications subject to change without notice.

SPECIFICATIONS¹

($V_{DD} = 3\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.)

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	−40°C to +85°C		
ANALOG SWITCH				
Analog Signal Range		0 V to V _{DD}	V	
On Resistance (R _{ON})	7		Ω typ	V _S = 0 V to V _{DD} , I _{DS} = 10 mA;
	11	12	Ω max	Test Circuit 1
On Resistance Match Between Channels (ΔR _{ON})		0.35	Ω typ	V _S = 0 V to V _{DD} , I _{DS} = 10 mA
		1	Ω max	
On Resistance Flatness (R _{FLAT(ON)})		3	Ω typ	V _S = 0 V to V _{DD} , I _{DS} = 10 mA
LEAKAGE CURRENTS				
Source OFF Leakage I _S (OFF)	±0.01		nA typ	V _{DD} = 3.3 V
	±0.25	±1	nA max	V _S = 3 V/1 V, V _D = 1 V/3 V;
Drain OFF Leakage I _D (OFF)	±0.05		nA max	Test Circuit 2
ADG726	±0.5	±2.5	nA max	V _S = 1 V/3 V, V _D = 3 V/1 V;
ADG732	±1	±5	nA max	Test Circuit 3
Channel ON Leakage I _D , I _S (ON)	±0.05		nA typ	V _S = V _D = 1 V or 3 V;
ADG726	±0.5	±2.5	nA max	Test Circuit 4
ADG732	±1	±5	nA max	
DIGITAL INPUTS				
Input High Voltage, V _{INH}		2.0	V min	
Input Low Voltage, V _{INL}		0.7	V max	
Input Current				
I _{INL} or I _{INH}	0.005		μA typ	V _{IN} = V _{INL} or V _{INH}
		±0.5	μA max	
C _{IN} , Digital Input Capacitance	5		pF typ	
DYNAMIC CHARACTERISTICS ²				
t _{TRANSITION}	34		ns typ	R _L = 300 Ω, C _L = 35 pF; Test Circuit 5
	52	62	ns max	V _{S1} = 2 V/0 V, V _{S32} = 0 V/2 V
Break-Before-Make Time Delay, t _D	26		ns typ	R _L = 300 Ω, C _L = 35 pF;
	1		ns min	V _S = 2 V; Test Circuit 6
t _{ON} ($\overline{WR}$, $\overline{CS}$)	29		ns typ	V _S = 2 V; Test Circuit 7
	43	52	ns max	R _L = 300 Ω, C _L = 35 pF;
t _{OFF} ($\overline{WR}$, $\overline{CS}$)	26		ns typ	V _S = 2 V; Test Circuit 7
	38	42	ns max	R _L = 300 Ω, C _L = 35 pF;
t _{ON} ($\overline{EN}$, $\overline{WR}$)	33		ns typ	R _L = 300 Ω, C _L = 35 pF;
	48	55	ns max	V _S = 3 V; Test Circuit 8
t _{OFF} ($\overline{EN}$)	19		ns typ	R _L = 300 Ω, C _L = 35 pF;
	25	28	ns max	V _S = 2 V; Test Circuit 8
Charge Injection	1		pC typ	V _S = 1.5 V, R _S = 0 Ω, C _L = 1 nF;
				Test Circuit 9
Off Isolation	−72		dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz;
				Test Circuit 10
Channel-to-Channel Crosstalk	−72		dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz;
				Test Circuit 11
−3 dB Bandwidth				R _L = 50 Ω, C _L = 5 pF; Test Circuit 12
ADG726	34		MHz typ	
ADG732	18		MHz typ	
C _S (OFF)	13		pF typ	f = 1 MHz
C _D (OFF)				
ADG726	170		pF typ	f = 1 MHz
ADG732	340		pF typ	f = 1 MHz
C _D , C _S (ON)				
ADG726	175		pF typ	f = 1 MHz
ADG732	350		pF typ	f = 1 MHz
POWER REQUIREMENTS				
I _{DD}	5		μA typ	V _{DD} = 3.3 V
		10	μA max	Digital Inputs = 0 V or 3.3 V

NOTES

¹Temperature ranges are as follows: B Version: –40°C to +85°C.²Guaranteed by design; not subject to production test.

Specifications subject to change without notice.

ADG726/ADG732 SPECIFICATIONS¹

DUAL SUPPLY ($V_{DD} = +2.5 \text{ V} \pm 10\%$, $V_{SS} = -2.5 \text{ V} \pm 10\%$, $GND = 0 \text{ V}$, unless otherwise noted.)

Parameter	B Version –40°C to +85°C		Unit	Test Conditions/Comments
	+25°C			
ANALOG SWITCH				
Analog Signal Range		V _{SS} to V _{DD}	V	
On Resistance (R _{ON})	4		Ω typ	V _S = V _{SS} to V _{DD} , I _{DS} = 10 mA;
	5.5	6	Ω max	Test Circuit 1
On Resistance Match Between		0.3	Ω typ	V _S = V _{SS} to V _{DD} , I _{DS} = 10 mA
Channels (ΔR _{ON})		0.8	Ω max	
On Resistance Flatness (R _{FLAT(ON)})	0.5		Ω typ	V _S = V _{SS} to V _{DD} , I _{DS} = 10 mA
		1	Ω max	
LEAKAGE CURRENTS				
Source OFF Leakage I _S (OFF)	±0.01		nA typ	V _{DD} = +2.75 V, V _{SS} = –2.75 V
	±0.25	±0.5	nA max	V _S = +2.25 V/–1.25 V, V _D = –1.25 V/+2.25 V;
Drain OFF Leakage I _D (OFF)	±0.05		nA max	Test Circuit 2
ADG726	±0.5	±2.5	nA max	V _S = +2.25 V/–1.25 V, V _D = –1.25 V/+2.25 V;
ADG732	±1	±5	nA max	Test Circuit 3
Channel ON Leakage I _D , I _S (ON)	±0.05		nA typ	V _S = V _D = +2.25 V/–1.25 V;
ADG726	±0.5	±2.5	nA max	Test Circuit 4
ADG732	±1	±5	nA max	
DIGITAL INPUTS				
Input High Voltage, V _{INH}		1.7	V min	
Input Low Voltage, V _{INL}		0.7	V max	
Input Current				
I _{INL} or I _{INH}	0.005		μA typ	V _{IN} = V _{INL} or V _{INH}
		±0.5	μA max	
C _{IN} , Digital Input Capacitance	5		pF typ	
DYNAMIC CHARACTERISTICS ²				
t _{TRANSITION}	33		ns typ	R _L = 300 Ω, C _L = 35 pF; Test Circuit 5
	45	51	ns max	V _{S1} = 1.5 V/0 V, V _{S32} = 0 V/1.5 V
Break-Before-Make Time Delay, t _D	15		ns typ	R _L = 300 Ω, C _L = 35 pF;
	1		ns min	V _S = 1.5 V; Test Circuit 6
t _{ON} ($\overline{CS}$, $\overline{WR}$)	21		ns typ	V _S = 1.5 V; Test Circuit 7
	30	37	ns max	R _L = 300 Ω, C _L = 35 pF;
t _{OFF} ($\overline{CS}$, $\overline{WR}$)	20		ns typ	V _S = 1.5 V; Test Circuit 7
	29	35	ns max	R _L = 300 Ω, C _L = 35 pF;
t _{ON} ($\overline{EN}$, $\overline{WR}$)	26		ns typ	R _L = 300 Ω, C _L = 35 pF;
	37		ns max	V _S = 1.5 V; Test Circuit 8
t _{OFF} ($\overline{EN}$)	18		ns typ	R _L = 300 Ω, C _L = 35 pF;
	26	29	ns max	V _S = 1.5 V; Test Circuit 8
Charge Injection	1		pC typ	V _S = 0 V, R _S = 0 Ω, C _L = 1 nF;
				Test Circuit 9
OFF Isolation	–72		dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz;
				Test Circuit 10
Channel-to-Channel Crosstalk	–72		dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz;
				Test Circuit 11
–3 dB Bandwidth				R _L = 50 Ω, C _L = 5 pF; Test Circuit 12
ADG726	34		MHz typ	
ADG732	18		MHz typ	
C _S (OFF)	13		pF typ	
C _D (OFF)				
ADG726	137		pF typ	f = 1 MHz
ADG732	275		pF typ	f = 1 MHz
C _D , C _S (ON)				
ADG726	150		pF typ	f = 1 MHz
ADG732	300		pF typ	f = 1 MHz
POWER REQUIREMENTS				
I _{DD}	10		μA typ	V _{DD} = +2.75 V
		20	μA max	Digital Inputs = 0 V or +2.75 V
I _{SS}	10		μA typ	V _{SS} = –2.75 V
		20	μA max	Digital Inputs = 0 V or +2.75 V

NOTES

¹Temperature range is as follows: B Version: –40°C to +85°C.

²Guaranteed by design; not subject to production test.

Specifications subject to change without notice.

TIMING CHARACTERISTICS^{1, 2, 3}

Parameter	Limit at T _{MIN} , T _{MAX}	Unit	Conditions/Comments
t ₁	0	ns min	$\overline{\text{CS}}$ to $\overline{\text{WR}}$ Setup Time
t ₂	0	ns min	$\overline{\text{CS}}$ to $\overline{\text{WR}}$ Hold Time
t ₃	10	ns min	$\overline{\text{WR}}$ Pulsewidth
t ₄	10	ns min	Time between $\overline{\text{WR}}$ Cycles
t ₅	5	ns min	Address, Enable Setup Time
t ₆	2	ns min	Address, Enable Hold Time

NOTES

¹See Figure 1.²All input signals are specified with tr = tf = 1 ns (10% to 90% of V_{DD}).³Guaranteed by design and characterization, not production tested.

Specifications subject to change without notice.

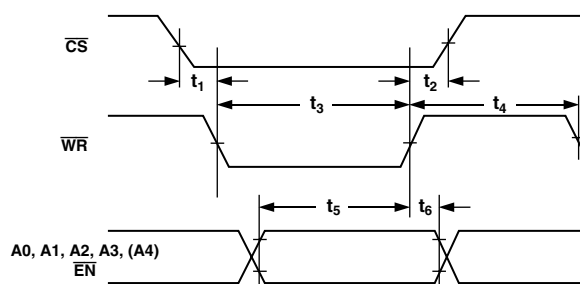


Figure 1. Timing Diagram

Figure 1 shows the timing sequence for latching the switch address and enable inputs. The latches are level sensitive; therefore, while $\overline{\text{WR}}$ is held low, the latches are transparent and the switches respond to changing the address and enable the inputs.

Input data is latched on the rising edge of $\overline{\text{WR}}$. The ADG726 has two $\overline{\text{CS}}$ inputs. This enables the part to be used either as a dual 16-1 channel multiplexer or a differential 16-channel multiplexer. If a differential output is required, tie $\overline{\text{CSA}}$ and $\overline{\text{CSB}}$ together.

ADG726/ADG732

ABSOLUTE MAXIMUM RATINGS¹

(T_A = 25°C, unless otherwise noted.)

V _{DD} to V _{SS}	7 V
V _{DD} to GND	–0.3 V to +7 V
V _{SS} to GND	+0.3 V to –7 V
Analog Inputs ²	V _{SS} – 0.3 V to V _{DD} + 0.3 V or 30 mA, Whichever Occurs First
Digital Inputs ²	–0.3 V to V _{DD} + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D	60 mA (Pulsed at 1 ms, 10% Duty Cycle Max)
Continuous Current, S or D	30 mA
Operating Temperature Range Industrial (B Version)	–40°C to +85°C

Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
Thermal Impedance (Four-layer board) 48-Lead LFCSP	25°C/W
48-Lead TQFP	54.6°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	235°C

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overvoltages at A, EN, WR, CS, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG726BCP	–40°C to +85°C	Chip Scale Package (LPCSP)	CP-48
ADG726BSU	–40°C to +85°C	Thin Quad Flatpack (TQFP)	SU-48
ADG732BCP	–40°C to +85°C	Chip Scale Package (LPCSP)	CP-48
ADG732BSU	–40°C to +85°C	Thin Quad Flatpack (TQFP)	SU-48

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG726/ADG732 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATIONS LFCSP and TQFP

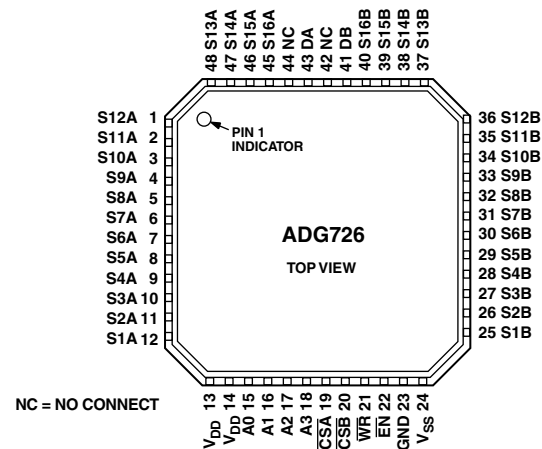
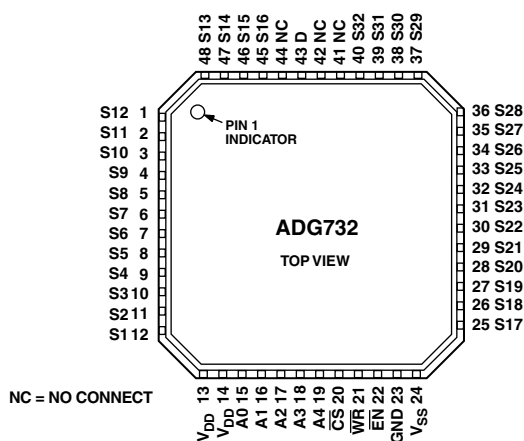


Table I. ADG726 Truth Table

A3	A2	A1	A0	$\overline{\text{EN}}$	$\overline{\text{CSA}}$	$\overline{\text{CSB}}$	$\overline{\text{WR}}$	ON Switch
X	X	X	X	X	1	1	L->H	Retains Previous Switch Condition
X	X	X	X	X	1	1	X	No Change in Switch Condition
X	X	X	X	1	0	0	0	NONE
0	0	0	0	0	0	0	0	S1A-DA, S1B-DB
0	0	0	1	0	0	0	0	S2A-DA, S2B-DB
0	0	1	0	0	0	0	0	S3A-DA, S3B-DB
0	0	1	1	0	0	0	0	S4A-DA, S4B-DB
0	1	0	0	0	0	0	0	S5A-DA, S5B-DB
0	1	0	1	0	0	0	0	S6A-DA, S6B-DB
0	1	1	0	0	0	0	0	S7A-DA, S7B-DB
0	1	1	1	0	0	0	0	S8A-DA, S8B-DB
1	0	0	0	0	0	0	0	S9A-DA, S9B-DB
1	0	0	1	0	0	0	0	S10A-DA, S10B-DB
1	0	1	0	0	0	0	0	S11A-DA, S11B-DB
1	0	1	1	0	0	0	0	S12A-DA, S12B-DB
1	1	0	0	0	0	0	0	S13A-DA, S13B-DB
1	1	0	1	0	0	0	0	S14A-DA, S14B-DB
1	1	1	0	0	0	0	0	S15A-DA, S15B-DB
1	1	1	1	0	0	0	0	S16A-DA, S16B-DB

X = Don't Care

Table II. ADG732 Truth Table

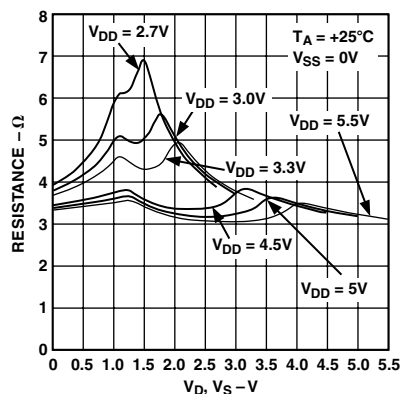
A4	A3	A2	A1	A0	$\overline{\text{EN}}$	$\overline{\text{CS}}$	$\overline{\text{WR}}$	Switch Condition
X	X	X	X	X	X	1	L->H	Retains Previous Switch Condition
X	X	X	X	X	X	1	X	No Change in Switch Condition
X	X	X	X	X	1	0	0	NONE
0	0	0	0	0	0	0	0	1
0	0	0	0	1	0	0	0	2
0	0	0	1	0	0	0	0	3
0	0	0	1	1	0	0	0	4
0	0	1	0	0	0	0	0	5
0	0	1	0	1	0	0	0	6
0	0	1	1	0	0	0	0	7
0	0	1	1	1	0	0	0	8
0	1	0	0	0	0	0	0	9
0	1	0	0	1	0	0	0	10
0	1	0	1	0	0	0	0	11
0	1	0	1	1	0	0	0	12
0	1	1	0	0	0	0	0	13
0	1	1	0	1	0	0	0	14
0	1	1	1	0	0	0	0	15
0	1	1	1	1	0	0	0	16
1	0	0	0	0	0	0	0	17
1	0	0	0	1	0	0	0	18
1	0	0	1	0	0	0	0	19
1	0	0	1	1	0	0	0	20
1	0	1	0	0	0	0	0	21
1	0	1	0	1	0	0	0	22
1	0	1	1	0	0	0	0	23
1	0	1	1	1	0	0	0	24
1	1	0	0	0	0	0	0	25
1	1	0	0	1	0	0	0	26
1	1	0	1	0	0	0	0	27
1	1	0	1	1	0	0	0	28
1	1	1	0	0	0	0	0	29
1	1	1	0	1	0	0	0	30
1	1	1	1	0	0	0	0	31
1	1	1	1	1	0	0	0	32

X = Don't Care

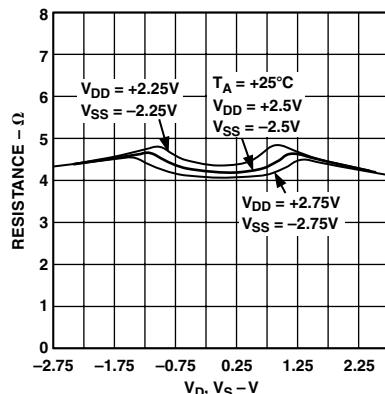
TERMINOLOGY

V_{DD}	Most Positive Power Supply Potential
V_{SS}	Most Negative Power Supply in a Dual-Supply Application. In single-supply applications, connect to GND.
I_{DD}	Positive Supply Current
I_{SS}	Negative Supply Current
GND	Ground (0 V) Reference
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
IN	Logic Control Input
$V_D (V_S)$	Analog Voltage on Terminals D and S
R_{ON}	Ohmic Resistance between D and S
ΔR_{ON}	On Resistance Match between any two channels, i.e., $R_{ONmax} - R_{ONmin}$
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
$I_S (OFF)$	Source Leakage Current with the Switch OFF
$I_D (OFF)$	Drain Leakage Current with the Switch OFF
$I_D, I_S (ON)$	Channel Leakage Current with the Switch ON
V_{INL}	Maximum Input Voltage for Logic “0”
V_{INH}	Minimum Input Voltage for Logic “1”
$I_{INL}(I_{INH})$	Input Current of the Digital Input
$C_S (OFF)$	OFF Switch Source Capacitance. Measured with reference to ground.
$C_D (OFF)$	OFF Switch Drain Capacitance. Measured with reference to ground.
$C_D, C_S(ON)$	ON Switch Capacitance. Measured with reference to ground.
C_{IN}	Digital Input Capacitance
$t_{TRANSITION}$	Delay Time Measured between the 50% and 90% Points of the Digital Inputs and the Switch ON Condition when Switching from One Address State to Another
$t_{ON}(\overline{EN})$	Delay Time between the 50% and 90% Points of the $\overline{EN}$ Digital Input and the Switch ON Condition
$t_{OFF}(\overline{EN})$	Delay Time between the 50% and 90% Points of the $\overline{EN}$ Digital Input and the Switch OFF Condition
t_{OPEN}	OFF Time Measured between the 80% Points of Both Switches when Switching from One Address State to Another
Charge Injection	A Measure of the Glitch Impulse Transferred from the Digital Input to the Analog Output During Switching
OFF Isolation	A Measure of Unwanted Signal Coupling through an OFF Switch
Crosstalk	A Measure of Unwanted Signal Coupling from One Channel to Another as a Result of Parasitic Capacitance
ON Response	The Frequency Response of the ON Switch
Insertion Loss	The Loss Due to the On Resistance of the Switch

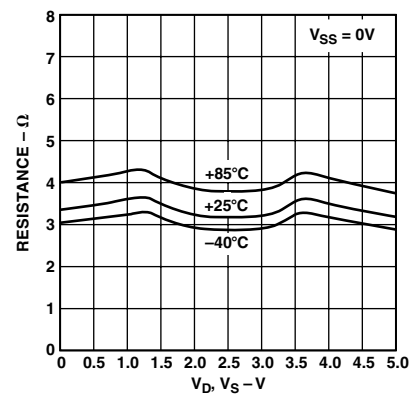
Typical Performance Characteristics—ADG726/ADG732



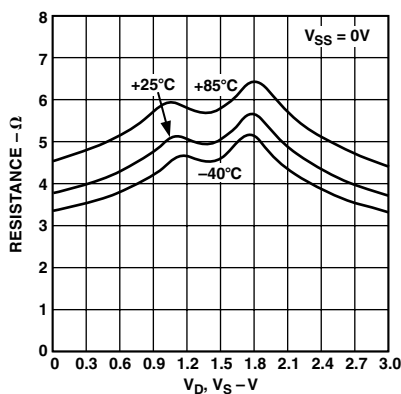
TPC 1. On Resistance vs. $V_D(V_S)$, Single Supply



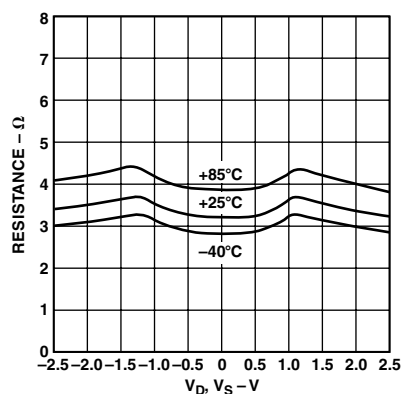
TPC 2. On Resistance vs. $V_D(V_S)$, Dual Supply



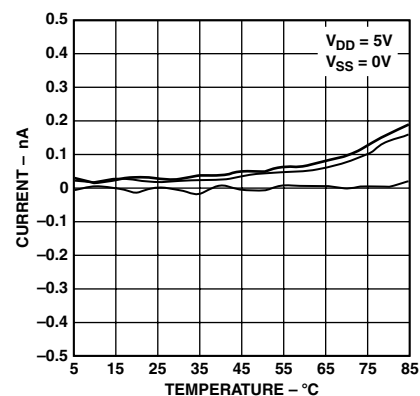
TPC 3. On Resistance vs. $V_D(V_S)$ for Different Temperatures, Single Supply



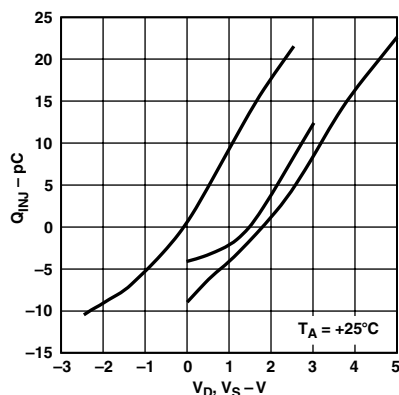
TPC 4. On Resistance vs. $V_D(V_S)$, Single Supply



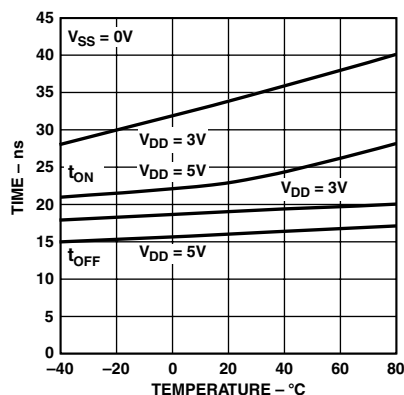
TPC 5. On Resistance vs. $V_D(V_S)$, Dual Supply



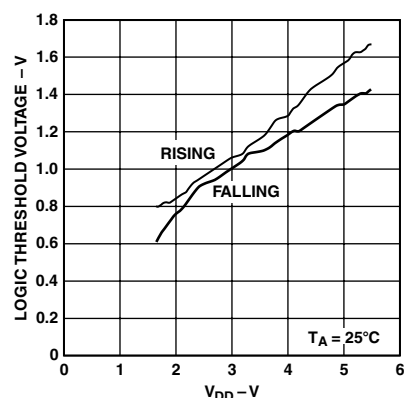
TPC 6. Leakage Currents vs. Temperature



TPC 7. ADG732 Charge Injection vs. Source Voltage

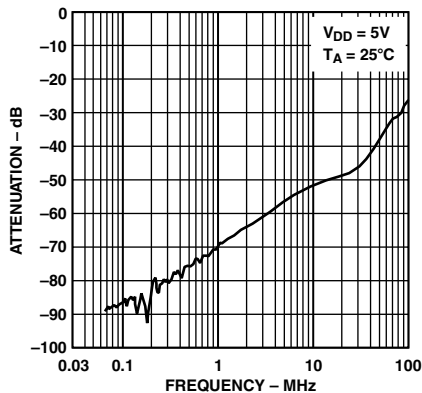


TPC 8. t_{ON}/t_{OFF} Times vs. Temperature

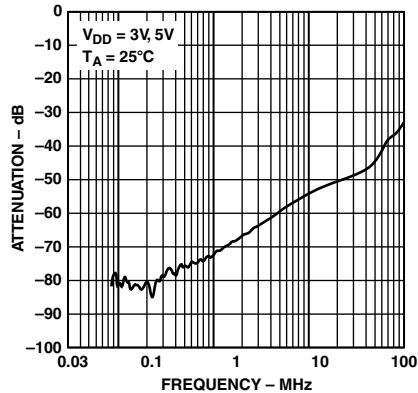


TPC 9. Logic Threshold Voltage vs. Supply Voltage

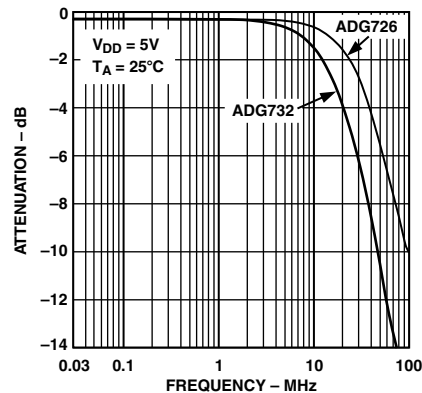
ADG726/ADG732



TPC 10. OFF Isolation vs. Frequency

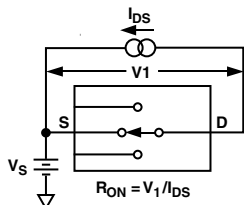


TPC 11. Crosstalk vs. Frequency

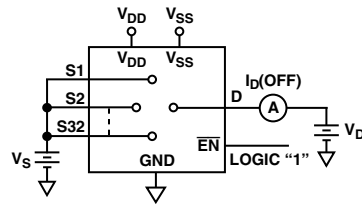


TPC 12. ON Response vs. Frequency

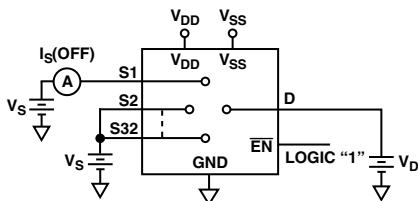
Test Circuits



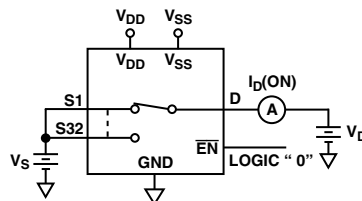
Test Circuit 1. On Resistance



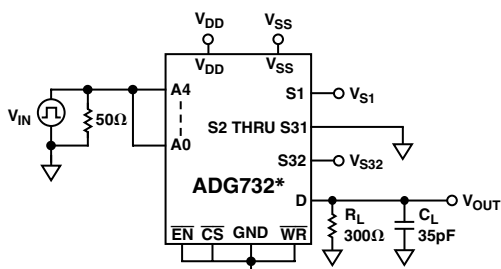
Test Circuit 3. I_D (OFF)



Test Circuit 2. I_S (OFF)

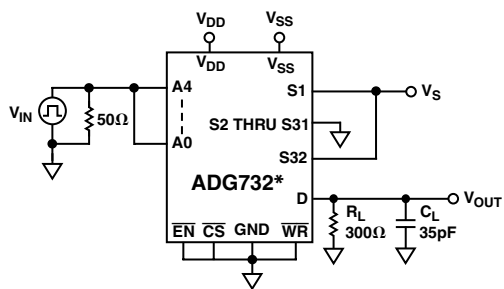


Test Circuit 4. I_D (ON)



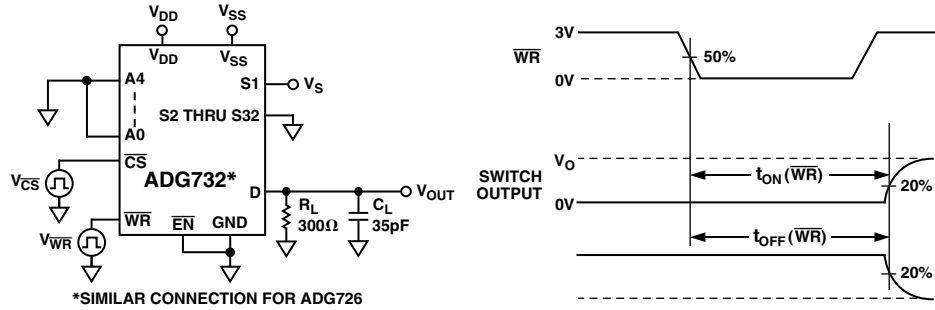
*SIMILAR CONNECTION FOR ADG726

Test Circuit 5. Switching Time of Multiplexer, $t_{\text{TRANSITION}}$

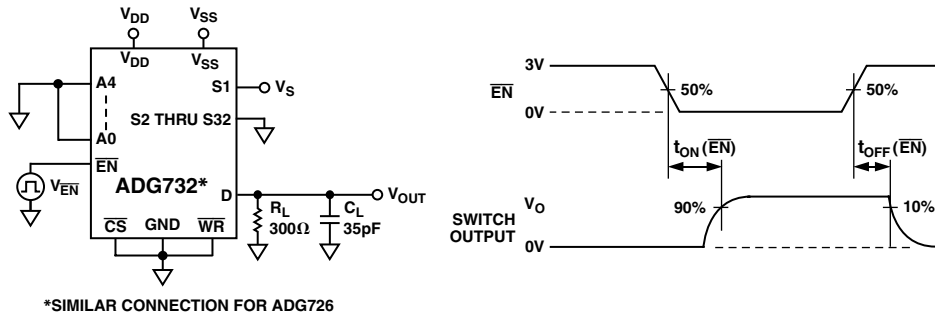


*SIMILAR CONNECTION FOR ADG726

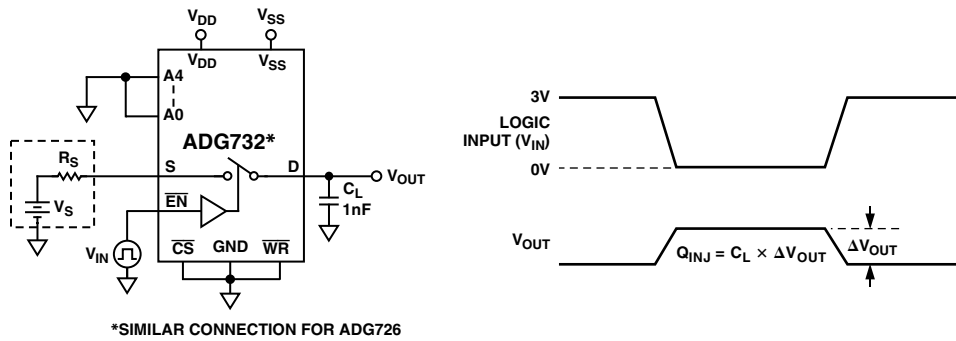
Test Circuit 6. Break-Before-Make Delay, t_{OPEN}



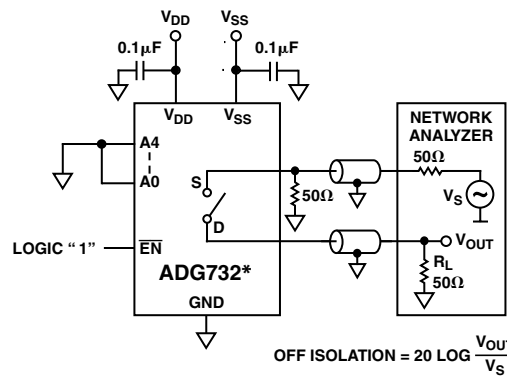
Test Circuit 7. Write Turn-ON and Turn-OFF Time, t_{ON} , $t_{OFF}(\overline{WR})$



Test Circuit 8. Enable Delay, $t_{ON}(\overline{EN})$, $t_{OFF}(\overline{EN})$

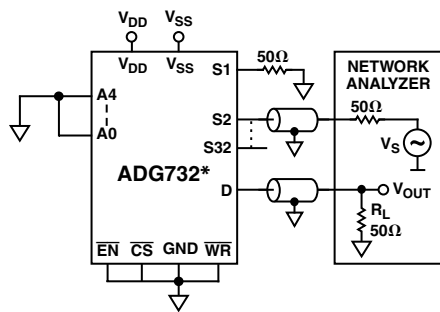


Test Circuit 9. Charge Injection



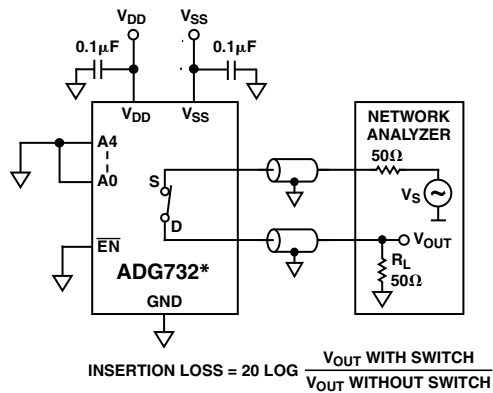
Test Circuit 10. OFF Isolation

ADG726/ADG732



***SIMILAR CONNECTION FOR ADG726**
CHANNEL-TO-CHANNEL CROSSTALK = $20\text{LOG}_{10} (V_{\text{OUT}}/V_S)$

Test Circuit 11. Channel-to-Channel Crosstalk



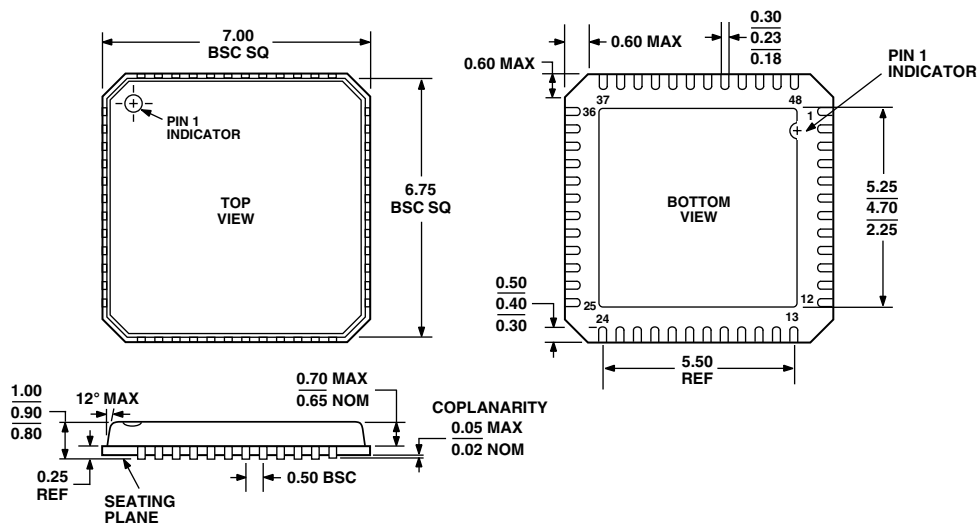
***SIMILAR CONNECTION FOR ADG726**

Test Circuit 12. Bandwidth

OUTLINE DIMENSIONS

48-Lead Frame Chip Scale Package [LFCSP] (CP-48)

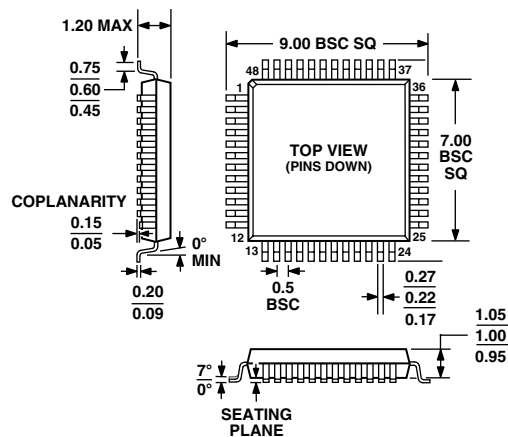
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VKGD-2

48-Lead Thin Plastic Quad Flatpack [TQFP] (SU-48)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026BBC