CMOS ±5 V/+5 V 4 Ω Single SPDT Switches

ADG619/ADG620

FEATURES

6.5 Ω (max) on resistance
0.8 Ω (max) on-resistance flatness
2.7 V to 5.5 V single supply
±2.7 V to ±5.5 V dual supply
Rail-to-rail operation
8-lead SOT-23 package, 8-lead MSOP package
Typical power consumption (<0.1 µW)
TTL/CMOS compatible inputs

FUNCTIONAL BLOCK DIAGRAM

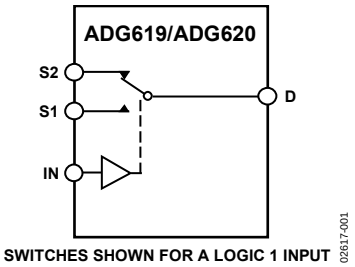


Figure 1.

APPLICATIONS

Automatic test equipment
Power routing
Communication systems
Data acquisition systems
Sample-and-hold systems
Avionics
Relay replacement
Battery-powered systems

GENERAL DESCRIPTION

The ADG619/ADG620 are monolithic, CMOS single-pole, double-throw (SPDT) switches. Each switch conducts equally well in both directions when on.

The ADG619/ADG620 offer low on resistance of 4 Ω, which is matched to within 0.7 Ω between channels. These switches also provide low power dissipation, yet give high switching speeds. The ADG619 exhibits break-before-make switching action, thus preventing momentary shorting when switching channels. The ADG620 exhibits make-before-break action.

The ADG619/ADG620 are available in an 8-lead SOT-23 package and an 8-lead MSOP package.

PRODUCT HIGHLIGHTS

1. Low On resistance (R_{ON}): 4 Ω typ.
2. Dual ±2.7 V to ±5.5 V or single 2.7 V to 5.5 V supply.
3. Low power dissipation. CMOS construction ensures low power dissipation.
4. Fast t_{ON}/t_{OFF}.
5. Tiny 8-lead SOT-23 package and 8-lead MSOP package.

Table 1. Truth Table for the ADG619/ADG620

IN	Switch S1	Switch S2
0	ON	OFF
1	OFF	ON

Rev. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

1/06—Rev. A to Rev. B

Changes to R_{ON} Values in Table 2 2
Updated Outline Dimensions 13
Changes to Ordering Guide 13

6/03—Rev. 0 to Rev. A.

Edits to Specifications 2
Changes to Ordering Guide 4
Updated Outline Dimensions 8

SPECIFICATIONS

DUAL SUPPLY[1]

V_{DD} = +5 V ± 10%, V_{SS} = −5 V ± 10%, GND = 0 V. All specifications −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter	B Version +25°C	−40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	V_{DD} = +4.5 V, V_{SS} = −4.5 V
On Resistance (R_{ON})	4		Ω typ	V_S = ±4.5 V, I_S = −10 mA, Figure 15
	6.5	8.5	Ω max	
On Resistance Match Between Channels (ΔR_{ON})	0.7		Ω typ	V_S = ±4.5 V, I_S = −10 mA
	1.1	1.35	Ω max	
On Resistance Flatness ($R_{FLAT (ON)}$)	0.7	0.8	Ω typ	V_S = ±3.3 V, I_S = −10 mA
	1.15	1.2	Ω max	
LEAKAGE CURRENTS				V_{DD} = +5.5 V, V_{SS} = −5.5 V
Source Off Leakage I_S (Off)	±0.01		nA typ	V_S = ±4.5 V, V_D = ∓4.5 V, Figure 16
	±0.25	±1	nA max	
Channel On Leakage I_D, I_S (On)	±0.01		nA typ	V_S = V_D = ±4.5 V; Figure 17
	±0.25	±1	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
C_{IN}, Digital Input Capacitance	2		pF typ	
DYNAMIC CHARACTERISTICS[2]				
ADG619				
t_{ON}	80		ns typ	R_L = 300 Ω, C_L = 35 pF
	120	155	ns max	V_S = 3.3 V; Figure 18
t_{OFF}	45		ns typ	R_L = 300 Ω, C_L = 35 pF
	75	90	ns max	V_S = 3.3 V; Figure 18
Break-Before-Make Time Delay, t_{BBM}	40		ns typ	R_L = 300 Ω, C_L = 35 pF
		10	ns min	V_{S1} = V_{S2} = 3.3 V; Figure 19
ADG620				
t_{ON}	40		ns typ	R_L = 300 Ω, C_L = 35 pF
	65	85	ns max	V_S = 3.3 V; Figure 18
t_{OFF}	200		ns typ	R_L = 300 Ω, C_L = 35 pF
	330	400	ns max	V_S = 3.3 V; Figure 18
Make-Before-Break Time Delay, t_{MBB}	160		ns typ	R_L = 300 Ω, C_L = 35 pF
		10	ns min	V_S = 0 V; Figure 20
Charge Injection	110		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, Figure 21
Off Isolation	−67		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, Figure 22
Channel-to-Channel Crosstalk	−67		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, Figure 23
Bandwidth −3 dB	190		MHz typ	R_L = 50 Ω, C_L = 5 pF; Figure 24
C_S (Off)	25		pF typ	f = 1 MHz
C_D, C_S (On)	95		pF typ	f = 1 MHz

Parameter	B Version +25°C	B Version −40°C to +85°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS				V_{DD} = +5.5 V, V_{SS} = −5.5 V
I_{DD}	0.001		µA typ	Digital inputs = 0 V or 5.5 V
		1.0	µA max	
I_{SS}	0.001		µA typ	Digital inputs = 0 V or 5.5 V
		1.0	µA max	

[1] Temperature range for B version is −40°C to +85°C.
[2] Guaranteed by design, not subject to production test.

SINGLE SUPPLY[1]

V_{DD} = +5 V ± 10%, V_{SS} = 0 V, GND = 0 V. All specifications –40°C to +85°C, unless otherwise noted.

Table 3.

Parameter	B Version +25°C	B Version –40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	V_{DD} = 4.5 V, V_{SS} = 0 V
On Resistance (R_{ON})	7		Ω typ	V_S = 0 V to 4.5 V, I_S = –10 mA, Figure 15
	10	12.5	Ω max	
On Resistance Match Between Channels (ΔR_{ON})	0.8		Ω typ	V_S = 0 V to 4.5 V, I_S = –10mA
	1.1	1.3	Ω max	
On Resistance Flatness ($R_{FLAT (ON)}$)	0.5	0.5	Ω typ	V_S = 1.5 V to 3.3 V, I_S = –10 mA
		1	Ω max	
LEAKAGE CURRENTS				V_{DD} = 5.5 V
Source Off Leakage I_S (Off)	±0.01		nA typ	V_S = 1 V/4.5 V; V_D = 4.5 V/1 V, Figure 16
	±0.25	±1	nA max	
Channel On Leakage I_D, I_S (On)	±0.01		nA typ	V_S = V_D = 1 V/4.5 V, Figure 17
	±0.25	±1	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
C_{IN}, Digital Input Capacitance	2		pF typ	
DYNAMIC CHARACTERISTICS[2]				
ADG619				
t_{ON}	120		ns typ	R_L = 300 Ω, C_L = 35 pF
	220	280	ns max	V_S = 3.3 V; Figure 18
t_{OFF}	50		ns typ	R_L = 300 Ω, C_L = 35 pF
	75	110	ns max	V_S = 3.3 V; Figure 18
Break-Before-Make Time Delay, t_{BBM}	70		ns typ	R_L = 300 Ω, C_L = 35 pF
		10	ns min	V_{S1} = V_{S2} = 3.3 V; Figure 19
ADG620				
t_{ON}	50		ns typ	R_L = 300 Ω, C_L = 35 pF
	85	110	ns max	V_S = 3.3 V; Figure 18
t_{OFF}	210		ns typ	R_L = 300 Ω, C_L = 35 pF
	340	420	ns max	V_S = 3.3 V; Figure 18
Make-Before-Break Time Delay, t_{MBB}	170		ns typ	R_L = 300 Ω, C_L = 35 pF
		10	ns min	V_S = 3.3 V; Figure 20
Charge Injection	6		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; Figure 21
Off Isolation	–67		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 22
Channel-to-Channel Crosstalk	–67		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 23
Bandwidth –3 dB	190		MHz typ	R_L = 50 Ω, C_L = 5 pF; Figure 24
C_S (OFF)	25		pF typ	f = 1 MHz
C_D, C_S (ON)	95		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = 5.5 V
I_{DD}	0.001		μA typ	Digital inputs = 0 V or 5.5 V
		1.0	μA max	

[1] Temperature range for B version is –40°C to +85°C
[2] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

TA = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to V_{SS}	13 V
V_{DD} to GND	−0.3 V to +6.5 V
V_{SS} to GND	+0.3 V to −6.5 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V
Digital Inputs[1]	−0.3 V to V_{DD} + 0.3 V or 30 mA (whichever occurs first)
Peak Current, S or D	100 mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current, S or D	50 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
MSOP Package	
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	44°C/W
SOT-23 Package	
θ_{JA} Thermal Impedance	229.6°C/W
θ_{JC} Thermal Impedance	91.99°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature	220°C

[1] Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

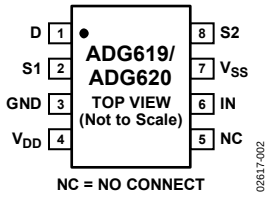


Figure 2. 8-Lead SOT-23 (RT-8)

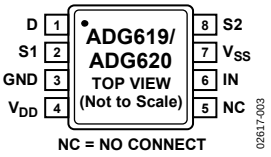


Figure 3. 8-Lead MSOP (RM-8)

Table 5.

Pin No.	Mnemonic	Description
1	D	Drain Terminal. May be an input or output.
2	S1	Source Terminal. May be an input or output.
3	GND	Ground (0 V) Reference.
4	V_{DD}	Most positive power supply pin.
5	NC	Not internally connected.
6	IN	Logic Control Input Pin.
7	V_{SS}	Most negative power supply pin in a dual-supply application. In single-supply applications, this pin should be tied to ground at the device.
8	S2	Source Terminal. May be an input or output.

TYPICAL PERFORMANCE CHARACTERISTICS

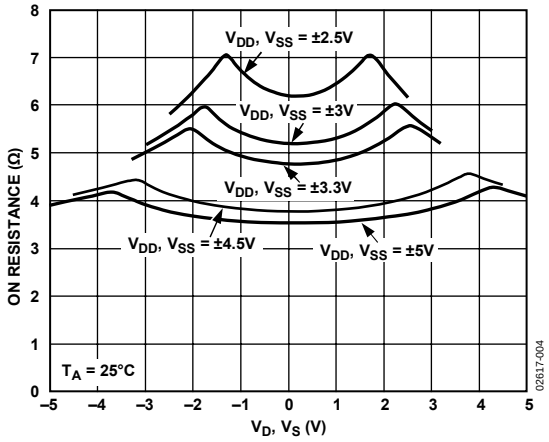


Figure 4. On Resistance vs. V_D (V_S) (Dual Supply)

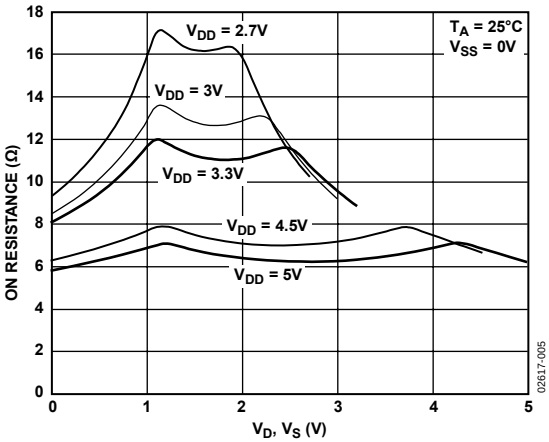


Figure 5. On Resistance vs. V_D (V_S) (Single Supply)

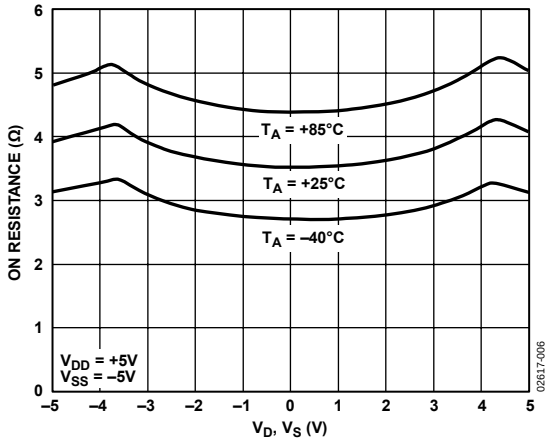


Figure 6. On Resistance vs. V_D (V_S) for Different Temperatures (Dual Supply)

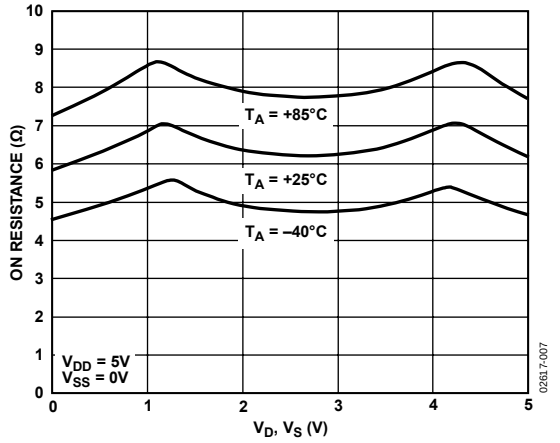


Figure 7. On Resistance vs. V_D (V_S) for Different Temperatures (Single Supply)

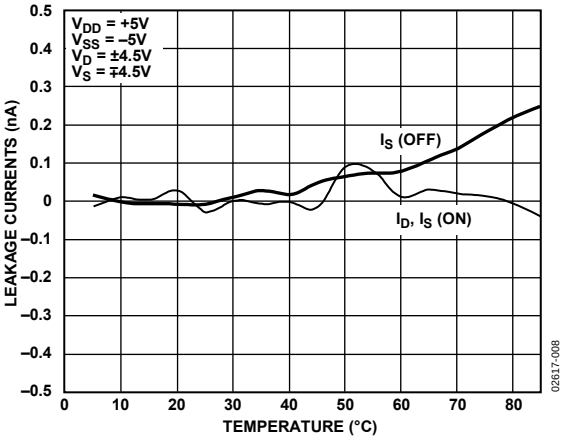


Figure 8. Leakage Currents vs. Temperature (Dual Supply)

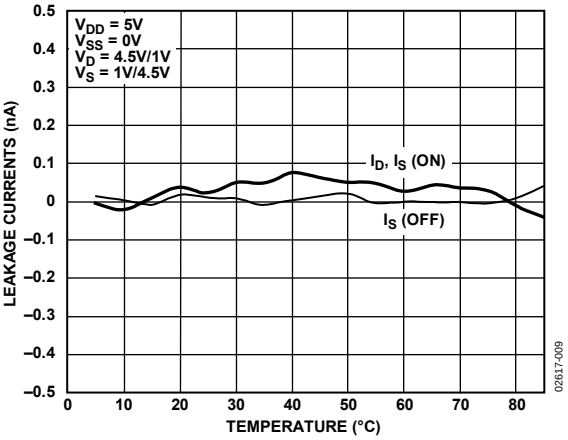


Figure 9. Leakage Currents vs. Temperature (Single Supply)

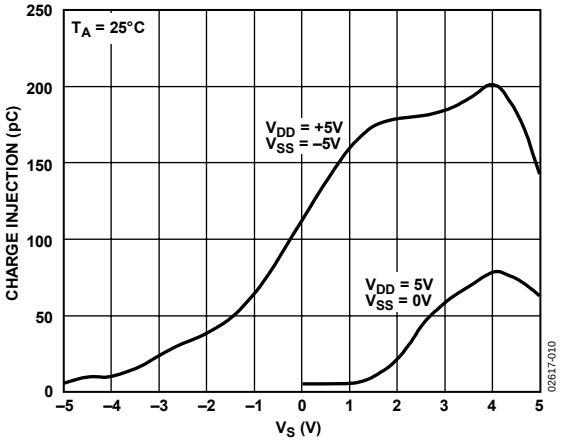


Figure 10. Charge Injection vs. Source Voltage

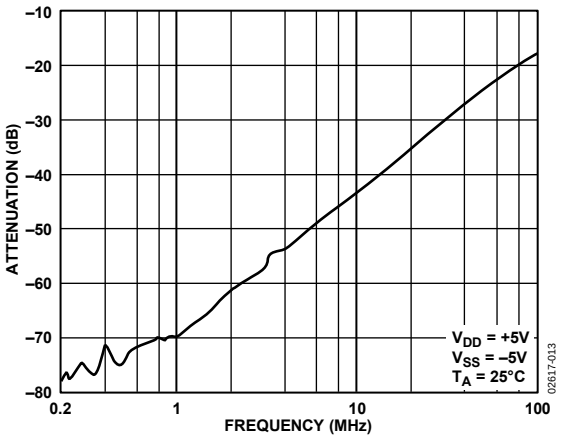


Figure 13. Crosstalk vs. Frequency

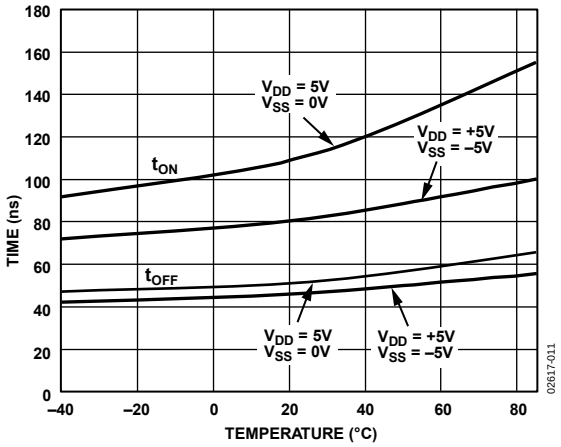


Figure 11. t_{ON}/t_{OFF} Times vs. Temperatures

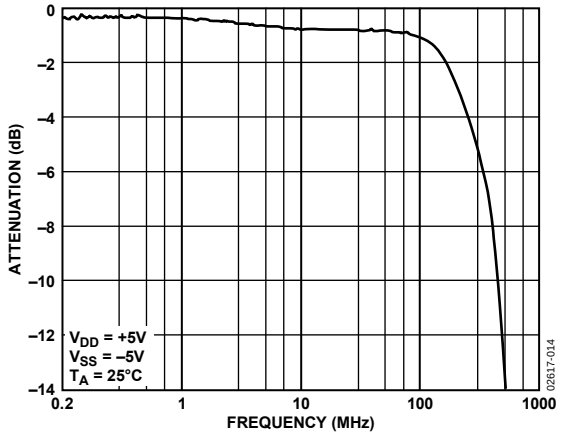


Figure 14. On Response vs. Frequency

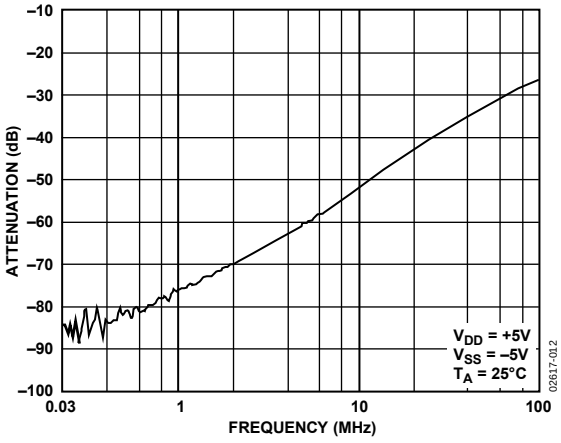


Figure 12. Off Isolation vs. Frequency

TERMINOLOGY

Table 6.

Mnemonic	Description
I_{DD}	Positive Supply Current.
I_{SS}	Negative Supply Current.
R_{ON}	Ohmic resistance between D and S.
ΔR_{ON}	On resistance match between any two channels, that is, R_{ON} Max − R_{ON} Min.
$R_{FLAT (ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
I_S (Off)	Source leakage current with the switch off.
I_D, I_S (On)	Channel leakage current with the switch on.
V_D (V_S)	Analog voltage on Terminals D, S.
V_{INL}	Maximum Input voltage for Logic 0.
V_{INH}	Minimum input voltage for Logic 1.
I_{INL} (I_{INH})	Input current of the digital input.
C_S (Off)	Off switch source capacitance.
C_D, C_S (On)	On switch capacitance.
t_{ON}	Delay between applying the digital control input and the output switching on.
t_{OFF}	Delay between applying the digital control input and the output switching off.
t_{MBB}	On time is measured between the 80% points of both switches, when switching from one address state to another.
t_{BBM}	Off time or On time is measured between the 90% points of both switches, when switching from one address state to another.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Crosstalk	A measure of unwanted signal coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an off switch.
Bandwidth	The frequency response of the on switch.
Insertion Loss	The loss due to the on resistance of the switch.

TEST CIRCUITS

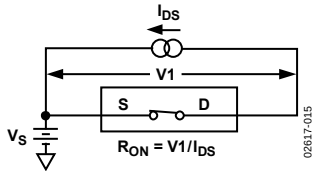


Figure 15. On Resistance

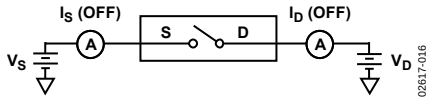


Figure 16. Off Leakage

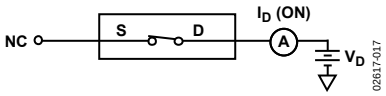


Figure 17. On Leakage

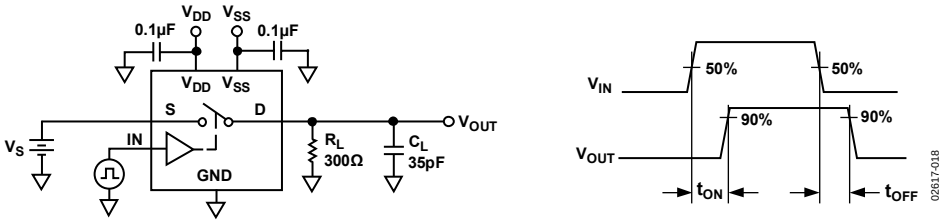


Figure 18. Switching Times

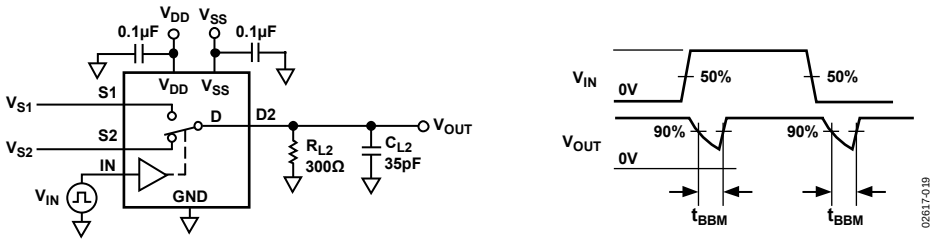


Figure 19. Break-Before-Make Time Delay, t_{BBM} (ADG619 Only)

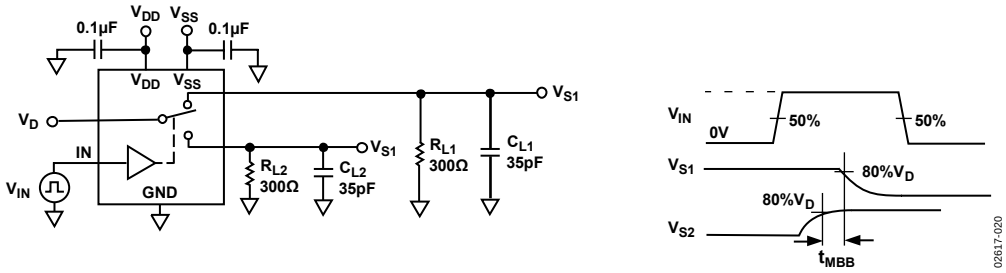


Figure 20. Make-Before-Break Time Delay, t_{MBB} (ADG620 Only)

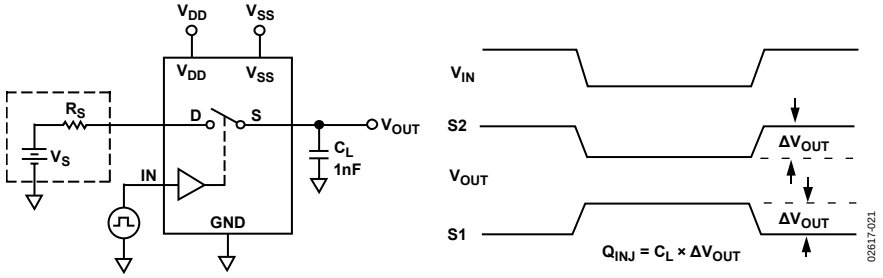


Figure 21. Charge Injection

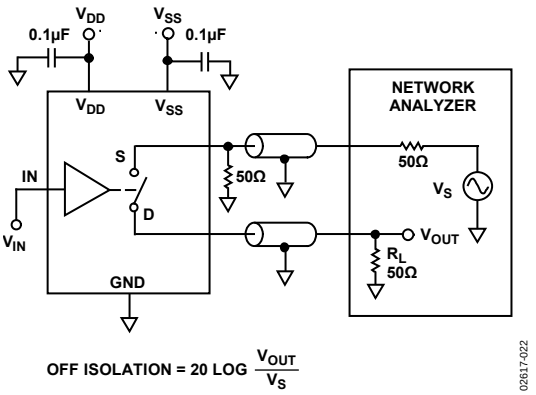


Figure 22. Off Isolation

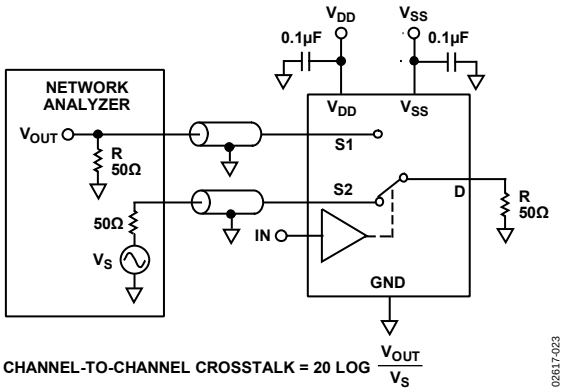


Figure 23. Channel-to-Channel Crosstalk

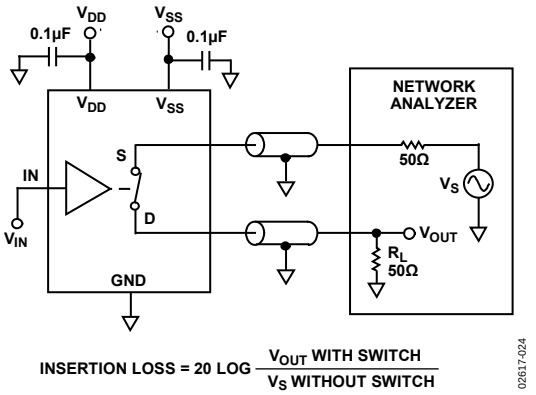
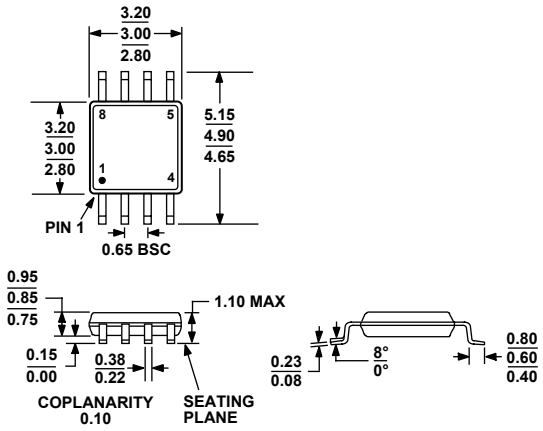


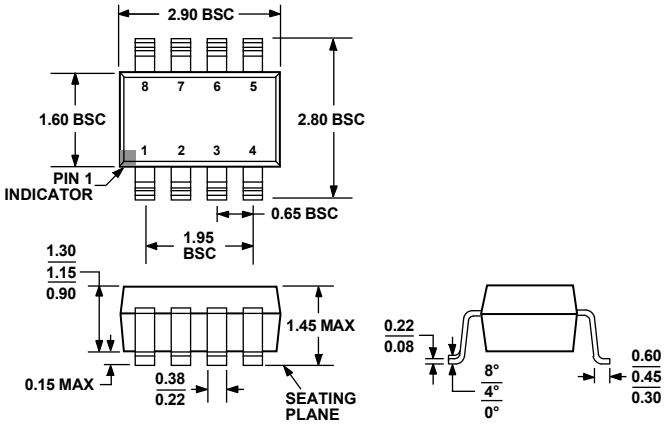
Figure 24. Bandwidth

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 25. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-178-BA

Figure 26. 8-Lead Small Outline Transistor Package [SOT-23]
(RT-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding[1]
ADG619BRM	−40°C to +85°C	8-Lead Mini Small Outline Package (MSOP)	RM-8	SVB
ADG619BRM-REEL	−40°C to +85°C	8-Lead Mini Small Outline Package (MSOP)	RM-8	SVB
ADG619BRM-REEL7	−40°C to +85°C	8-Lead Mini Small Outline Package (MSOP)	RM-8	SVB
ADG619BRMZ[2]	−40°C to +85°C	8-Lead Mini Small Outline Package (MSOP)	RM-8	SCC
ADG619BRMZ-REEL[2]	−40°C to +85°C	8-Lead Mini Small Outline Package (MSOP)	RM-8	SCC
ADG619BRMZ-REEL7[2]	−40°C to +85°C	8-Lead Mini Small Outline Package (MSOP)	RM-8	SCC
ADG619BRT-REEL	−40°C to +85°C	8-Lead Small Outline Transistor Package (SOT-23)	RT-8	SVB
ADG619BRT-REEL7	−40°C to +85°C	8-Lead Small Outline Transistor Package (SOT-23)	RT-8	SVB
ADG619BRT-500RL7	−40°C to +85°C	8-Lead Small Outline Transistor Package (SOT-23)	RT-8	SVB
ADG619BRTZ-REEL[2]	−40°C to +85°C	8-Lead Small Outline Transistor Package (SOT-23)	RT-8	SCC
ADG619BRTZ-REEL7[2]	−40°C to +85°C	8-Lead Small Outline Transistor Package (SOT-23)	RT-8	SCC
ADG619BRTZ-500RL7[2]	−40°C to +85°C	8-Lead Small Outline Transistor Package (SOT-23)	RT-8	SCC
ADG620BRM	−40°C to +85°C	8-Lead Mini Small Outline Package (MSOP)	RM-8	SWB
ADG620BRM-REEL	−40°C to +85°C	8-Lead Mini Small Outline Package (MSOP)	RM-8	SWB
ADG620BRM-REEL7	−40°C to +85°C	8-Lead Mini Small Outline Package (MSOP)	RM-8	SWB
ADG620BRMZ[2]	−40°C to +85°C	8-Lead Mini Small Outline Package (MSOP)	RM-8	S21
ADG620BRT-REEL	−40°C to +85°C	8-Lead Small Outline Transistor Package (SOT-23)	RT-8	SWB
ADG620BRT-REEL7	−40°C to +85°C	8-Lead Small Outline Transistor Package (SOT-23)	RT-8	SWB
ADG620BRTZ-REEL7[2]	−40°C to +85°C	8-Lead Small Outline Transistor Package (SOT-23)	RT-8	S21

[1] Branding on SOT-23 and MSOP packages is limited to three characters due to space constraints.
[2] Z= Pb-free part.

NOTES

NOTES

C02617-0-1/06(B)