TFT-LCD Module Specification

Module NO.: VRC160160-COG1

☐ APPROVAL FOR SPECIFICATION ☐ APPROVAL FOR SAMPLE

For Customer’s Acceptance：	
Approved by	**Comment**

Team Source Display：		
Presented by	**Reviewed by**	**Organized by**

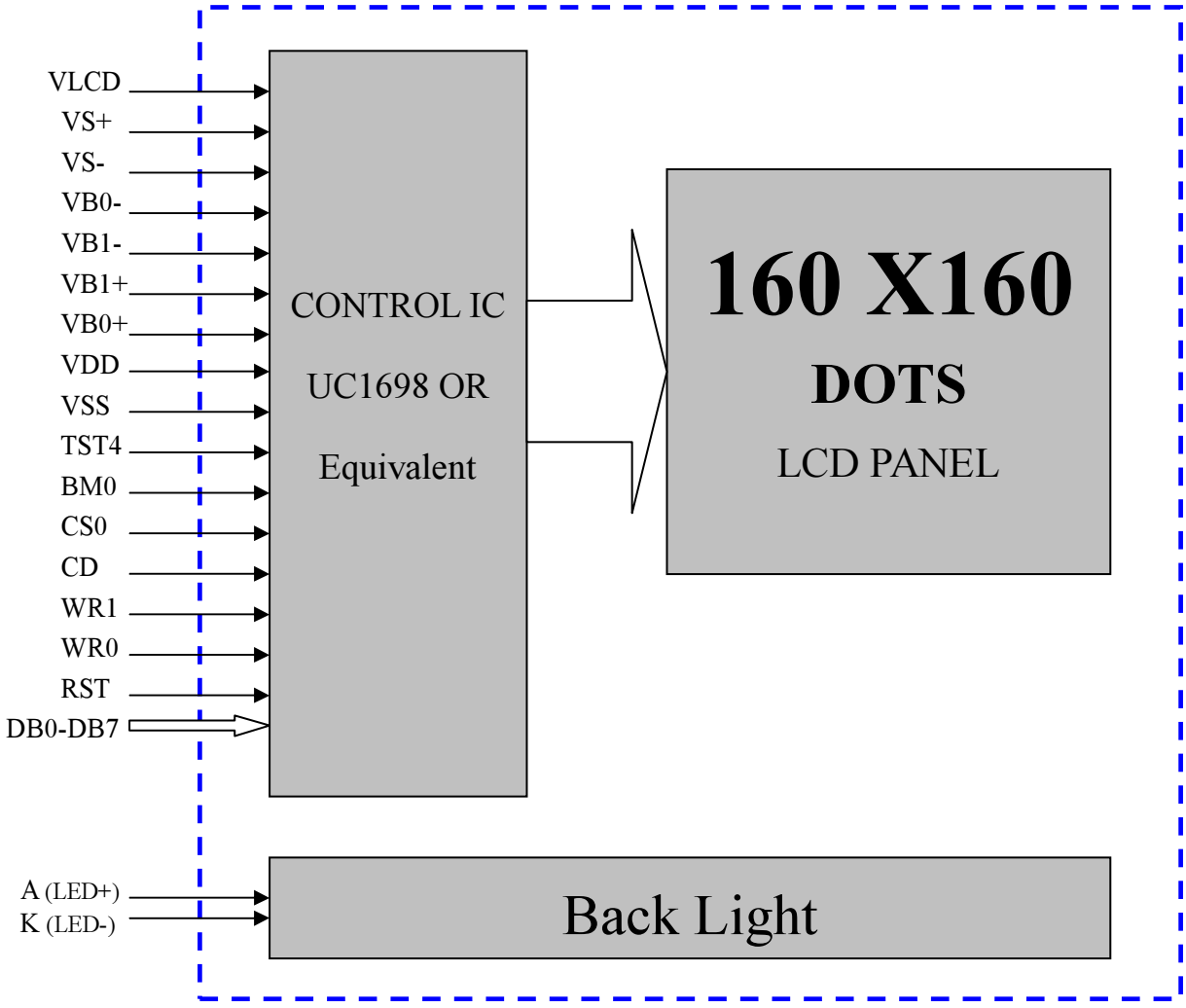
Version No.	Date	Content	Remark
V1.0	2017-7-10	Initial Release	

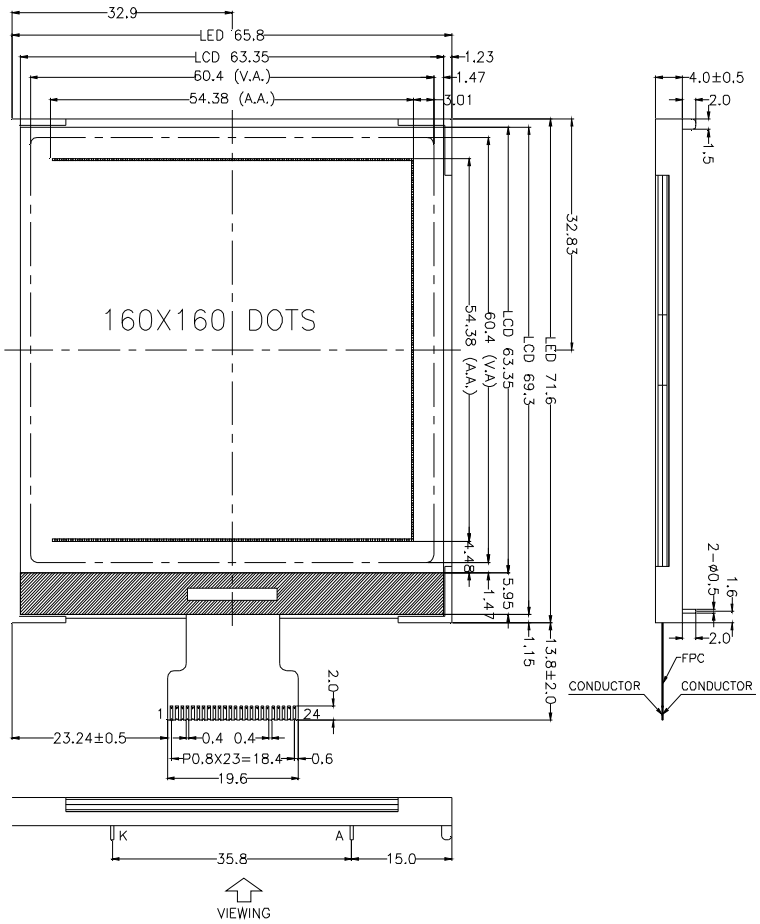
CONTENTS

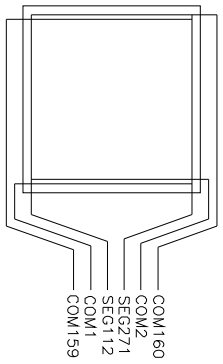
FUNCTIONS & FEA ¨URES

- Construction : COG (Chip-on-Glass)
- Display Format : 160x160 dots
- Display Type : FSTN, Transflective, Positive, B-W
- Controller : UC1698 or equivalent controller
- Interface : 6800/8080 mode 8-bit parallel interface
- Backlight : white/side light
- Viewing Direction : 6 O'clock
- Driving Scheme : 1/160 Duty Cycle, 1/10 Bias
- Power Supply Voltage : 3.3 V
- V_{LCD} Adjustable For Best Contrast : 16.5 V ($V_{OP.}$)
- Operation temperature : -20℃ to +70℃
- Storage temperature : -30℃ to +80℃

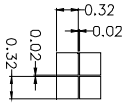
BLOCK DIAGRAM







LOGIC



DETAIL DOTS
SCALE:10:1

INTERFACE PIN FUNCTIONS

8080/8-Bit interface:

Pin No.	Symbol	Level	Description
1	VLCD	--	High voltage LCD Power supply.
2	VS+	--	LCD SEG driving voltages. These are voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of CBX value between VBX+ and VBX-. Connect a 150~220 nF/25v capacitor between VS+ and VS-. The resistance of these traces directly affects the driving strength of SEG electrodes and impacts the image of the LCD module. Minimize the trace resistance is critical in achieving high quality image.
3	VS-	--	
4	VB0-	--	
5	VB1-	--	
6	VB1+	--	
7	VB0+	--	
8	VDD	+3.3V	Supply voltage for logic operating.
9	VSS	0V	Ground
10	TST4	--	Test control. This pin has on-chip pull-up resistor. Leave it open during normal operation. TST4 is also used as one of the high voltage power supply for MTP programming operation. For COG designs, please wire out TST4 with trace resistance between 30~50Ω.
11	BM0	L	Bus mode: The interface bus mode is determined by BM0. When the BM0 is LOW, the mode is 8080/8-bit mode.
12	CS0	L	Chip select. Chip is selected when CS0="L". When the chip is not selected, D [7:0] will be high impedance.
13	CD	H/L	Selects control data or display data for read/ write operation. "L": Control command "H": Display data
14	WR1	H/L	In 8080 parallel mode, this pin is used as Read.
15	WR0	H/L	In 8080 parallel mode, this pin is used as Write.
16	RST	H/L	When RST="L", all control registers are re-initialized by their default states. Since UC1698u has built-in Power-ON reset and software reset commands, RST pin is not required for proper chip operation. An RC Filter has been included on-chip. There is no need for external RC noise filter. When RST is not used, connect the pin to VDD.
17	DB0	H/L	These are 8080/8-bit data bus for data transfer between MPU and UC1698.
18	DB1	H/L	
19	DB2	H/L	
20	DB3	H/L	
21	DB4	H/L	
22	DB5	H/L	
23	DB6	H/L	
24	DB7	H/L	

Pin No.	Symbol	Level	Description
1	A(LED+)	+3.1V	Power supply for Back Light. The current is controlling in the 75mA.
2	K(LED-)	0V	Ground for Back Light.

68000/8-Bit interface:

Pin No.	Symbol	Level	Description
1	VLCD	--	High voltage LCD Power supply.
2	VS+	--	LCD SEG driving voltages. These are voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of CBX value between VBX+ and VBX-. Connect a 150~220 nF/25v capacitor between VS+ and VS-. The resistance of these traces directly affects the driving strength of SEG electrodes and impacts the image of the LCD module. Minimize the trace resistance is critical in achieving high quality image.
3	VS-	--	
4	VB0-	--	
5	VB1-	--	
6	VB1+	--	
7	VB0+	--	
8	VDD	+3.3V	Supply voltage for logic operating.
9	VSS	0V	Ground
10	TST4	--	Test control. This pin has on-chip pull-up resistor. Leave it open during normal operation. TST4 is also used as one of the high voltage power supply for MTP programming operation. For COG designs, please wire out TST4 with trace resistance between 30~50Ω.
11	BM0	H	Bus mode: The interface bus mode is determined by BM0. When the BM0 is High, the mode is 6800/8-bit mode.
12	CS0	L	Chip select. Chip is selected when CS0="L". When the chip is not selected, D [7:0] will be high impedance.
13	CD	H/L	Selects control data or display data for read/ write operation. "L": Control command "H": Display data
14	WR1	H/L	In 6800 parallel mode, this pin is used as Enable.
15	WR0	H/L	In 6800 parallel mode: "L": Write instruction "H": Read data
16	RST	H/L	When RST="L", all control registers are re-initialized by their default states. Since UC1698u has built-in Power-ON reset and software reset commands, RST pin is not required for proper chip operation. An RC Filter has been included on-chip. There is no need for external RC noise filter. When RST is not used, connect the pin to VDD.
17	D0	H/L	These are 6800/8-bit data bus for data transfer between MPU and UC1698.
18	D1	H/L	
19	D2	H/L	
20	D3	H/L	
21	D4	H/L	
22	D5	H/L	
23	D6	H/L	
24	D7	H/L	

Pin No.	Symbol	Level	Description
1	A(LED+)	+3.1V	Power supply for Back Light. The current is controlling in the 75mA.
2	K(LED-)	0V	Ground for Back Light.

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃)

Parameter	Symbol	Min	Max	Unit
Supply voltage for logic	V_{DD}	-0.3	+4.0	V
Supply voltage for LCD	V_o	-0.3	+19.8	V
Input voltage	V_I	-0.4	V_{DD} +0.5	V
Normal Operating temperature	T_{OP}	-30	+80	℃
Normal Storage temperature	T_{ST}	-40	+100	℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	Min	T_{YP}	Max	Unit
Supply voltage for logic	VDD	--	3.0	3.3	3.5	V
Supply current for logic	IDD	--	--	76	85	mA
Operating voltage for LCD	VLCD	-20℃				
		+25℃	16.7	16.9	17.2	V
		+70℃				
Input voltage "H" level	VIH	--	0.8 V_{DD}	-	V_{DD}	V
Input voltage "L" level	VIL	--	0	-	0.2 V_{DD}	V

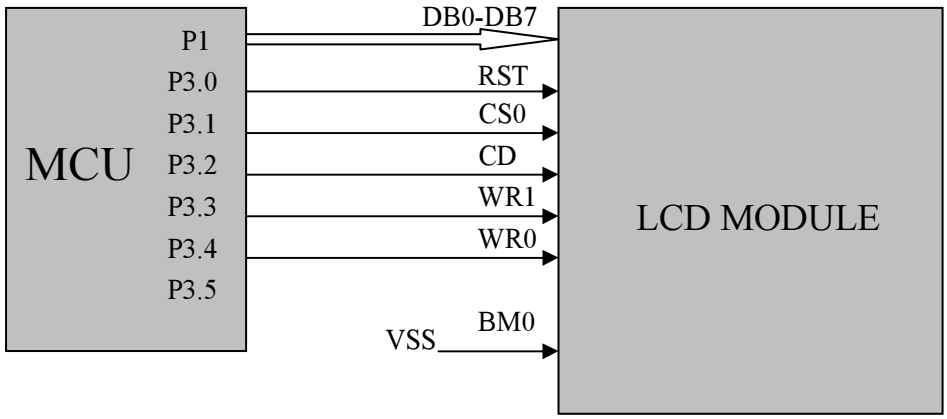
LED BACKLIGHT CHARACTERISTICS

COLOR	Wavelength λp(nm)	Operating Voltage(±0.15V)	Spectral line half width Δλ(nm)	Forward Current (mA)
white	--	3.0	--	75

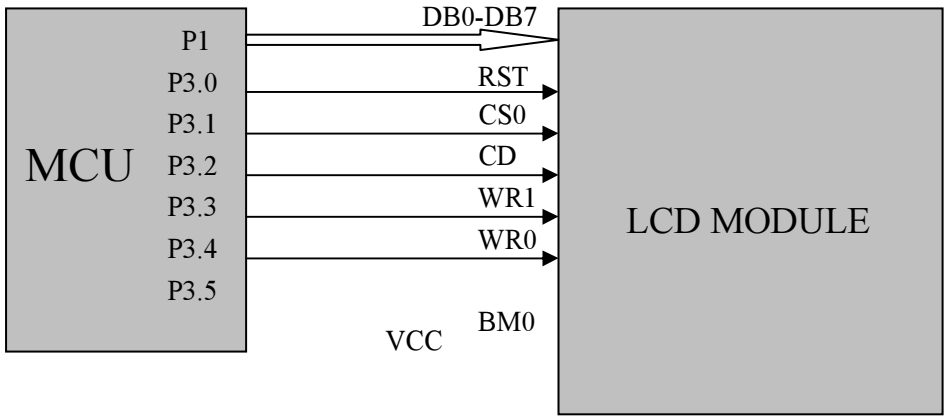
NOTE: Do not connect +5V directly to the backlight terminals. This will ruin the backlight.

CONNECTION WITH MCU

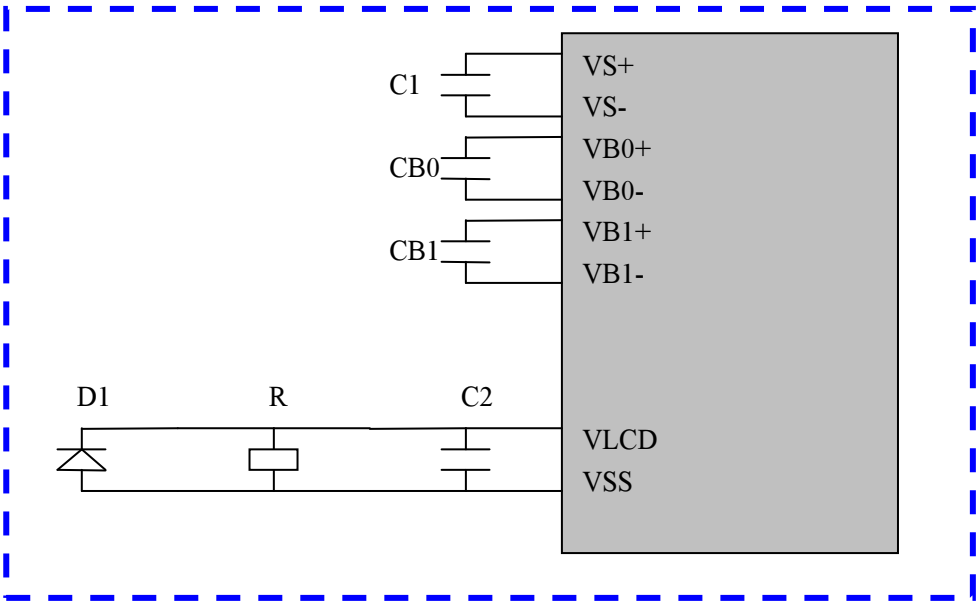
8080/8-Bit interface:



6800/8-Bit interface:



Hi-V generator and Bias reference circuit



Note:

Sample component values: (The illustrated circuit and component values are for reference only. Please optimize for specific requirements of each application.)

CB0~1: 2.2uF/25V or 300x LCD load capacitance, whichever is higher.

C1: 150~220nF/25V or Non-connection.

C2: 0.1uF/50V Package: 0805

D1: 18V TVS, Package: D0-214AA; such as: SMBJ18CA

R: 3.0 MΩ / Package:0805 Power: 1/8

Parallel Interface

The timing relationship between UC1698u internal control signal RD, WR and their associated bus actions are shown in the figure below.

The Display RAM read interface is implemented as a two-stage pipe-line. This architecture requires that, every time memory address is modified, either in 8-bit mode or 16-bit mode, by either *Set CA*, or *Set RA* command, a dummy read cycle needs to be performed before the actual data can propagate through the pipe-line and be read from data port D.

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

16-BIT & 8-BIT BUS OPERATION

UC1698u supports both 8-bit and 16-bit bus width. The bus width is determined by pin BM[1].

8-bit bus operation exactly doubles the clock cycles of 16-bit bus operation, MSB followed by LSB, including the dummy read, which also requires two clock cycles. The bus cycle of 8-bit mode is reset each time CD pin changes state (when CS is active).

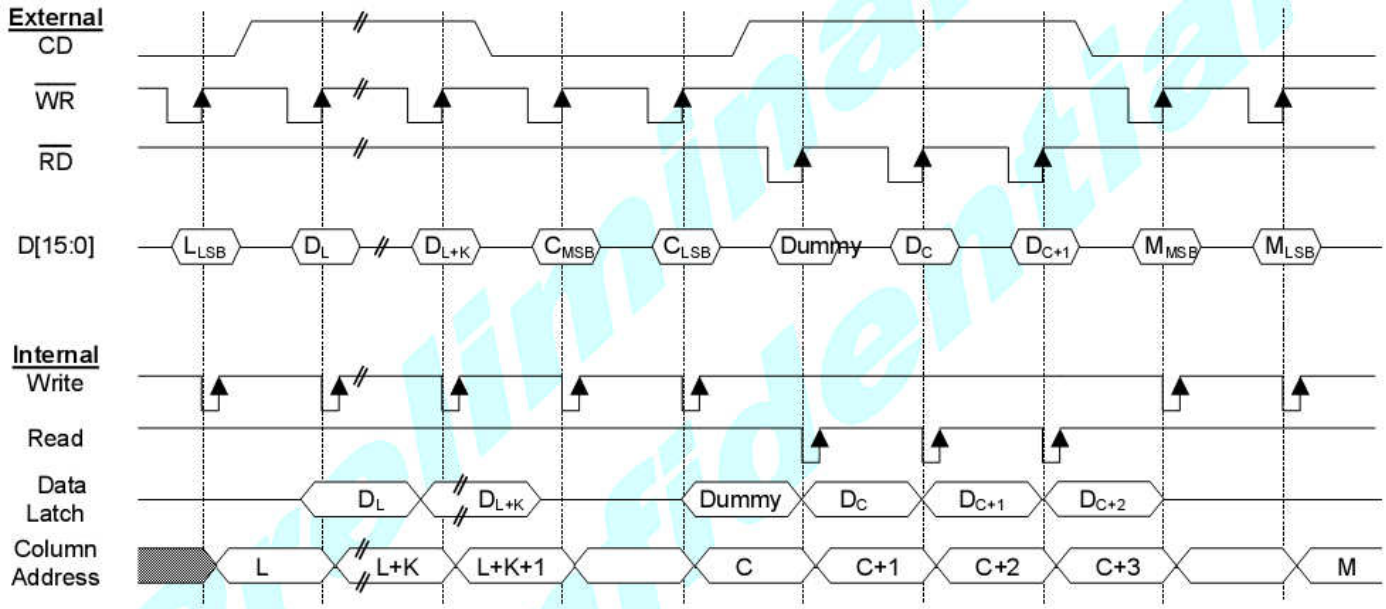


FIGURE 3: 16-bit Parallel Interface & Related Internal Signals

AC CHARACTISTICS

8080/8-Bit interface:

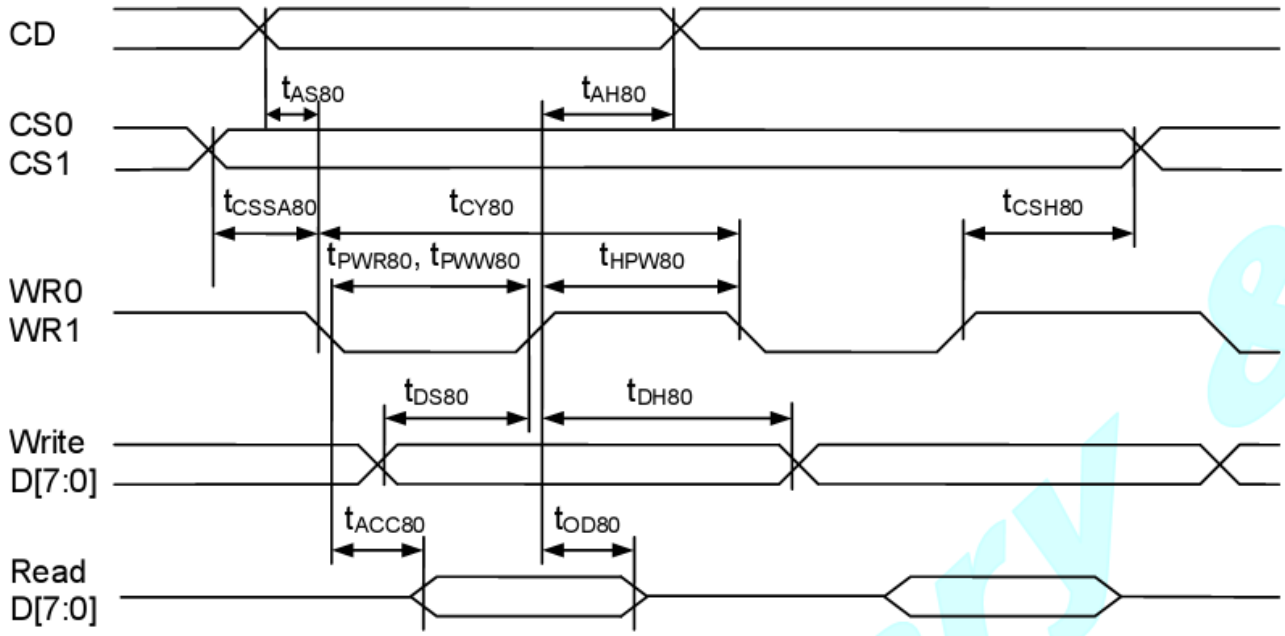


FIGURE 14: Parallel Bus Timing Characteristics (for 8080 MCU)

($2.5V \leqslant V_{DD} < 3.3V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY80}		System cycle time 16-bit bus (read) (write) 8-bit bus (read) (write)		 170 130 100 80	–	nS
t_{PWR80}	WR1	Pulse width 16-bit (read) 8-bit		85 50	–	nS
t_{PWW80}	WR0	Pulse width 16-bit (write) 8-bit		65 40	–	nS
t_{HPW80}	WR0, WR1	High pulse width 16-bit bus (read) (write) 8-bit bus (read) (write)		 85 65 50 40	–	nS
t_{DS80} t_{DH80}	D0~D15	Data setup time Data hold time		30 0	–	nS
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 15	60 30	nS
T_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time		5 5		nS

6800/8-Bit interface:

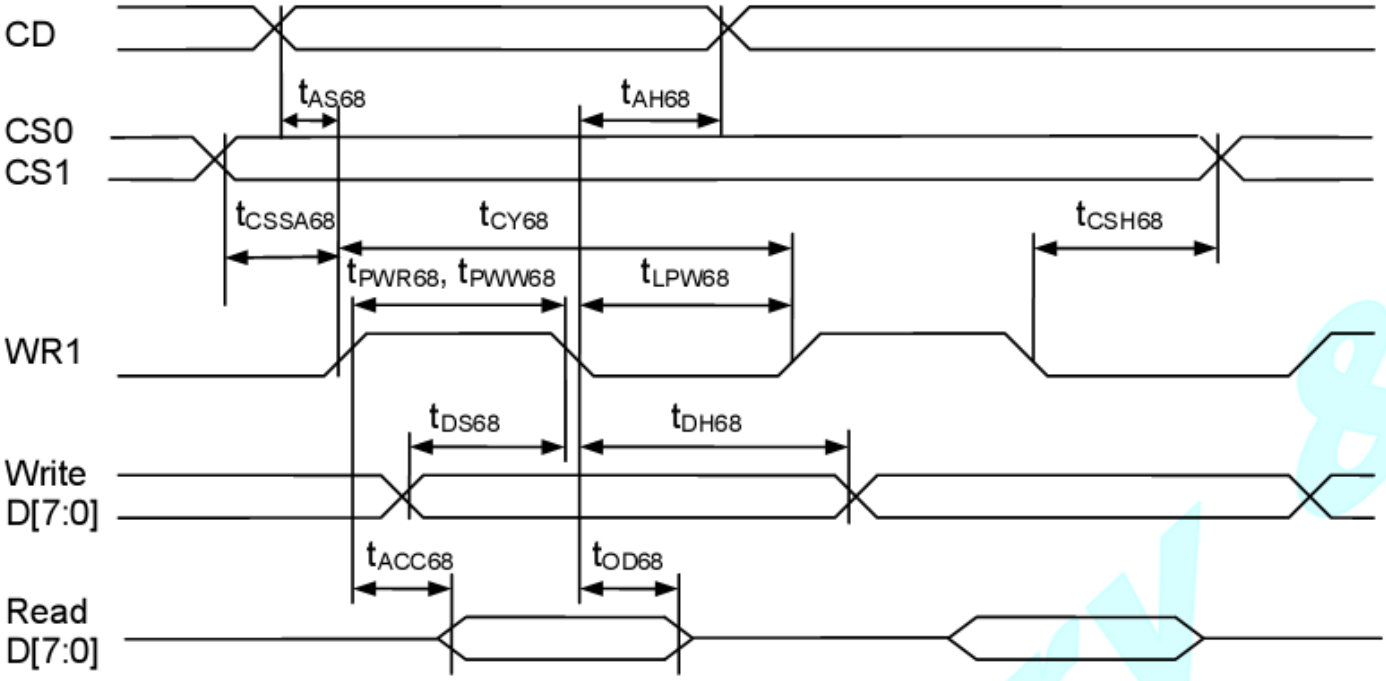


FIGURE 15: Parallel Bus Timing Characteristics (for 6800 MCU)

($2.5V \leqslant V_{DD} < 3.3V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY68}		System cycle time 16-bit bus (read) (write) 8-bit bus (read) (write)		 170 130 100 80	–	nS
t_{PWR68}	WR1	Pulse width 16-bit (read) 8-bit		85 50	–	nS
t_{PWW68}		Pulse width 16-bit (write) 8-bit		65 40	–	nS
t_{LPW68}		Low pulse width 16-bit bus (read) (write) 8-bit bus (read) (write)		 85 65 50 40	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 0	–	nS
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 15	60 30	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time		5 5		nS

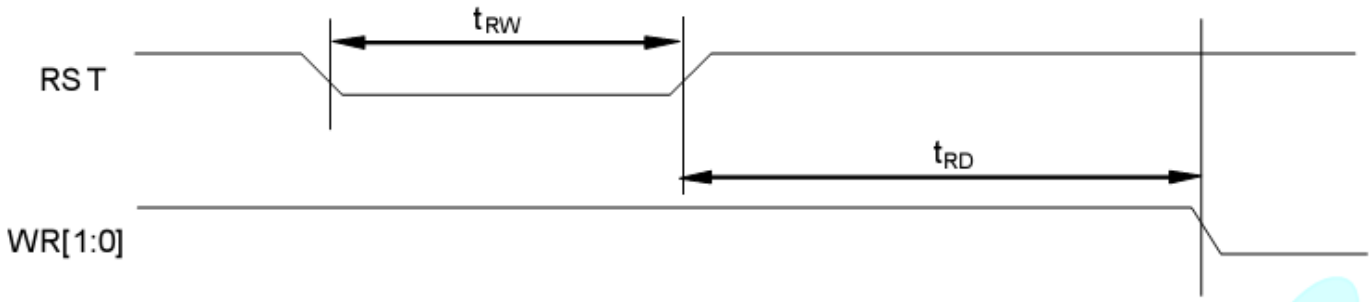


FIGURE 17: Reset Characteristics

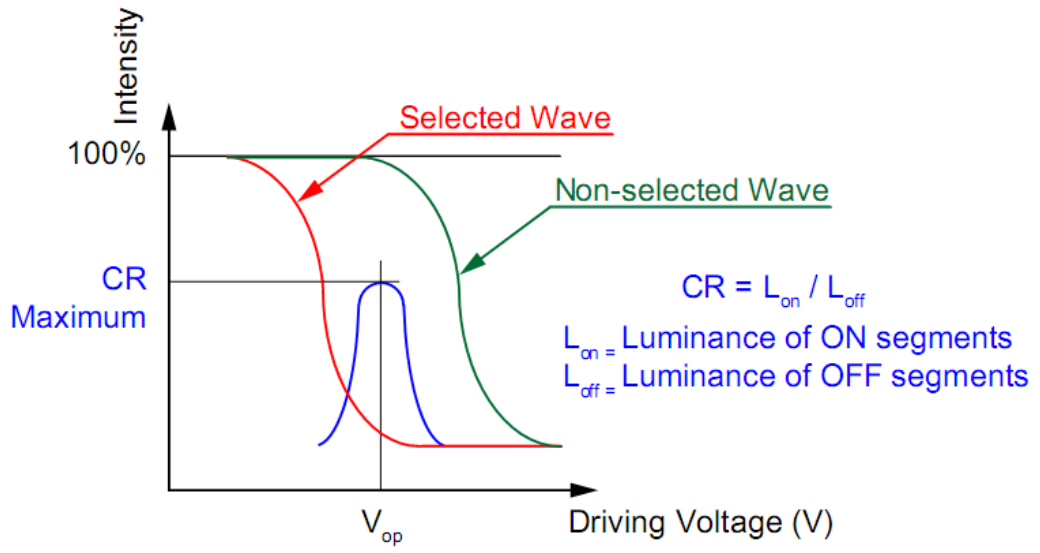
(1.65V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		3	–	μS
t_{RD}	RST, WR	Reset to WR pulse delay		10	–	mS

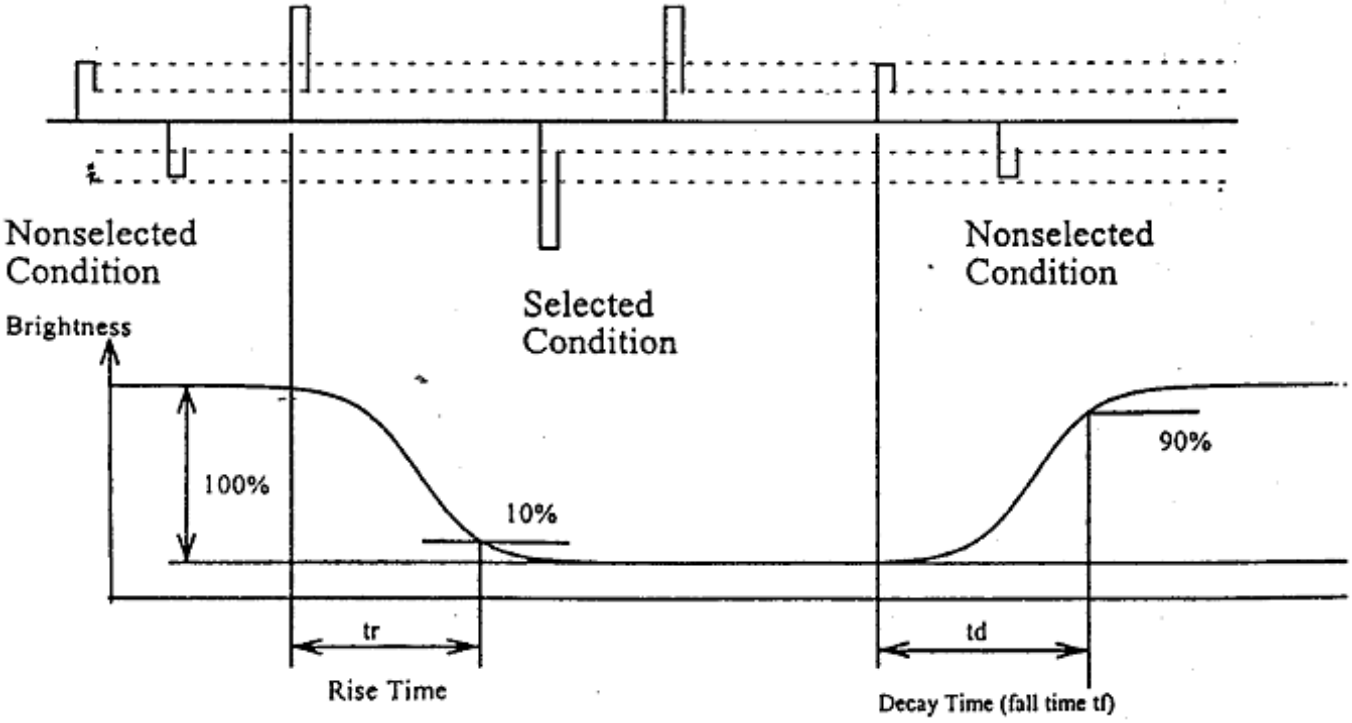
OPTICAL CHARACTERISTICS

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	NOTE
Contrast ratio	CR	θ=0，Φ=0	-	2	-		
Response time(rise)	Tr	25℃		-	230	ms	
Response time(fall)	Td			-	250		
Viewing angle	θf	25℃					
	θb						
	θl			-		deg.	
	θr			-			

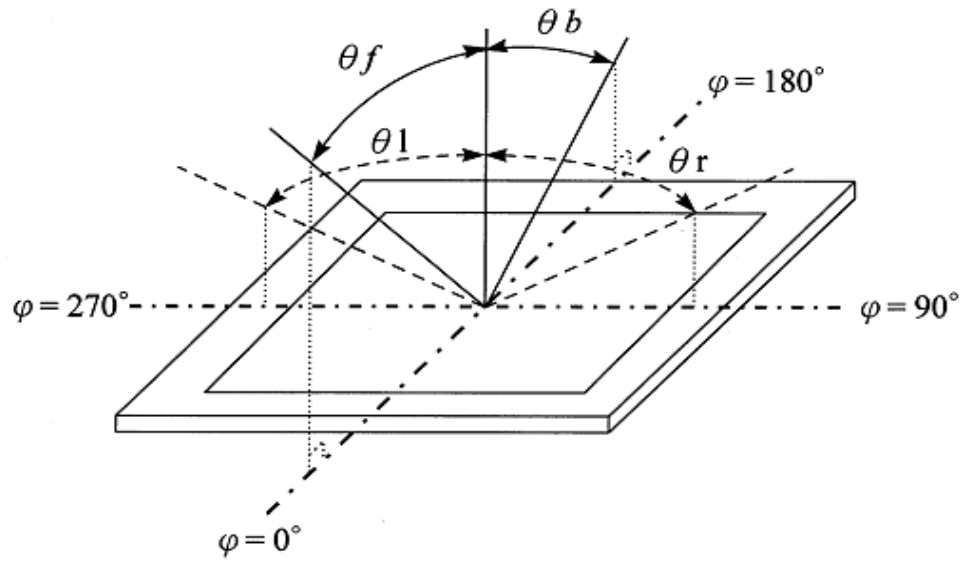
Note1: Definition Operation Voltage (V_{OP})



Note2: Response time



Note3: Viewing angle



COMMAND TABLE

The following is a list of host commands supported by UC1698u

C/D: 0: Control, 1: Data
W/R: 0: Write Cycle, 1: Read Cycle
#: Useful Data bits –: Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status & PM	0	1	GE	MX	MY	WA	DE	WS	MD	MS	Get {Status, Ver, PMO, Product Code, PID, MID}	N/A
				Ver	PMO[6:0]								
				Product Code (8h)				PID[1:0]		MID[1:0]			
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	0	#	#	#	Set CA[6:4]	0
5	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	0
6	Set Power Control	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	10b
7	Set Adv. Program Control	0	0	0	0	1	1	0	0	0	R	Set APC[R][7:0], R = 0 or 1	N/A
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
8	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0
	Set Scroll Line MSB	0	0	0	1	0	1	#	#	#	#	Set SL[7:4]	0
9	Set Row Address LSB	0	0	0	1	1	0	#	#	#	#	Set RA[3:0]	0
	Set Row Address MSB	0	0	0	1	1	1	#	#	#	#	Set RA[7:4]	0
10	Set PMO	0	0	1 -	0 #	1 #	1 #	1 #	0 #	0 #	1 #	Set PMO[6:0]	0
11	Set V_{BIAS} Potentiometer	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	40H
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
12	Set Partial Display Control	0	0	1	0	0	0	0	1	0	#	Set LC[8]	0
13	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
14	Set Fixed Lines	0	0	1	0	0	1	0	0	0	0	Set {FLT,FLB}	0
		0	0	#	#	#	#	#	#	#	#		

15	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	10b
16	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0
17	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0
18	Set Display Enable	0	0	1	0	1	0	1	#	#	#	Set DC[4:2]	110b
19	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	0
20	Set N-Line Inversion	0	0	1 -	1 -	0 -	0 #	1 #	0 #	0 #	0 #	Set NIV[4:0]	1DH
21	Set Color Pattern	0	0	1	1	0	1	0	0	0	#	Set LC[5]	0 (BGR)
22	Set Color Mode	0	0	1	1	0	1	0	1	#	#	Set LC[7:6]	10b
23	Set COM Scan Function	0	0	1	1	0	1	1	#	#	#	Set CSF[2:0]	000b
24	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
25	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
26	Set Test Control	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
27	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 12
28	Set COM End	0 0	0 0	1 -	1 #	1 #	1 #	0 #	0 #	0 #	1 #	Set CEN[6:0]	159
29	Set Partial Display Start	0 0	0 0	1 -	1 #	1 #	1 #	0 #	0 #	1 #	0 #	Set DST[6:0]	0
30	Set Partial Display End	0 0	0 0	1 -	1 #	1 #	1 #	0 #	0 #	1 #	1 #	Set DEN[6:0]	159
31	Set Window Program Starting Column Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	0 #	0 #	Shared with MTP commands	Set WPC0	0
32	Set Window Program Starting Row Address	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	1 #		Set WPP0	0
33	Set Window Program Ending Column Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	1 #	0 #		Set WPC1	127
34	Set Window Program Ending Row Address	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	1 #		Set WPP1	159
35	Window Program Mode	0	0	1	1	1	1	1	0	0	#	Set AC[3]		0: Inside
36	Set MTP Operation control	0 0	0 0	1 -	0 -	1 -	1 #	1 #	0 #	0 #	0 #	Set MTPC[4:0]		10H
37	Set MTP Write Mask	0 0 0	0 0 0	1 - -	0 # -	1 # -	1 # -	1 # -	0 # -	0 # #	1 # #	Set MTPM[6:0] MTPM1[1:0]		0
38	Set V_{MTP1} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	0 #	Shared with Window Program commands	Set MTP1	N/A
39	Set V_{MTP2} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	1 #		Set MTP2	N/A
40	Set MTP Write Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	0 #		Set MTP3	N/A
41	Set MTP Read Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	1 #		Set MTP4	N/A

NOTE:

- All other bit patterns other than commands listed above may result in undefined behavior.
- Command `Set PMO` is only available for non-MTP version UC1698u. This command has no meaning for the MTP version of UC1698u.
- The interpretation of commands (37)~(41) depends on the setting of register MTPC[3].
  - Commands (38)~(41) are shared with commands (31)~(34). These two sets of commands share exactly the same code and control registers. When MTPC[3]=0, they are interpreted as Window Program commands and registers. When MTPC[3]=1, they function as MTP Control commands and registers.
  - MTPM and PMO are actually the same register and it can be modified by either command (37) or command (10). Only one of these two commands is valid at any time, as determined by MTPC[3].
- After MTP ERASE or PROGRAM operation, before resuming normal operation, please always
  a) Remove TST4 power source,
  b) Do a full V_{DD} ON-OFF-ON cycle.

Example:

8-bit bus mode:

Set PL[1:0] = 2'b11 : D[7:0] = 0010 1011

Set PM[7:0] = 8'h8b : 1st D[7:0] = 1000 0001

2nd D[7:0] = 1000 1011

16-bit bus mode:

Set PL[1:0] = 2'b11: D[15:0] = 0000 0000 0010 1011

Set PM[7:0] = 8'h8b: 1st D[15:0] = 0000 0000 1000 0001

2nd D[15:0] = 0000 0000 1000 1011

DISPLAY DATA RAM (DD RAM)

DATA ORGANIZATION

The input display data (depend on color mode) are stored to a dual port static RAM (RAM, for Display Data RAM) organized as 160x128X16.

After setting CA and RA, the subsequent data write cycles will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page between the relation of COM, SEG, SRAM, and various memory control registers.

DISPLAY DATA RAM ACCESS

The Display RAM is a special purpose dual port RAM which allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Row Address (RA) and Column Address (CA) by issuing `Set Row Address` and `Set Column Address` commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the end of row (159), and system programmers need to set the values of RA and CA explicitly.

If WA is ON (1), when CA reaches the end of a row, CA will be reset to 0 and RA will increment or decrement, depending on the setting of row Increment Direction (RID, AC[2]). When RA reaches the boundary of RAM (i.e. RA = 0 or 159), RA will be wrapped around to the other end of RAM and continue.

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (127–CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect on the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

ROW MAPPING

COM electrode scanning orders are not affected by Start Line (SL), Fixed Line (FLT & FTB) or Mirror Y (MY, LC[3]). Visually, register SL having a non-zero value is equivalent to scrolling the LCD display up or down (depends on MY) by *SL* rows.

RAM ADDRESS GENERATION

The mapping of the data stored in the display SRAM and the scanning COM electrodes can be obtained by combining the fixed COM scanning sequence and the following RAM address generation formula.

When FL=0, during the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field

Line = *SL*

Otherwise

Line = Mod(*Line*+1, 160)

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to SEG drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produces the "loop around" effect as it effectively resets *Line* to 0 when *Line+1* reaches 160. Effects such as scrolling can be emulated by changing SL dynamically.

MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between COM electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field

Line = Mod(*SL* + *MUX-1*, 160)
where MUX = CEN + 1

Otherwise

Line = Mod(*Line-1*, 160)

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM are not affected by MY.

RELIABILITY TEST CONDITION

No.	TEST Item	Content of Test	Test Condition	Applicable Standard
1	High temperature storage	Endurance test applying the high storage Temperature for a long time.	80° C 96hrs	------
2	Low temperature storage	Endurance test applying the low storage Temperature for a long time	-30° C 96hrs	-----
3	High temperature operation	Endurance test applying the electric stress (Voltage & current)and the thermal stress to the element for a long time	70° C 96hrs	------
4	Low temperature operation	Endurance test applying the electric stress Under low temperature for a long time	-20° C 96hrs	------
5	High temperature/ Humidity storage	Endurance test applying the electric stress(Voltage & current) and Temperature/ Humidity stress to the element for a long time	40° C 90%RH 96hrs	
6	High temperature/ Humidity operation	Endurance test applying the electric stress (voltage & current)and temperature/ humidity stress to the element for a long time	40° C 90%RH 96hrs	
7	Temperature cycle	Endurance test applying the low and high temperature cycle. -20° C →25° C→70° C 30min←5min←30min.(1 cycle)	-20° C/70° C 10 cycle	------

Supply voltage for logic system = 5V. Supply voltage for LCD system = Operating voltage at 25° C.

Mechanical Test

Vibration test	Endurance test applying the vibration during transportation and using	10~22Hz→1.5mmp-p 22~500Hz→1.5G Total 0.5hour	
Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G half sign wave 11 msede 3 times of each direction	
Atmospheric pressure test	Endurance test applying the atmospheric pressure during transportation by air	115mbar 40hrs	
Static electricity test	Endurance test applying the electric stress to the terminal	VS=800V,RS-1.5KΩ CS=100pF, 1 time	

Environmental condition

The inspection should be performed at the 1metre height from the LCD module under 2 pieces of 40W white fluorescent lamps (Normal temperature 20~25℃ and normal humidity 60±15%RH).

PRECAUTION FOR USING LCM MODULE

- Please remove the protection foil of polarizer before using.
- The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
- If the display panel is damaged and the liquid crystal substance inside it leaks out, do not get any in your mouth. If the substance come into contact with your skin or clothes promptly wash it off using soap and water.
- Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarize carefully.
- To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
  -Be sure to ground the body when handling the LCD module.
  -Tools required for assembly, such as soldering irons, must be properly grounded.
  -To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
  -The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.
- Storage precautions
  When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.
  Keep the modules in bags designed to prevent static electricity charging under low temperature / normal humidity

conditions (avoid high temperature / high humidity and low temperatures below 0℃).Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

OTHERS

- Liquid crystals solidify at low temperature (below the storage temperature range) leading to defective orientation of liquid crystal or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subjected to a strong shock at a low temperature.

- If the LCD modules have been operating for a long time showing the same display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. Abnormal operating status can be resumed to be normal condition by suspending use for some time. It should be noted that this phenomena does not adversely affect performance reliability.

- To minimize the performance degradation of the LCD modules resulting from caused by static electricity, etc. exercise care to avoid holding the following sections when handling the modules :
  - Exposed area of the printed circuit board
  - Terminal electrode sections