

TECHNICAL DATA

Datasheet 4118, Rev. F

PRODUCT PARAMETERS - ($T_C=25\text{ }^\circ\text{C}$ unless otherwise noted)

| Over-Temperature Shutdown | | | | | |
|--------------------------------------|-----|-----|-----|-----|------------------------|
| Over-Temperature Shutdown | Tsd | 100 | 105 | 110 | $^\circ\text{C}$ |
| Over-Temperature Output | Tso | | 10 | | 10mV/ $^\circ\text{C}$ |
| Over-Temperature Shutdown Hysteresis | | | 20 | | $^\circ\text{C}$ |

DIODES CHARACTERISTICS

| | | | | | |
|---|----------|---|-----------|--------------|------|
| Continuous Source Current, $T_C=90\text{ }^\circ\text{C}$ SPM6M080-010D SPM6M060-025D | I_S | - | - | 70 40 | A |
| Diode Forward Voltage, SPM6M080-010D, $I_S=60\text{A}$ SPM6M060-025D, $I_S=40\text{A}$ | V_{SD} | - | | 1.15 1.35 | V |
| Diode Reverse Recovery Time, $V_{DD}=50\text{V}$, $di/dt=100\text{ A}/\mu\text{s}$ SPM6M080-010D SPM6M060-025D | t_{rr} | - | 70 290 | - | nsec |

Gate Driver

| | | | | | |
|---|-----------|-----|----------|-----|----|
| Supply Voltage | VCC | 14 | 15 | 16 | V |
| Supply Input Current at Vcc, Pin 19, Without PWM Switching , with 10KHz PWM at Two Inputs | | | 35 50 | | mA |
| Input On Current | HIN, LIN | 2 | | 5.0 | mA |
| Opto-Isolator Logic High Input Threshold | I_{th} | - | 1.6 | - | mA |
| Input Reverse Breakdown Voltage | BV_{in} | 5.0 | - | - | V |
| Input Forward Voltage @ $I_{in}=5\text{mA}$ | V_F | - | 1.5 | 1.7 | V |

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| | | | | | |
|--|-------------------|------|------|------|---------|
| Under Voltage Lockout | VCCUV | 9.0 | 10.0 | 11.5 | V |
| ITRIP Reference Voltage ⁽¹⁾ | Itrip-ref | 1.57 | 1.63 | 1.68 | V |
| Input-to-Output Turn On Delay | t _{ond} | - | 700 | - | nsec |
| Output Turn On Rise Time | t _r | - | 50 | - | |
| Input-to-Output Turn Off Delay | t _{offd} | - | 750 | - | |
| Output Turn Off Fall Time | t _f | - | 60 | - | |
| @ VCC=50V, ID=40A, T _C = 25 | | | | | |
| Dead Time Requirement, for Shoot Through Prevention | | 600 | 750 | | nsec |
| Opto-Isolator Input-to-Output Isolation Voltage, momentary | - | - | 2500 | - | V |
| Opto-Isolator Operating Input Common Mode Voltage | | | | 1000 | V |
| Opto-Isolator Operating Input Common Mode Transient Immunity, with I _{in} > 5mA | | | | 10 | KV/usec |
| Pin-To-Case Isolation Voltage, DC Voltage | | - | 1500 | - | V |

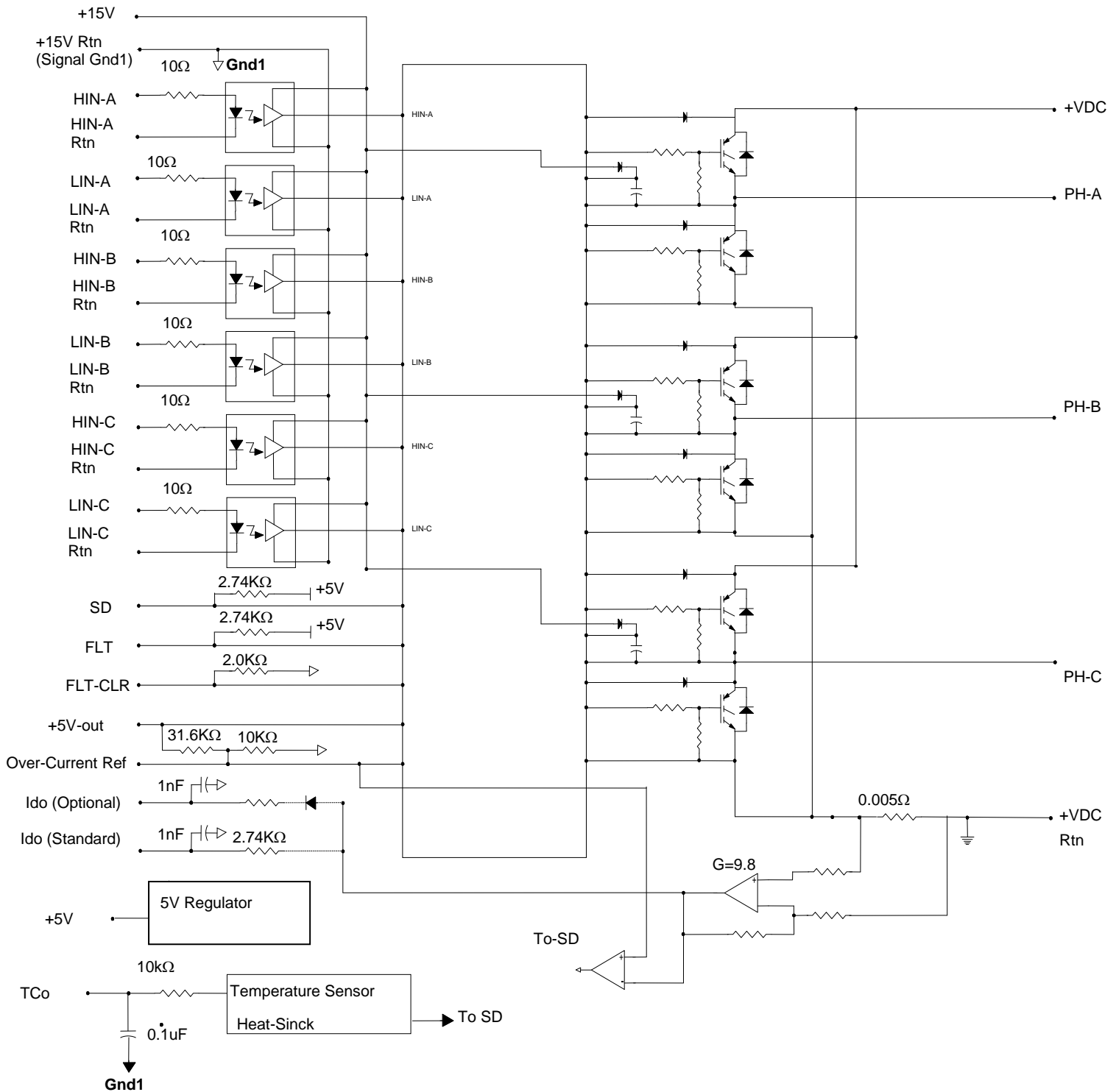
DC Bus Current Sensor

| | | | | | |
|---|---|---|-------|-------|------|
| Shunt Resistor Value | - | - | 5 | - | mOhm |
| Current Amplifier Gain, Referenced to Signal Gnd | | | 0.049 | | V/A |
| Current Amplifier DC Offset (Zero DC Bus Current) | | | 0.010 | 0.030 | V |
| Current Amplifier Response Time | | | 3 | | usec |

(1) ITRIP current limit is internally set to 35A peak. The set point can be lowered by connecting a resistor between Itrip-ref and Gnd. The set point can be increased by connecting a resistor between Itrip-ref and +5V ref. The off time duration is about 70 usec.

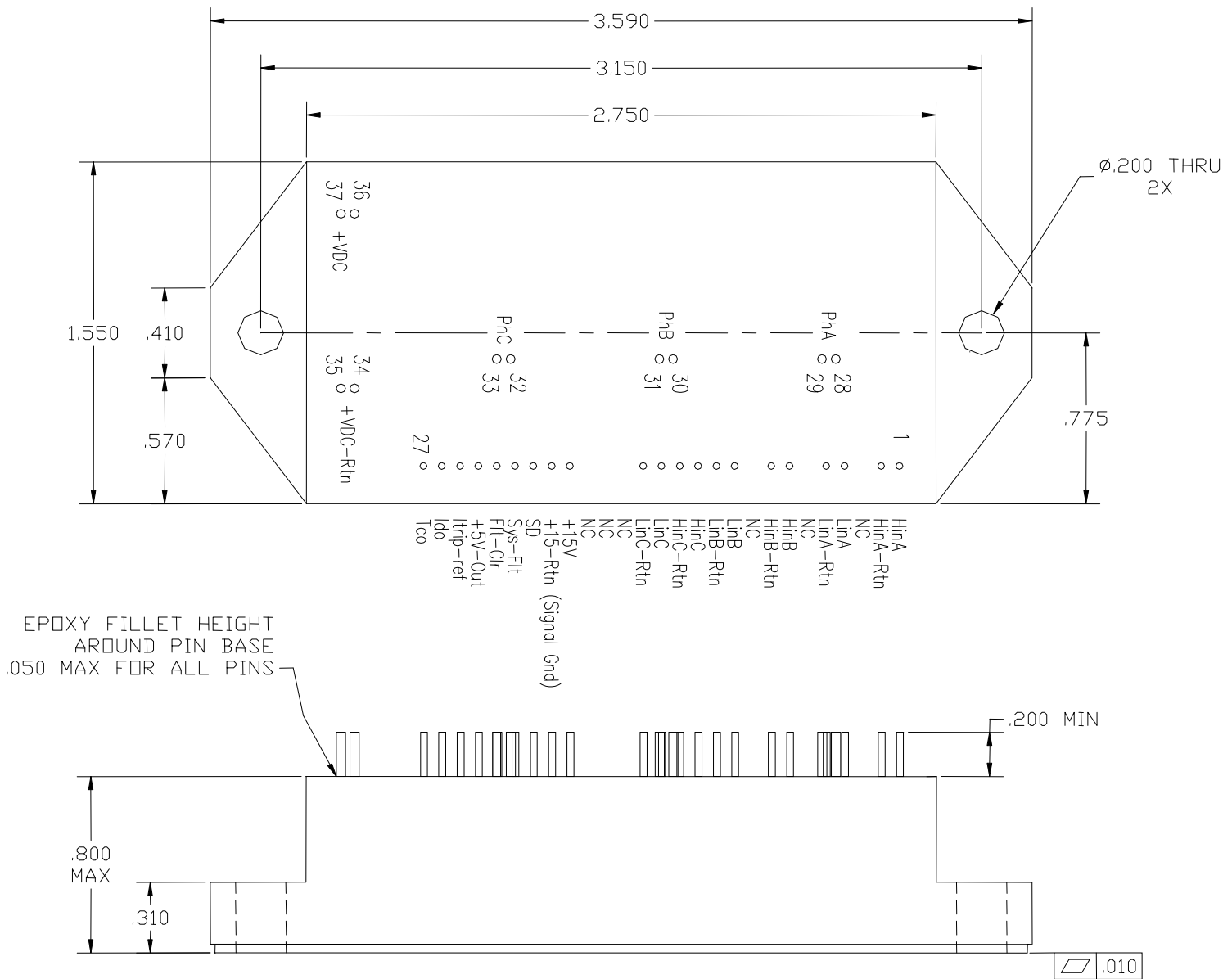
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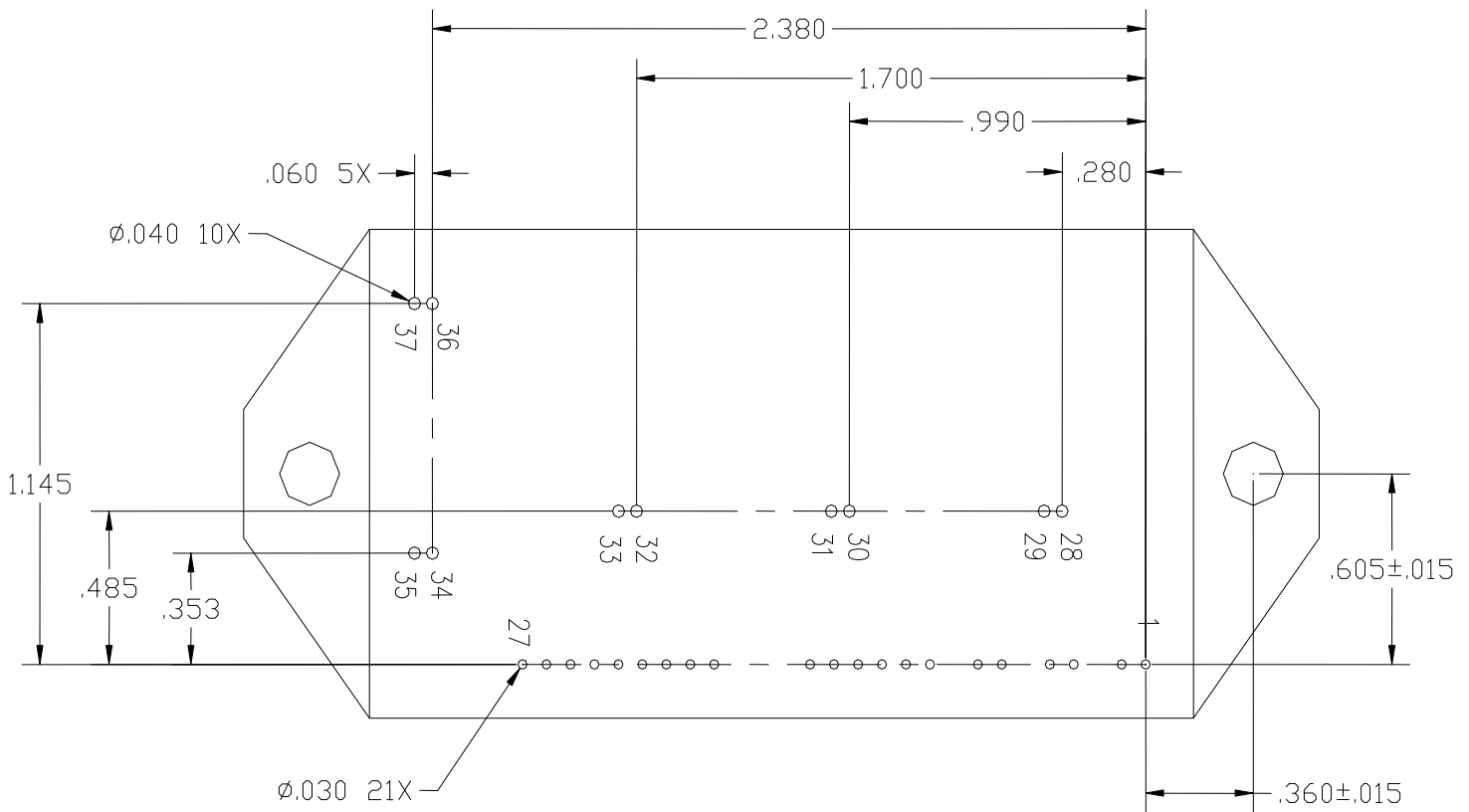
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Figure 2 - Package Drawing Top & Side Views
(All dimensions are in inches, tolerance is +/- 0.010")



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Figure 3 - Package Pin Locations
(All dimensions are in inches; tolerance is +/- 0.005" unless otherwise specified)



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PIN OUT

| Pin # | Name | Description |
|-------|-------------------------|---|
| 1 | HinA | Isolated Drive Input for High-side MOSFET of Phase A |
| 2 | HinA-Rtn | Return for Input at 1 |
| 3 | NC | Not Connected |
| 4 | LinA | Isolated Drive Input for Low-side MOSFET of Phase A |
| 5 | LinA-Rtn | Return for Input at 4 |
| 6 | NC | Not Connected |
| 7 | HinB | Isolated Drive Input for High-side MOSFET of Phase B |
| 8 | HinB-Rtn | Return for Input at 7 |
| 9 | NC | Not Connected |
| 10 | LinB | Isolated Drive Input for Low-side MOSFET of Phase B |
| 11 | LinB-Rtn | Return for Input at 10 |
| 12 | HinC | Isolated Drive Input for High-side MOSFET of Phase C |
| 13 | HinC-Rtn | Return for Input at 12 |
| 14 | LinC | Isolated Drive Input for Low-side MOSFET of Phase C |
| 15 | LinC-Rtn | Return for Input at 14 |
| 16 | NC | Not Connected |
| 17 | NC | Not Connected |
| 18 | NC | Not Connected |
| 19 | Vcc | +15V input biasing supply connection for the controller. Under-voltage lockout keeps all outputs off for Vcc below 10.5V. Vcc pin should be connected to an isolated 15V power supply. Vcc recommended limits are 14V to 16V , and shall not exceed 18V. The return of Vcc is pin 20. Recommended power supply capability is about 70mA. |
| 20 | +15V Rtn ⁽³⁾ | Signal ground for all signals at Pins 19 through 27. This ground is internally connected to the +VDC Rtn through 1.7 Ohms. It is preferred not to have external connection between Signal Gnd and +VDC Rtn. |

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| Pin # | Name | Description |
|-------|------------------------|---|
| 21 | SD ⁽³⁾ | <p>It is an active low, dual function input/output pin. It is internally pulled high to +5V by 2.74K Ω. As a low input it shuts down all MOSFETs regardless of the Hin and Lin signals.</p> <p>SD is internally activated by the over-temperature shutdown, over-current limit, and desaturation protection</p> <p>Desaturation shutdown is a latching feature. Over-temperature shutdown, and over-current limit are not latching features.</p> <p>SD can be used to shutdown all MOSFETs by an external command. An open collector switch shall be used to pull down SD externally.</p> <p>SD can be used as a fault condition output. Low output at SD indicates a latching fault situation.</p> |
| 22 | Flt ⁽³⁾ | <p>It is a dual function input/output pin. It is an active low input, internally pulled high to +5V by 2.74K Ω. If pulled down, it will freeze the status of all the six MOSFETs regardless of the Hin and Lin signals.</p> <p>As an output, Pin 13, reports desaturation protection activation. When desaturation protection is activated a low output for about 9 μsec is reported.</p> <p>If any other protection feature is activated, it will not be reported by Pin 22.</p> |
| 23 | Flt-Clr ⁽³⁾ | <p>is a fault clear input. It can be used to reset a latching fault condition, due to desaturation protection.</p> <p>Pin 23 an active high input. It is internally pulled down by 2.0KΩ. A latching fault due to desaturation can be cleared by pulling this input high to +5V by 200-500Ω, or to +15V by 3-5KΩ, as shown in Fig. 6.</p> <p>It is recommended to activate fault clear input for about 300 μsec at startup.</p> |

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| Pin # | Name | Description |
|---------|--------------------------|---|
| 24 | +5V Output | +5V output. Maximum output current is 30mA |
| 25 | Itrip-Ref ⁽³⁾ | Adjustable voltage divider reference for over-current shutdown. Internal pull-up to +5V 31.6K Ω , pull down to ground is 10K Ω , and hysteresis resistance of 50K Ω . The internal set point is 1.64V, corresponding to over-current shutdown of 34A. The re-start delay time is about 100 usec. |
| 26 | Idco | DC bus current sense amplifier output. The sensor gain is 0.049V/A. The internal impedance of this output is 2.74K Ω , and internal filter capacitance is 1nF. |
| 27 | TCo | Analog output of case temperature sensor. The sensor output gain is 0.010 V/ $^{\circ}$ C, with zero DC offset. This sensor can measure both positive and negative $^{\circ}$ C. The internal impedance of this output is 10K Ω . The internal block diagram of the temperature sensor is shown in Fig. 5. |
| 28 & 29 | PhA | Phase A output |
| 30 & 31 | PhB | Phase B Output |
| 32 & 33 | PhC | Phase C Output |
| 34 & 35 | +VDC Rtn | DC Bus return |
| 36 & 37 | +VDC | DC Bus input |
| Case | Case | Isolated From All Terminals |

Application Notes

a- Input Interface:

Recommended input turn-on current for all six drive signals is 5-8mA.
For higher noise immunity the tri-state differential buffer, DS34C87, is recommended as shown in Fig. 4.

Note : Connect LinA to non-inverting output for a non-inverting input logic.
Connect LinA to inverting output for an inverting input logic.

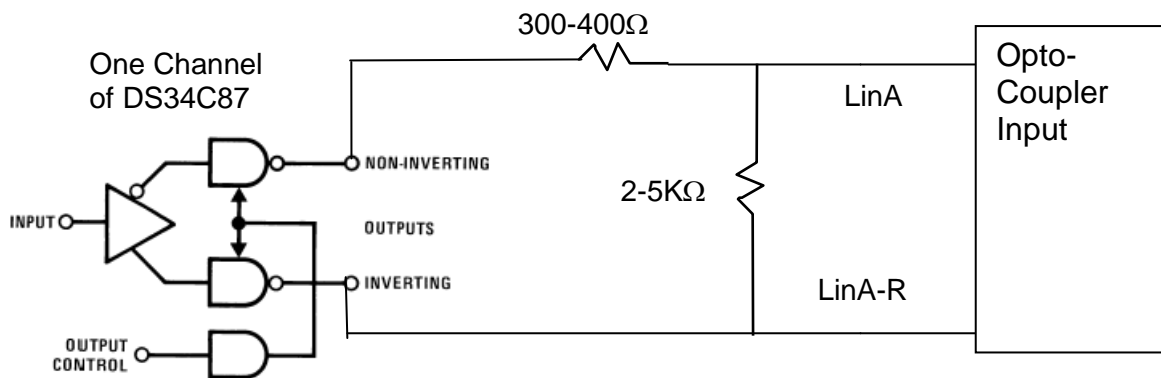


Fig. 4. Input Signal Buffer

b-Temperature Sensor Output:

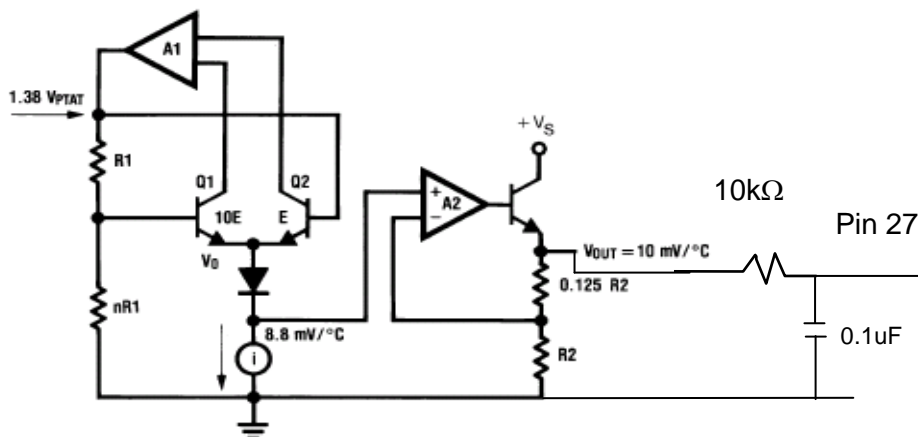


Fig. 5 Temperature Sensor Internal Block Diagram

For both negative and positive temperature measurement capability, Contact the Factory.

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c- System Start Up Sequence:

Activate fault clear input for about **300 μsec** at startup. The micro-controller enable output is inverted and fed to the second DS34C87 control input. When the controller is in disable mode, the Flt-clr is enabled and Phase C low-side MOSFET is turned on. This allows for the bootstrap circuit of the high-side MOSFET of Phase C to be charged. At the same time, the high-side bootstrap circuits of Phases A and B will charge through the motor winding. Once the controller is enabled, PWM signals of all channels should start.

Fig. 6 shows a recommended startup circuit.

Notes:

- 1- Gnd1 and Gnd2 are isolated grounds from each other.
- 2- The +5V power supply used for DS34C87 is an isolated power supply.
- 3- The +15V power supply used for SPM6M0xx-0xxD is an isolated power supply.

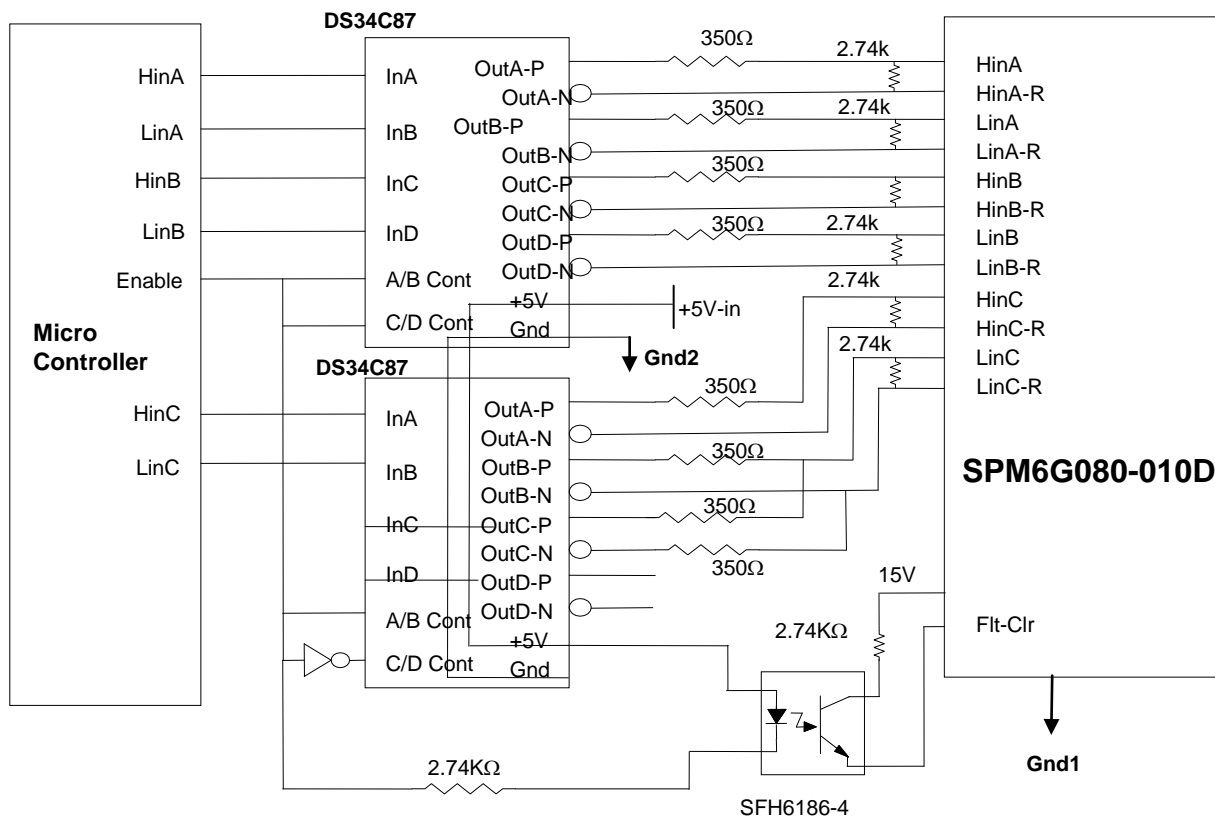


Fig. 6 Input Interface and Startup Circuit

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Truth Table For DS34C87

| Input | Control Input | Non-Inverting Output | Inverting Output |
|-------|---------------|----------------------|------------------|
| H | H | H | L |
| L | H | L | H |
| X | L | Z | Z |

d- DC Bus Charging from 15V

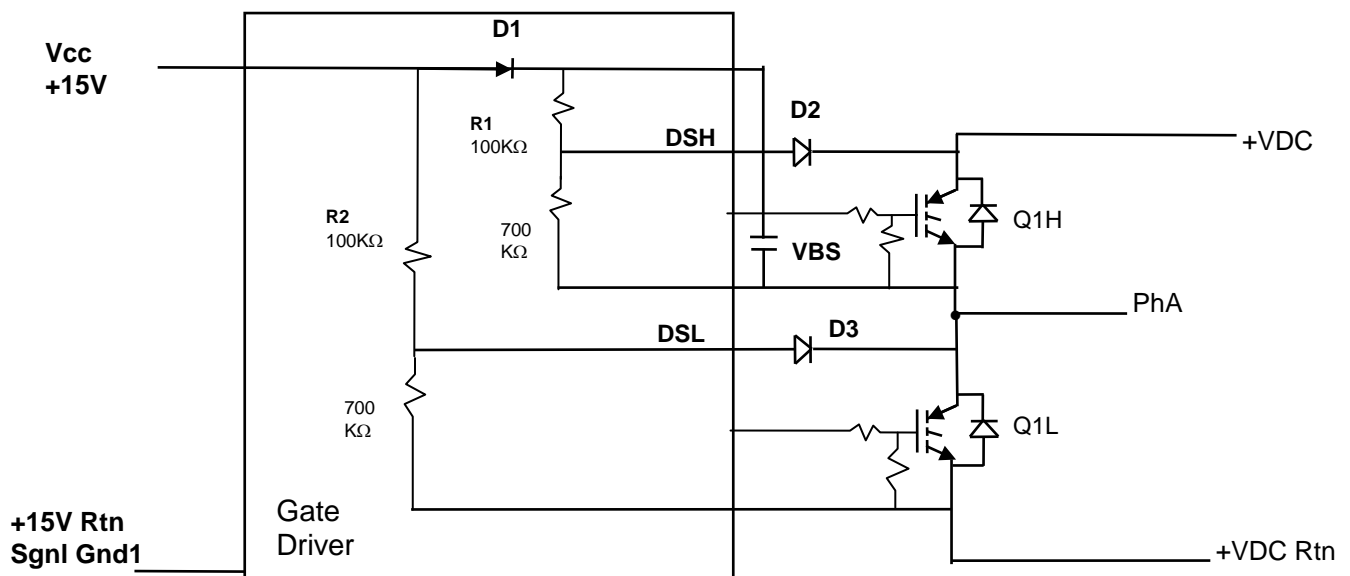


Figure 7. Charging Path from 15V Supply to DC Bus when DC Bus is off

- Each MOSFET is protected against desaturation.
- D2 is the desaturation sense diode for the high-side MOSFET
- D3 is the desaturation sense diode for the low-side MOSFET
- When the DC bus voltage is not applied or below 15V, there is a charging path from the 15V supply to the DC bus through D2 and D3 and the corresponding pull up 100K Ohm resistor. The charging current is 0.15mA per MOSFET. Total charging current is about 1.5mA.
- **Do not apply PWM signal if the DC bus voltage is below 20V.**

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g- Increasing Current Limit Window:

The adjustable over-current shutdown reference at Pin25 is internally set to 1.64V corresponding to 34A. A voltage divider reference is used as shown in Fig.16. Internal pull-up to +5V is 31.6K Ω , pull down to ground is 10K Ω , and hysteresis resistance to SD is 49.9K Ω . The re-start delay time, off time, is about 100 usec.

In order to increase the over-current shutdown reference to 2.8V, corresponding to 57A peak current, an external pull-up resistance R is needed. It is recommended to add R=9 K Ω between Pins 21 and 25. The corresponding off time will be about 200usec. The additional R=9 K Ω will reduce the high level of SD to 4.4V.

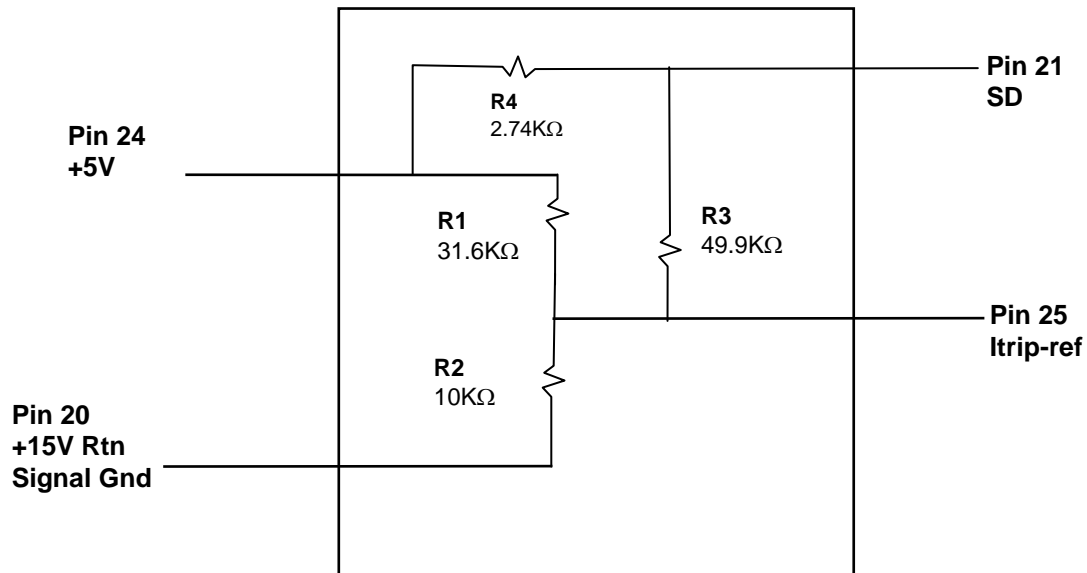


Figure 10. Internal Over-Current Shutdown Reference

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h- Cleaning Process:

Suggested precaution following cleaning procedure:

If the parts are to be cleaned in an aqueous based cleaning solution, it is recommended that the parts be baked immediately after cleaning. This is to remove any moisture that may have permeated into the device during the cleaning process. For aqueous based solutions, the recommended process is to bake for at least 2 hours at 125°C.

Do not use solvents based cleaners.

i- Soldering Procedure:

Recommended soldering procedure:

Signal pins 1 to 27: 210C for 10 seconds max

Power pins 28 to 37: 260C for 10 seconds max. Pre-warm module to 125C to aid in power pins soldering.

Ordering Information:

SPM6M080-010D, SPM6M060-025D are standard with a bi-directional current sense signal.

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