L30

Quectel GPS Engine

Hardware Design

L30_HD_V1.0

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0 Revision History

Revision	Date	Author	Description of change
1.0	2011-04-07	Ray XU/David WEI	Initial

1 Introduction

This document defines and specifies L30 GPS module. It describes L30 hardware interface and its external application reference circuits, mechanical size and air interface.

This document can help customer quickly understand module interface specifications, electrical and mechanical characteristics. With the help of this document and other application notes, customer can use L30 module to design and set up application quickly.

1.1 Related Documents

Table 1: Related documents

SN	Document name	Remark
[1]	L30_EVB _UGD	L30 EVB User Guide
[2]	L30_GPS_Protocol	L30 GPS Protocol Specification
[3]	SIRF_AGPS_AN	SIRF Platform A-GPS Application Note

1.2 Terms and Abbreviations

Table 2: Terms and abbreviations

Abbreviation	Description
CGEE	Client Generated Extended Ephemeris
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
EGNOS	European Geostationary Navigation Overlay Service
GPS	Global Positioning System
GNSS	Global Navigation Satellite System
GGA	GPS Fix Data
GLL	Geographic Position – Latitude/Longitude
GSA	GNSS DOP and Active Satellites
GSV	GNSS Satellites in View
HDOP	Horizontal Dilution of Precision
IC	Integrated Circuit
I/O	Input/Output
Kbps	Kilo Bits Per Second
LNA	Low Noise Amplifier
MSAS	Multi-Functional Satellite Augmentation System

NMEA	National Marine Electronics Association
OSP	One Socket Protocol
PDOP	Position Dilution of Precision
RMC	Recommended Minimum Specific GNSS Data
SBAS	Satellite-based Augmentation System
SUPL	Secure User Plane Location
SAW	Surface Acoustic Wave
TBD	To Be Determined
TTFF	Time-To-First-Fix
UART	Universal Asynchronous Receiver & Transmitter
VDOP	Vertical Dilution of Precision
VTG	Course over Ground and Ground Speed, Horizontal Course and Horizontal Velocity
WAAS	Wide Area Augmentation System
ZDA	Time & Date
Inorm	Normal Current
Imax	Maximum Load Current
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
VIHmax	Maximum Input High Level Voltage Value
VIHmin	Minimum Input High Level Voltage Value
VILmax	Maximum Input Low Level Voltage Value
VILmin	Minimum Input Low Level Voltage Value
VImax	Absolute Maximum Input Voltage Value
VImin	Absolute Minimum Input Voltage Value
VOHmax	Maximum Output High Level Voltage Value
VOHmin	Minimum Output High Level Voltage Value
VOLmax	Maximum Output Low Level Voltage Value
VOLmin	Minimum Output Low Level Voltage Value

2 Product Concept

The GPS ROM-based module L30 features fast acquisition and tracking with the latest SiRF Star IV technology. This module provides outstanding GPS performance in a compact form factor. Based on an external optional EEPROM which provides capability of storing ephemeris and downloading patch codes through UART, L30 can support Standalone and A-GPS (CGEE function). Advanced jamming suppression mechanism and innovative RF architecture, L30 provides a higher level of anti-jamming, ensuring maximum GPS performance. The module supports location, navigation and industrial applications including autonomous GPS C/A, SBAS (WAAS or EGNOS) and A-GPS.

L30, in SMD type, can be embedded in customer applications via the 21-pin pads with the compact 9mm * 9 mm * 1.6mm form factor. It provides all hardware interfaces between the module and host board.

- The multiplexed communication interface: UART/SPI/I2C interface.
- The Dead Reckoning I2C interface up to 400Kbps can be used to connect with an external EEPROM to save Ephemeris data for CGEE function and to store patch codes.
- The antenna interface supports passive or active antenna.

The module is RoHS compliant to EU regulation.

2.1 Key Features

Table 3: Module key features

Feature	Implementation
Power supply	supply voltage: 1.71V – 1.89V typical : 1.8V
Power consumption (passive antenna)	● Acquisition 40 mA @ -130dBm ● Tracking 36 mA @ -130dBm
Receiver Type	● GPS L1 1575.42MHz C/A Code ● 48 search channels
Sensitivity	● Cold Start (Autonomous) -145 dBm ● Reacquisition -159 dBm ● Hot Start -159 dBm ● Tracking -160 dBm ● Navigation -159 dBm
Sensitivity（with external LNA）	● Cold Start (Autonomous) -148 dBm ● Reacquisition -160 dBm ● Hot Start -160 dBm ● Tracking -163 dBm ● Navigation -160 dBm
Time-To-First-Fix	● Cold Start (Autonomous) <35s

	● Warm Start (Autonomous) <35s ● Warm Start (With CGEE) 10s typ. ● Hot Start (Autonomous) <1s
Horizontal Position Accuracy	● <2.5 m CEP
Max Update Rate	● 1Hz
Accuracy of 1PPS Signal	● Typical accuracy 61 ns ● Time pulse 200ms
Velocity Accuracy	● Without aid 0.01 m/s
Acceleration Accuracy	● Without aid 0.1 m/s²
Dynamic Performance	● Maximum altitude <18288m ● Maximum velocity 514m/s Maximum ● Acceleration 4 G
Dead Reckoning I2C Interface	● Open drain output ● MEMS support (TBD devices) ● Standard I2C bus maximum data rate 400kbps ● Minimum data rate 100kbps
Communication interface	● Support multiplexed SPI/I2C/UART interface ● the output is CMOS 1.8V compatible and the input is 3.6V tolerant
Temperature range	● Normal operation: -40°C ~ +85°C ● Storage temperature: -45°C ~ +125°C
Physical Characteristics	Size: 9±0.15 mm * 9±0.15 mm * 1.6±0.1mm Weight: Approx. 0.6 g

2.2 Functional Diagram

The block diagram of L30 is shown in the Figure 1.

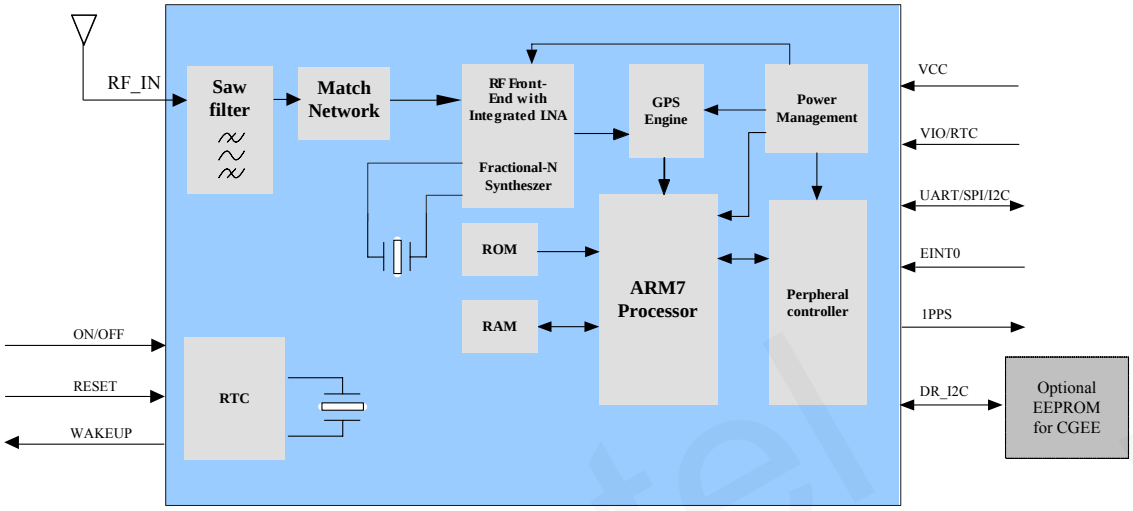


Figure 1: Module functional diagram

2.3 Evaluation Board

In order to help customer to develop applications with L30, Quectel offers an Evaluation Board (EVB) with appropriate power supply, RS-232 serial port, EEPROM and active antenna.

Note: For more details, please refer to the document [1].

2.4 Protocol

L30 supports standard NMEA-0183 protocol and the One Socket Protocol (OSP), which is the binary protocol interface that enables customer host device to access all SiRF GPS chip products of the SiRF Star IV family and beyond. The module is capable of supporting the following NMEA formats: ***GGA, GSA, GLL, GSV, RMC, and VTG.***

Table 4: The module supports protocols

Protocol	Type
NMEA	Input/output, ASCII, 0183, 3.01
OSP	Input/output, OSP protocol

Note: Please refer to document [2] about NMEA standard protocol and SiRF private protocol.

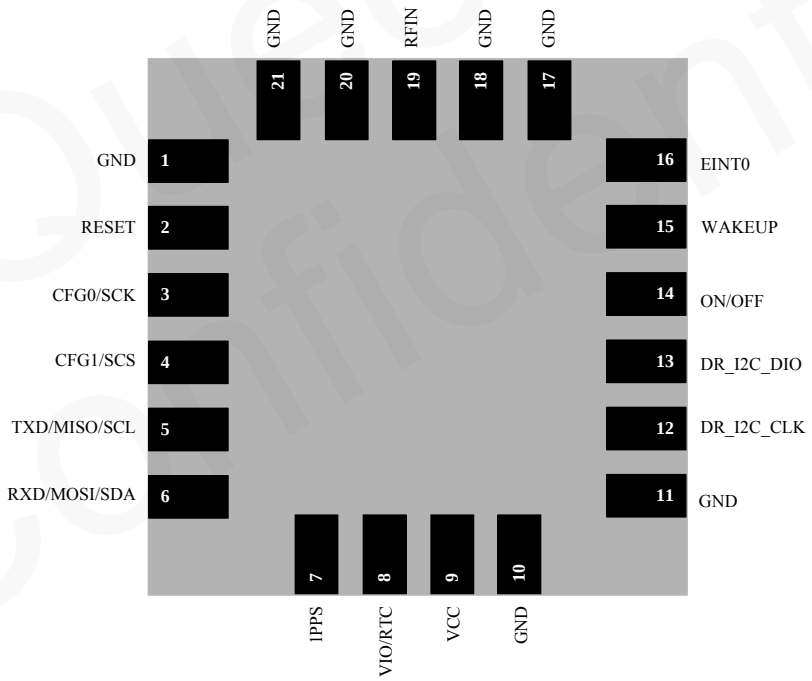
3 Application

L30 is equipped with a 21-pin SMT pad that connects to customer serial port. Sub-interfaces included in these pads are described in details in the following chapters:

- Power management *(refer to Chapter 3.4)*
- Power supply *(refer to Chapter 3.5)*
- Timing sequence *(refer to Chapter 3.6)*
- Communication interface (*refer to Chapter 3.7)*
- Assisted GPS *(refer to Chapter 3.8)*

Electrical and mechanical characteristics of the SMT pad are specified in *Chapter 5* & *Chapter 6.*

3.1 Pin Assignment of the Module



3.2 Pin Description

Table 5: Pin description

Power Supply					
PIN NAME	**PIN NO.**	**I/O**	**DESCRIPTION**	**DC CHARACTERISTICS**	**COMMENT**
VCC	9	I	Supply voltage	Vmax= 1.89V Vmin=1.71V Vnorm=1.8V	Supply current will be no less than 100mA.
VIO/RTC	8	I	RTC and CMOS I/O voltage supply	Vmax=1.89V Vmin=1.71V Vnorm=1.8V $I_{VIO/RTC}$=15uA@ hibernate mode	Power supply for RTC and CMOS I/O. In the full on mode make sure both VIO/RTC and VCC simultaneously power-on. In the hibernate mode make sure VIO/RTC power-on to keep the data lossless.
General purpose input/output					
PIN NAME	**PIN NO.**	**I/O**	**DESCRIPTION**	**DC CHARACTERISTICS**	**COMMENT**
WAKEUP	15	O	When the module is in full on mode, this pin will output high level.	VOLmin=-0.3V VOLmax=0.4V VOHmin=0.75* VIO/RTC	The wakeup pin is used as a flag of power mode. The low level indicates hibernate mode and the high level indicates the full on module. If unused, keep this pin open.
RESET	2	I	External reset input, active low	VILmin=-0.4V VILmax=0.45V VIHmin=0.7* VIO/RTC VIHmax=3.6V	The system reset is provided by the RTC monitor circuit and it is active low and must have an external pull up resistor to keep the signal stable when it works. Pressing reset pin will result in clearing of all BBRAM , SRAM and RTC block. If unused, keep this pin open.

EINT0	16	I	External interrupt input pin Provides an interrupt on either high or low logic level or edge sensitive interrupt.	VILmin=-0.4V VILmax=0.45V VIHmin=0.7*VCC VIHmax=3.6V	If unused, pull this pin down to ground directly. It is not supported by SIRF at present.
ON_OFF	14	I	Power control pin	VILmin=-0.4V VILmax=0.45V VIHmin=0.7* VIO/RTC VIHmax=3.6V	A pulse generated on the ON_OFF pin which lasts for at least 1ms and consists of a rising edge and low level, can switch operating mode between hibernate and full-on.
1PPS	7	O	One pulse per second	VOLmin=-0.3V VOLmax=0.4V VOHmin=0.75*VCC	1PPS output provides a pulse signal for time purpose. If unused, keep this pin open.
Serial Interface					
PIN NAME	**PIN NO.**	**I/O**	**DESCRIPTION**	**DC CHARACTERISTICS**	**COMMENT**
DR_I2C DIO	13	I/O	Dead Reckoning I2C data (SDA)	VOLmax=0.4V VOHmin=0.75*VCC VILmin=-0.4V VILmax=0.45V VIHmin=0.7*VCC VIHmax=3.6V	If unused, keep this pin open.
DR_I2C_ CLK	12	O	Dead Reckoning I2C clock(SCL)	VOLmax=0.4V VOHmin=0.75*VCC	If unused, keep this pin open.
CFG0/ SCK	3	I	Function overlay: ● SPI_CLK slave SPI clock input (SCK) ● Configure Pin 0	VILmin=-0.4V VILmax=0.45V VIHmin=0.7*VCC VIHmax=3.6V	When serial port is configured as UART, pull up to VCC via a 10k resistor.
CFG1/ SCS	4	I	Function overlay: ● SPI_CS_N slave SPI chip select (SCS) active low	VILmin=-0.4V VILmax=0.45V VIHmin=0.7*VCC VIHmax=3.6V	When serial port is configured as I2C, pull down to GND via a 10k resistor.

			● Configure Pin 1		
RXD/ MOSI/ SDA	6	I/O	Function overlay: ● SSPI_DI slave SPI data input (MOSI) ● UART_RX UART data receive (RXD) ● I2C_DIO I2C data (SDA)	VOLmax=0.4V VOHmin=0.75*VCC VILmin=-0.4V VILmax=0.45V VIHmin=0.7*VCC VIHmax=3.6V	
TXD/ MISO/ SCL	5	I/O	Function overlay: ● SSPI_DO slave SPI data output (MISO) ● UART_TX UART data transmit (TXD) ● I2C_CLK I2C clock (SCL)	VOLmax=0.4V VOHmin=0.75*VCC VILmin=-0.4V VILmax=0.45V VIHmin=0.7*VCC VIHmax=3.6V	
RF interface					
PIN NAME	**PIN NO.**	**I/O**	**DESCRIPTION**	**DC CHARACTERISTICS**	**COMMENT**
RFIN	19	I	GPS signal input	Impedance of 50Ω	Refer to Chapter 4.

3.3 Operating Modes

The table below briefly summarizes the various operating modes in the following chapters.

Table 6: Overview of operating modes

Mode	Function
Acquisition mode	The module starts to search satellite, determine visible satellites and coarse carrier frequency and code phase of satellite signals. When the acquisition is done, it switches to tracking mode automatically.
Tracking mode	The module refines acquisition's message, as well as keeps tracking and demodulating the navigation data from the specific satellites.
Hibernate mode	The module can be switched to hibernate mode by applying a pulse which consists of a rising edge and high level that persists for at least 1ms on the ON_OFF pin.

3.4 Power Management

There are two power supply pins in L30, VCC and VIO/RTC.

3.4.1 VCC Power

VCC pin supplies power for GPS BB domain and GPS RF domain. The power supply VCC's current varies according to the processor load and satellite acquisition. Typical VCC max current is 100 mA. So it is important that the power is clean and stable .Generally, ensure that the VCC supply ripple voltage meet the requirement: 54 mV(RMS) max @ f = 0… 3MHz and 15 mV(RMS) max @ f > 3 MHz.

Table 7: Pin definition of the VCC pin

Name	Pin	Function
VCC	9	power supply for GPS BB and RF part

3.4.2 VIO/RTC Power

The VIO/RTC pin supplies power for all RTC domain and CMOS I/O domain. So VIO/RTC should be powered all the time when the module is running. It ranges from 1.71V to 1.89V, In order to achieve a better Time To First Fix (TTFF) after VCC power down, VIO/RTC should be valid all the time. It can supply power for SRAM memory which contains all the necessary GPS information for quick start-up and a small amount of user configuration variables.

Table 8: Pin definition of the VIO/RTC pin

Name	Pin	Function
VIO/RTC	8	Power for RTC and CMOS /IO

3.4.3 Energy Saving Mode

3.4.3.1 ATP Mode

Adaptive trickle power (ATP): In this mode, L30 cycles three modes internally to optimize power consumption. This three modes consist of full on mode, CPU only mode and standby mode. The full on mode lasts about 200~900ms to require new ephemeris to get a valid position, and the other two modes are partially power off or completely power off to decrease consumption. The timing sequence is shown in following figure. This mode is configurable with SiRF binary protocol message ID151. The following diagram is a default configuration and it is tested in the strong signal environment. When the signal becomes weak, it will not comply with the following rule. The weaker the signal is, the longer time the module lasts in full on mode. In the extreme condition, when there is no signal input, the mode cycles only two modes including full on and standby mode.

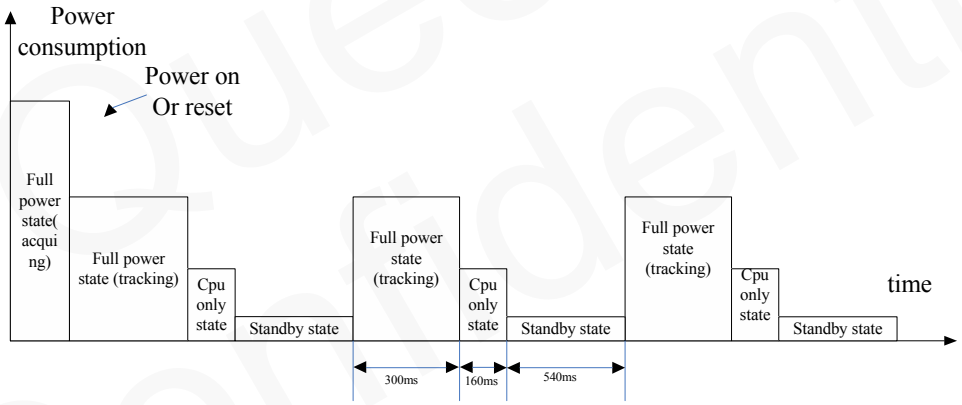


Figure 2: ATP timing sequence

3.4.3.2 PTF Mode

Push to fix (PTF) : In this mode, L30 is configured to be waked up periodically, typically every 1800 sec (configurable range 10… 7200 sec) for updating position and collecting new ephemeris data from valid satellites. For the rest of the time, the module stays in Hibernate mode. A position request acts as a wakeup of the module, which is then able to supply a position within the hot-start time specification.This mode is configurable with SiRF binary protocol message ID167 and the following figure is the default configuration. Additionally, when the signal becomes weak, push to fix function is not valid.

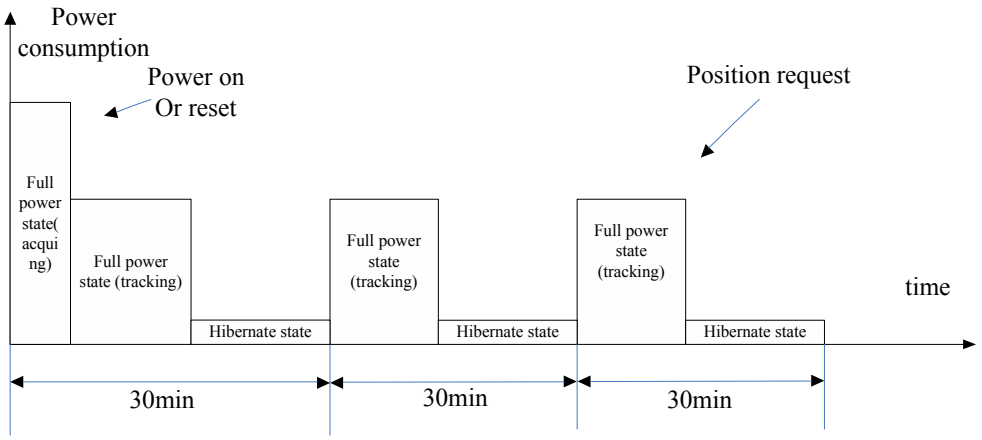


Figure 3: PTF timing sequence

3.4.3.3 Hibernate Mode

Hibernate mode means low consumption in this mode. Some power domains are powered off such as ARM, DSP and RF part, but the RTC domain includes all non-volatile logic, the RAM, and GPS BB logic I/O are still active. The module is waked up from Hibernate mode on the next ON_OFF (at rising edge) using all internal aided information like GPS time, Ephemeris, Last Position and so on, to carry out a fast TTFF in either Cold or Warm start mode.

3.5 Power Supply

3.5.1 Power Reference Design

The following diagram is one solution of power supply for L30 module. Customer can follow this reference design to get a short TTFF in either warm start or cold start. The point of this design is that battery will take the place of VCC_3.3 to supply power for the module when VCC_3.3 is lost. At the same time, VCC_3.3 will charge the battery when it is active.

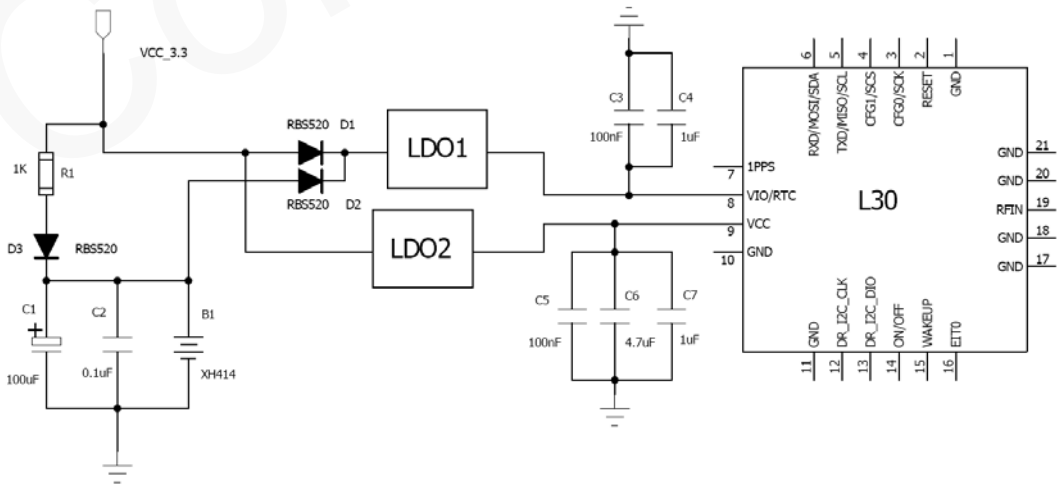


Figure 4: Reference power design for L30 module

3.5.2 Battery

In this part, the charging circuit of battery is introduced and XH414 is chosen as an example, the following circuit is the reference design.

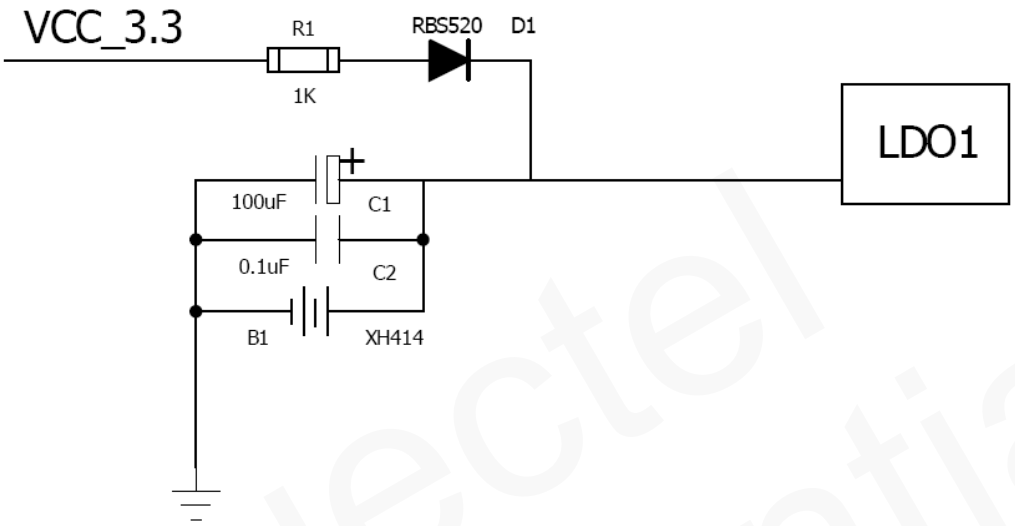


Figure 5: Reference charging circuit for chargeable battery

Coin-type Rechargeable Capacitor such as XH414H-IV01E from Seiko can be used and Schottky diode such as RB520S30T1G from ON Semiconductor is recommended for its low voltage drop. The charging and discharging characteristic of XH414 in shown in the following figure,

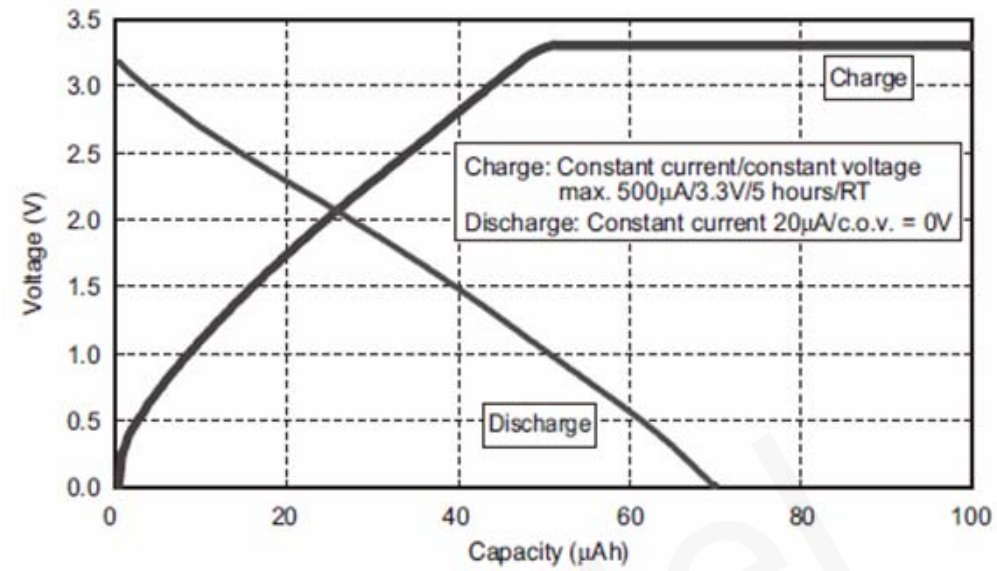


Figure 6: Seiko XH414 charging and discharging characteristics

3.6 Timing Sequence

The ON_OFF pin is used to wake up the module. Pull this pin up to VCC via a 10K resistor to avoid being triggered unexpectedly.

L30 integrates power on reset circuit internally and external RESET signal which are based on VIO/RTC domain. When VCC and VIO/RTC is supplied simultaneously, the internal power on reset circuit occurs. Normally external control of RESET is not necessary. When power supply VCC is removed abruptly, an externally RESET is suggested. Additional, make sure external RESET pin pull up to VCC via 10K resistor.

The following diagram is the reference timing sequence. Firstly, VCC and VIO/RTC power on ,then a pulse of wakeup will be generated , after that when ON/OFF is toggled ,the module will go into the full on mode and the WAKEUP will turn to high level. Next toggling of the ON/OFF can return to the hibernate mode. The state conversion is shown in the following figure.

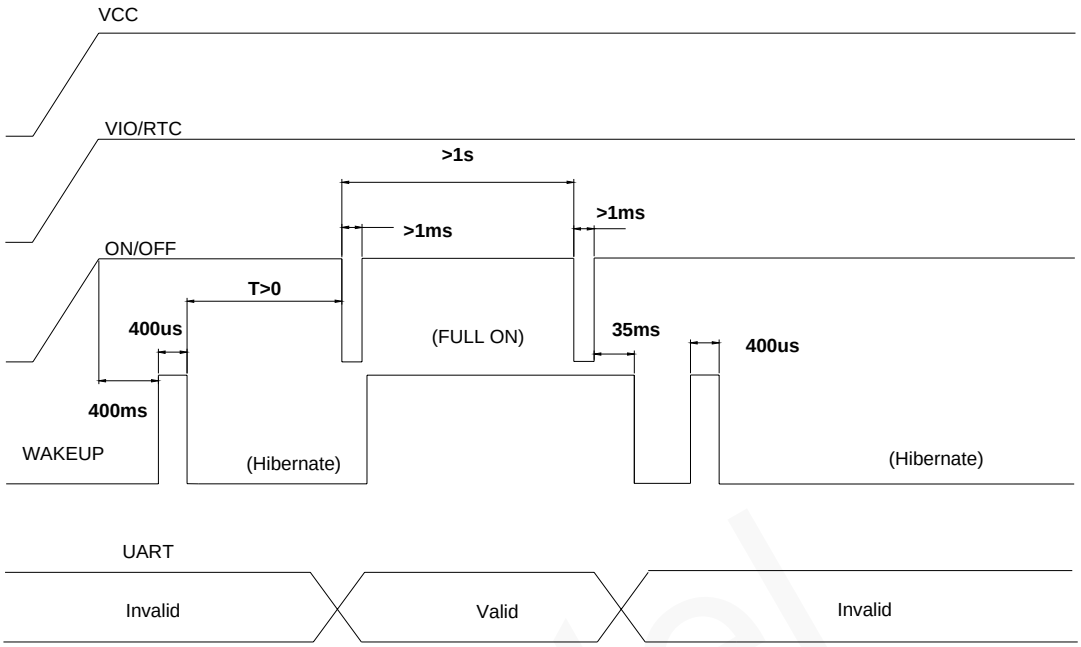


Figure 7: Turn on timing sequence of module

NOTE:

If the "ON_OFF" pin is controlled by host controller, a 1K Ω resistor should be inserted between the GPIO of the controller and "ON_OFF" pin.

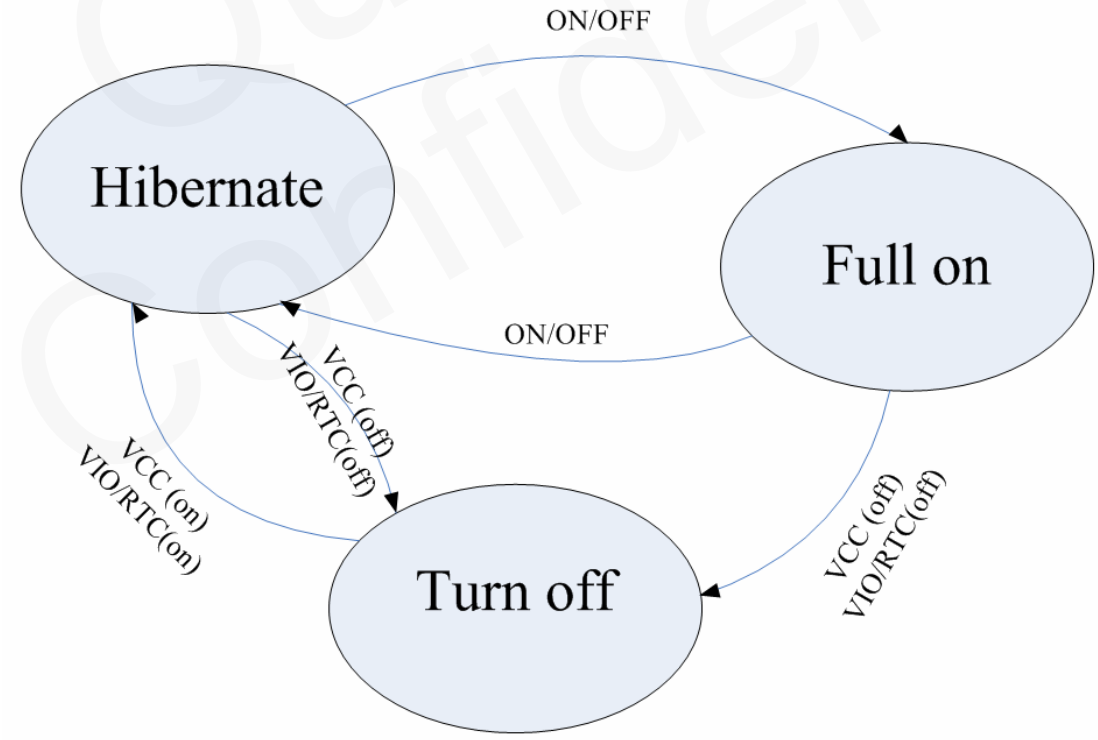


Figure 8: State conversion of module

3.7 Communication Interface

Communicate interface which includes UART interface/ I2C interface/ SPI interface is used to output NMEA messages or to communicate with the customer device via the OSP protocol. All these interfaces are multiplexed on a share set of pins. The interface selection is not intended o be changed dynamically but only at boot time.

Table 9: Communicate interface multiplexed function pin

Pin name	Pin NO.	Communicate interface		
		UART	**Slave SPI**	**I2C**
CFG0/SCK	3	Pull up	slave SPI clock input (SCK)	Open
CFG1/SCS	4	Open	slave SPI chip select (SCS) active low	Pull down
RXD/MOSI/SDA	6	Data receive	slave SPI data input (MOSI)	I2C data (SDA)
TXD/MISO/SCL	5	Data transmit	slave SPI data output (MISO)	I2C clock (SCL)

3.7.1 UART Interface

L30 offers multiplexed pins which can be configured as one UART interface and CFG0/SCK should be pulled up to VCC via a 10K resistor. The module is designed as a DCE (Data Communication Equipment). Serial port TXD/MISO/SCL is connected to UART RX of customer device. Serial port RXD/MOSI/SDA is connected to UART TX of customer device. It supports data baud-rate from 4800bps to 115200bps, meanwhile customer can change the baud-rate by SIRF binary protocol message ID 134.

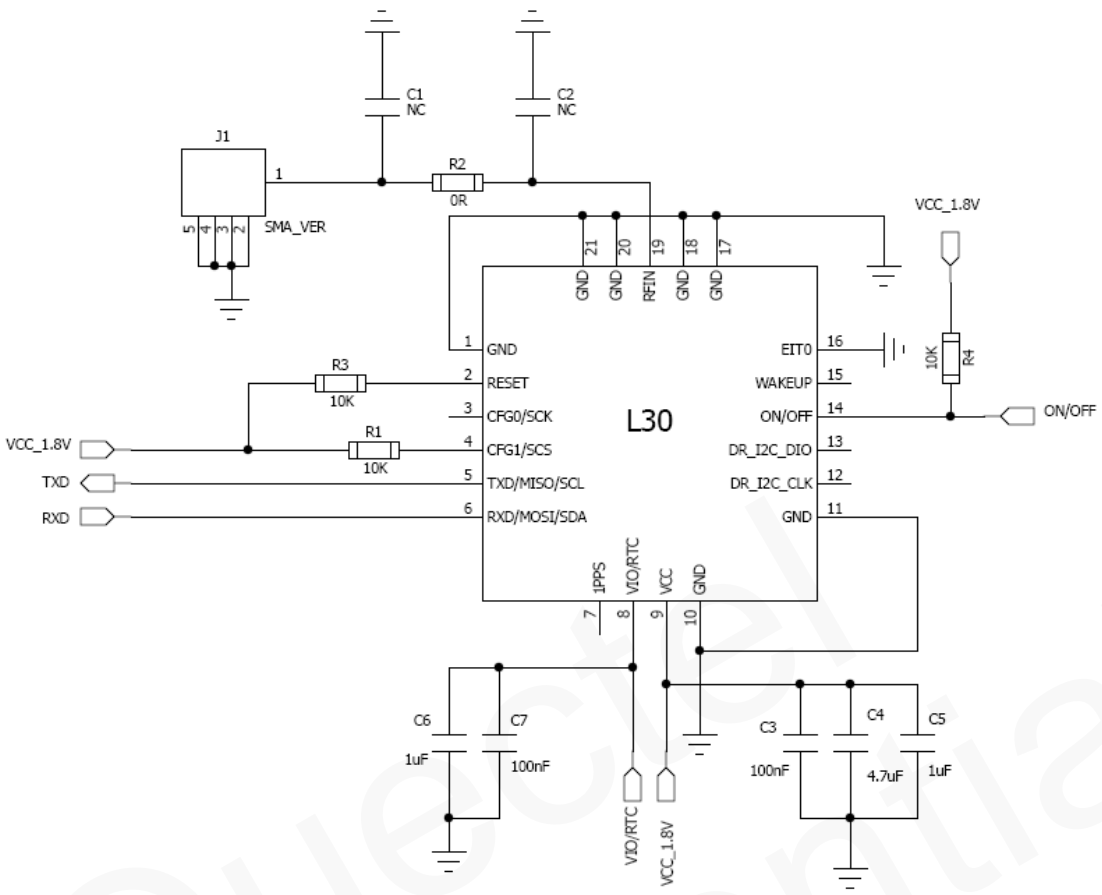


Figure 9: UART design for L30 module

This UART interface has the following features:

- The UART interface can be used to output NMEA and input & output OSP messages.
  The default output NMEA types are **RMC, GGA, GSA, and GSV (after successful positioning).**
- The UART interface supports the following data rates:
  4800, 9600, 14400, 19200, 28800, 38400, 57600, 115200.
  The default setting is 4800bps, 8 bits, no parity bit, 1 stop bit, no hardware flow control.
- The output is CMOS 1.8V compatible and the input is 3.6V tolerant.

Note: It is strongly recommended that the UART interface is used to output NMEA message to serial port of host processor.

The UART interface does not support the RS-232 level. It supports only the TTL/CMOS level. If the module UART interface is connected to the UART interface of a computer, it is necessary to insert a level shift circuit between the module and the computer. Please refer to the following figure.

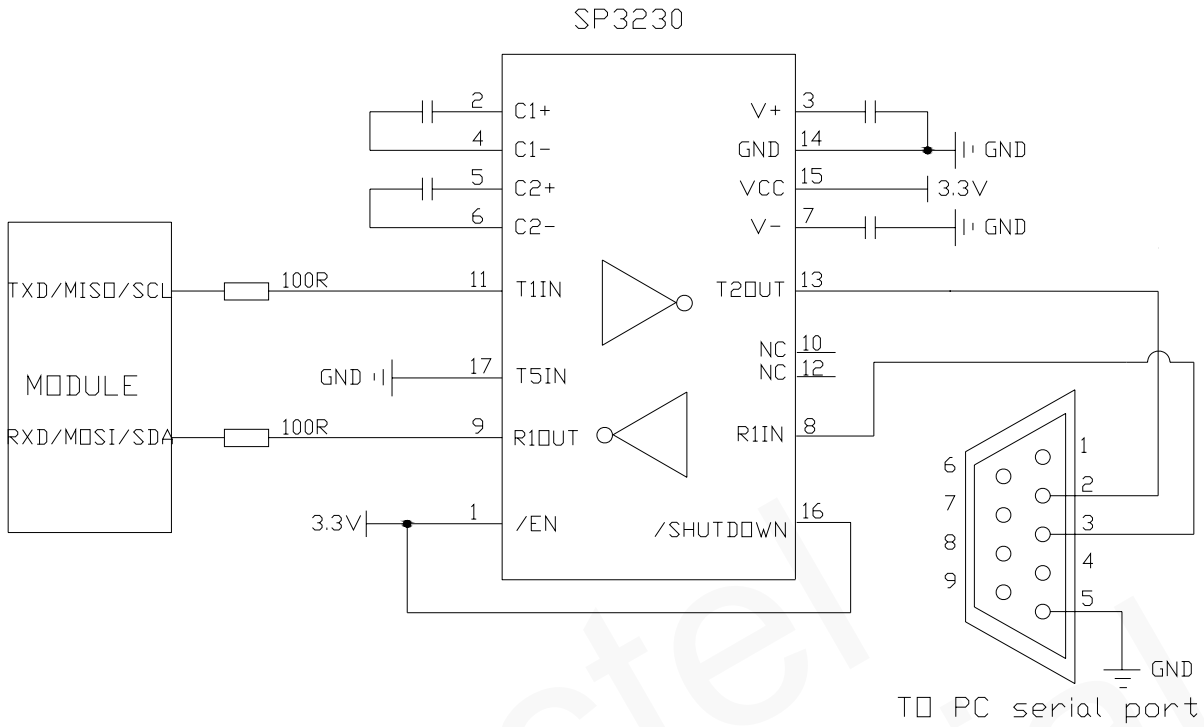


Figure 10: RS-232 level shift circuit

3.7.2 I2C Interface

L30 provides multiplex function via TXD/MISO/SCL, RXD/MOSI/SDA and CFG1/SCS to construct I2C interface. Communication interface is configured as I2C by pulling CFG1/SCS down via the resistor R1. The default mode is master mode. It is important that the customer must pull up these two pins via 2K resistor for the OC/OD interface. Otherwise, there is no signal output. The reference design is described in Figure 12.

This I2C interface has the following features:

- Operate up to 400kbps.
- Support Multi-master I2C mode by default.
- The default I2C master address: 0x60.
- The default I2C slave address: 0x62.

The following figure is the I2C timing sequence.

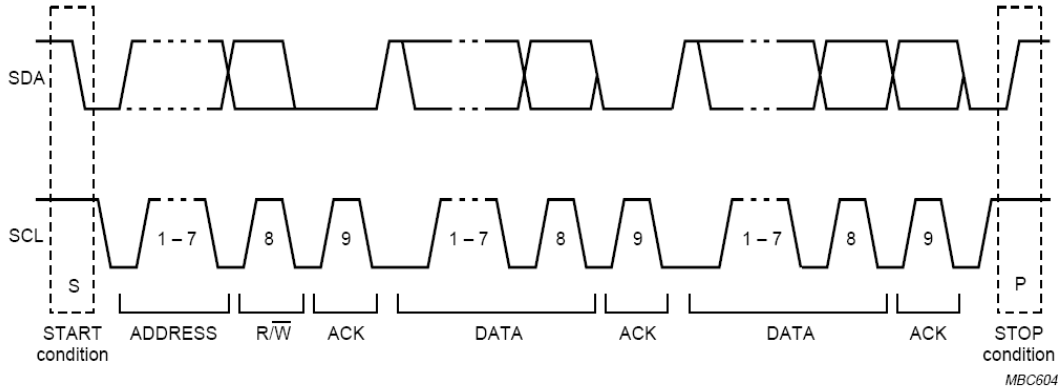


Figure 11: I2C timing sequence

The following circuit is an example of connection.

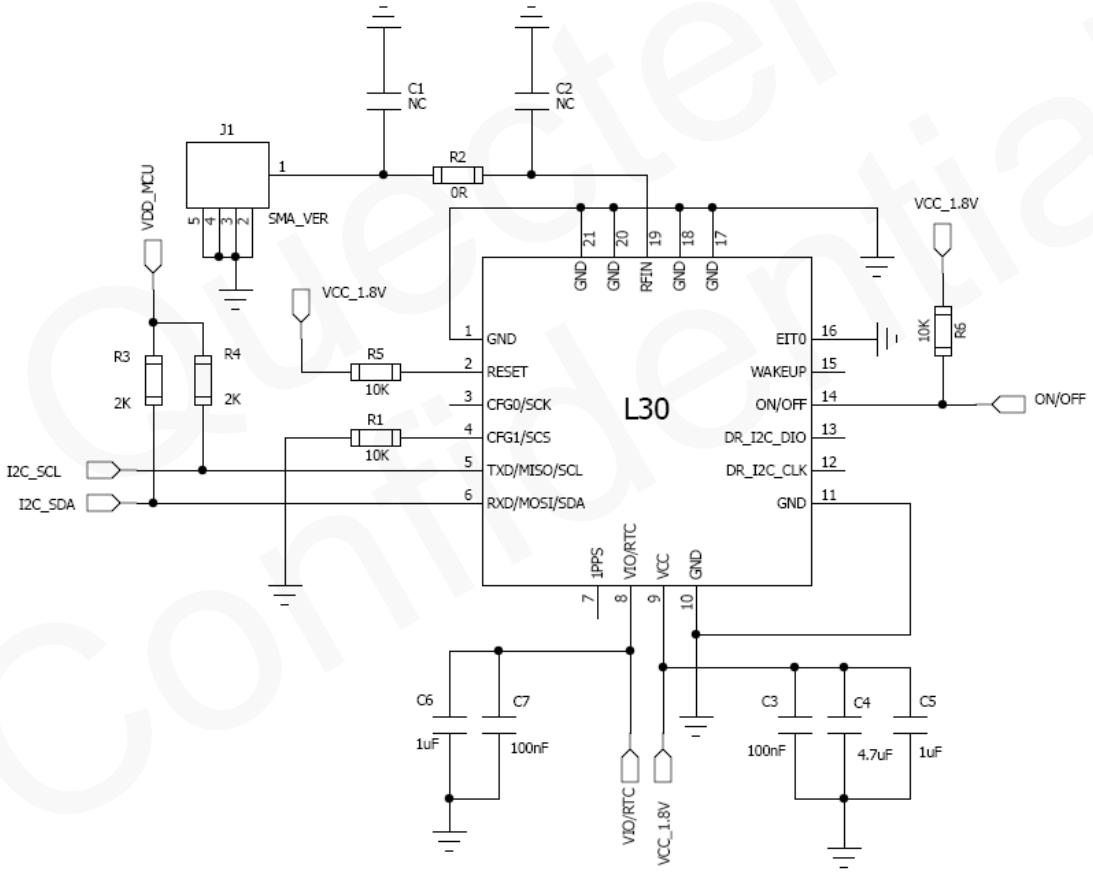


Figure 12: I2C design for L30 module

Note: The reference code of I2C will be released in the future, L30 does not support I2C at present.

3.7.3 SPI Interface

L30 provides SPI interface and is designed as a slave mode. The reference design is shown in Figure 14.

This SPI interface has the following features:

- An interrupt is provided when the transmit FIFO and output serial register (SR) are both empty.
- The transmitter and receiver have individual software-defined 2-byte idle patterns of 0xa7 0xb4.
- SPI detects synchronization errors and is reset by software.
- Supports both SPI and Microwire formats.
- Supports a maximum clock of 6.8MHz.
- Clock polarity: default SPI mode 1 (CPOL=0; CPHA=1).
- The output is CMOS 1.8V compatible and the input is 3.6V tolerant.

The following diagram is the timing sequence of SPI.

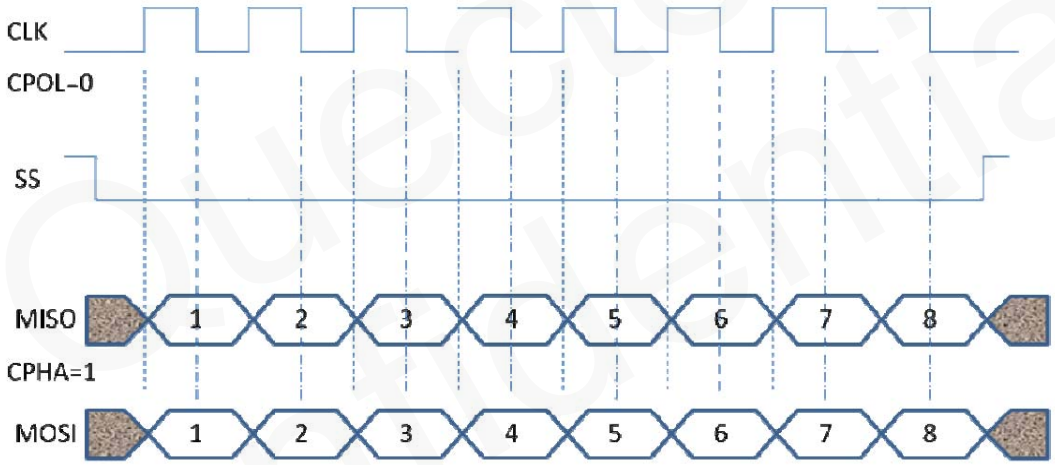


Figure 13: Timing sequence of SPI

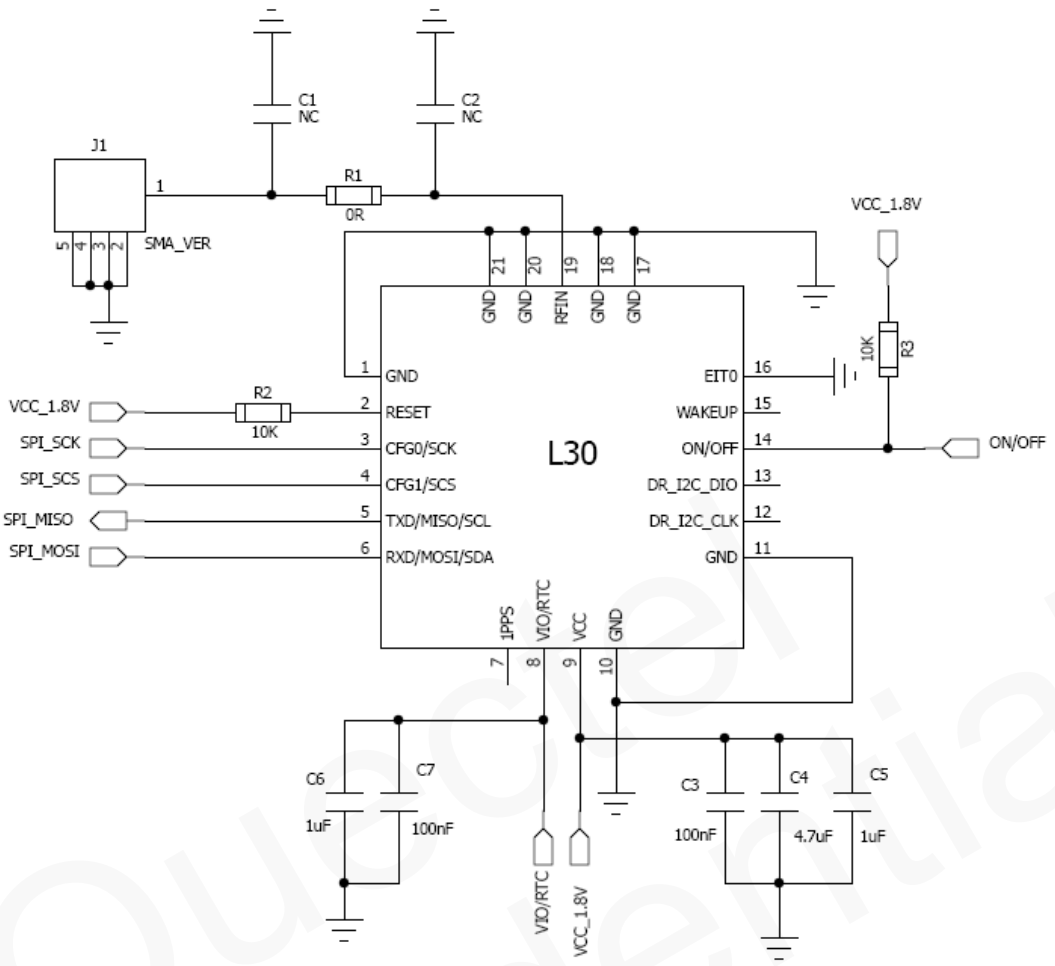


Figure 14: SPI design for L30 module

Note: The reference code of SPI will be released in the future, L30 does not support SPI at present.

3.8 Assisted GPS

By supplying aided information like ephemeris, almanac, rough last position, time and satellite status, A-GPS can help improving TTFF and the acquisition sensitivity of the GPS receiver.

L30 supports one kind of A-GPS called Client Generated Extended Ephemeris (CGEE) which ensures fast TTFF for 3 days .The CGEE data is generated internally from satellite ephemeris as a background task, and then L30 collects ephemeris from as many satellites as possible before entering Hibernate mode.

The CGEE feature requires that VIO/RTC power supply is kept active all the time and an external 1Mbit EEPROM connected to DR_I2C bus for CGEE data storage. The recommended EEPROM is in the following table and it is verified.

Table 10: Recommended EEPROM

Manufacturer	Part Number
ST	M24M01
Seiko Instruments Inc.	S-24CM01C
Atmel	AT24C1024B

Note: The part number which we recommend is a series part number, please get more details from the datasheet such as operation voltage and package.

Table 11: Pin definition of the DR_I2C interfaces

Interface	Name	Pin	Function
Dead Reckoning I2C Interface	DR_I2C_ DIO	13	I2C data (SDA)
	DR_I2C_ CLK	12	I2C clock (SCL)

The DR_I2C_DIO and DR_I2C_CLK pins are open-drain output and pulled up to VDD which depends on the EEPROM's operation voltage externally by 2K resistors to meet requirement of maximum data rate up to 400Kbs. The following circuit is the reference design between L30 and EEPROM.

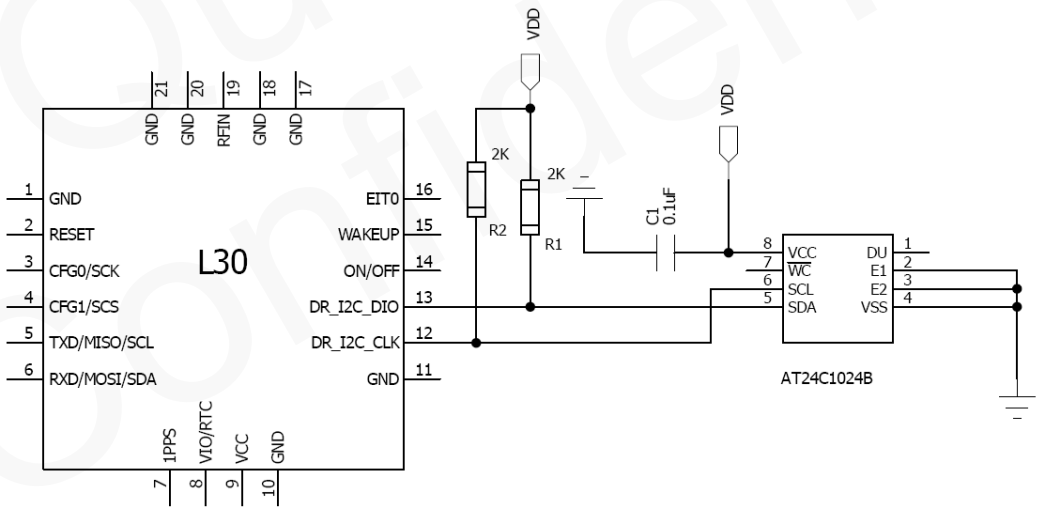


Figure 15: Reference design for CGEE function

4 Radio Frequency

L30 receives L1 band signal from GPS satellites at a nominal frequency of 1575.42MHz. The RF signal is connected to the RFIN pin. The input impedance of RFIN is 50Ω.

4.1 Antenna

L30 can be connected to passive or active antenna.

Table 12: Antenna specification for L30 module

Antenna type	Specification
Passive antenna	Center frequency: 1575.42 MHz Band Width: >20 MHz Gain: >0 dB Polarization: RHCP or Linear
Active antenna	Center frequency: 1575.42 MHz Band Width: >5 MHz Minimum gain: 15-20dB (compensate signal loss in RF cable) Maximum noise figure: 1.5dB Maximum gain: 50dB Polarization: RHCP or Linear

4.2 Antenna Reference Design

4.2.1 Passive Antenna

Connecting a passive antenna does not require a DC bias voltage and the antenna can be connected to RFIN pin directly. It is always beneficial to reserve a passive matching network between the antenna and the RFIN interface of the module. The reference design is shown in Figure 16.

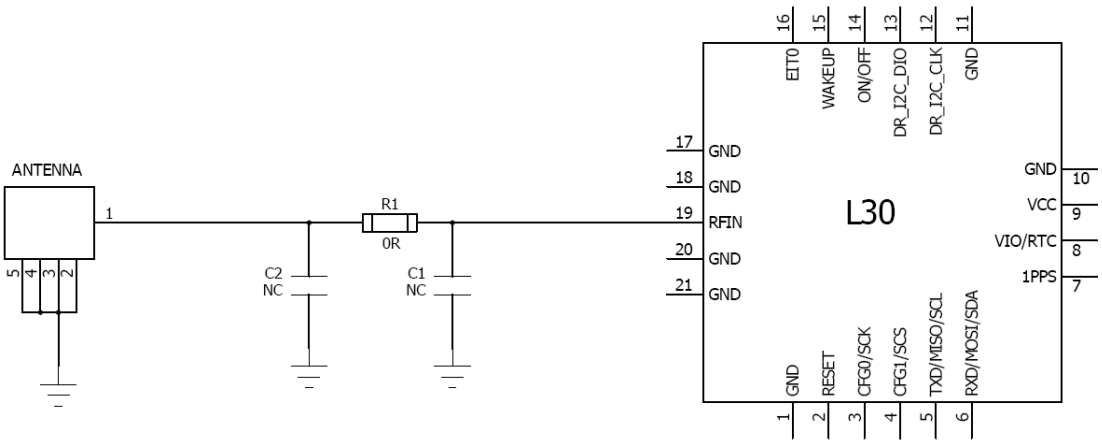


Figure 16: Reference design for passive antenna

4.2.2 Active Antenna

Active antenna could be connected to RFIN directly. If an active antenna is connected to RFIN, the integrated low-noise amplifier of the antenna must be powered by a external correct supply voltage. Generally, the supply voltage is fed to the antenna through the coaxial RF cable. An active antenna's loading current is between 5mA to 20mA. The inductor outside of the module prevents the RF signal from leaking into the VCC_ANT pin and routes the bias supply to the active antenna. Please refer to the reference circuit shown in Figure 17.

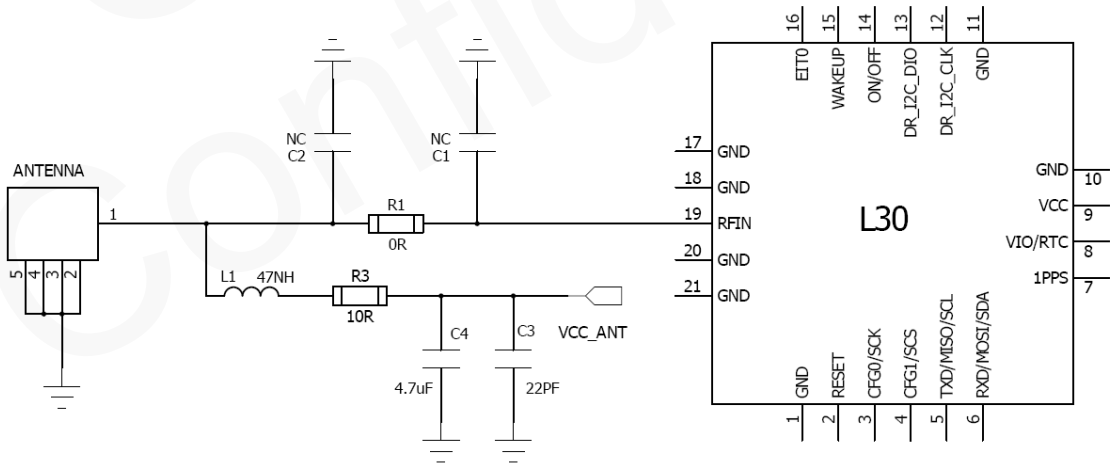


Figure 17: Reference design for active antenna with external power

Note: The rated power of resistor R3 should be chosen no less than 1 watt in case active antenna is shorted unexpectedly.

4.3 External LNA

If a passive antenna is adopted in customer's application, an LNA could be inserted between the antenna and pin RFIN of L30 to improve the general sensitivity by 2~3dB. A reference schematic diagram based on the LNA BGA715L7 manufactured by INFINEON is given as Figure 18. Here, the gain of LNA is 20 dB, noise figure is 0.75 dB, current consumption is 3.3 mA, and range of power supply is 1.5 V to 3.3 V. Generally, the customer can get a good effective performance by using the default value marked in the reference design. Note that the interelectrode capacitance of TVS1 should be less than 0.5pF.

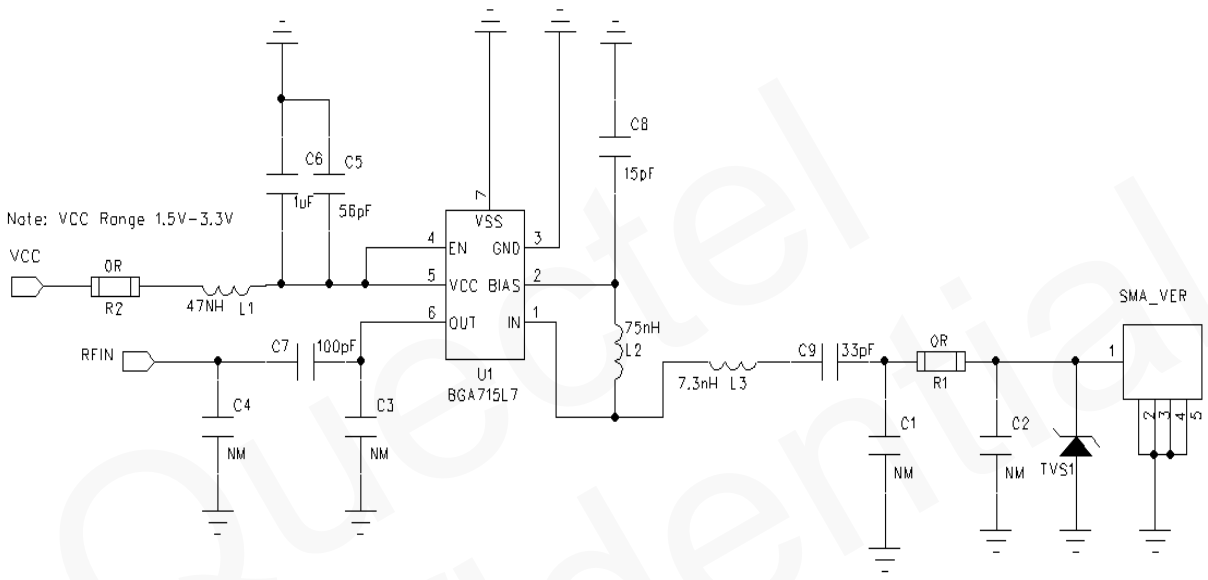


Figure 18: Reference design for external LNA

5 Electrical, Reliability and Radio Characteristics

5.1 Absolute Maximum Ratings

Absolute maximum rating for power supply and voltage on digital pins of the module are listed in the following table.

Table 13: Absolute maximum ratings

Parameter	Min	Max	Unit
Power supply voltage （VCC）	-0.3	2	V
Backup battery voltage (VIO/RTC)	-0.3	2	V
Input voltage at digital pins	-0.5	3.6	V
Input power at RFIN (Prfin)	—	10	dBm
Storage temperature	-45	125	°C

Note: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. The product is not protected against over voltage or reversed voltage. If necessary, voltage spikes exceeding the power supply voltage specification, given in table above, must be limited to values within the specified boundaries by using appropriate protection diodes.

5.2 Operating Conditions

Table 14: The module power supply ratings

Parameter	Description	Conditions	Min	Typ	Max	Unit
VCC	Supply voltage	Voltage must stay within the min/max values, including voltage drop, ripple, and spikes.	1.71	1.8	1.89	V
I_{VCC}	Peak supply current	VCC=1.8V@-140dBm	—	—	54	mA
VIO/RTC	Backup voltage supply		1.71	1.8	1.89	V
$I_{VIO/RTC}$	Backup battery current	VIO/RTC=1.8V In hibernate mode	—	15	—	uA
T_{OPR}	Normal Operating temperature		-40	25	85	°C

Note: Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

5.3 Current Consumption

Table 15: The module current consumption (passive antenna)

Parameter	Condition	Min	Typ	Max	Unit
Itotal Acquisition	Open sky @-130dBm	-	40	-	mA
Itotal Tracking	Open sky@-130dBm	-	36	-	mA
Hibernate	Open sky@-130dBm		17		uA

Note: Itotal=Ivcc+Ivio/rtc

5.4 Electro-Static Discharge

L30 module is ESD sensitive device, ESD protection precautions should be emphasized. Proper ESD handing and packaging procedures must be applied throughout the processing, handing and operation of any application.

The ESD bearing capability of the module is listed in the following table. Note that the customer should add ESD components to module pins in detail application except RFIN, VCC and GND pins.

Table 16: The ESD endurance table (Temperature: 25°C, Humidity: 45 %)

Pin	Contact discharge	Air discharge
RFIN	±5KV	±8K
VCC, GND	±4KV	±8K

5.5 Reliability Test

Table 17: Reliability test

Test term	Condition	Standard
Thermal shock	-30°C...+80°C, 144 cycles	GB/T 2423.22-2002 Test Na IEC 68-2-14 Na
Damp heat, cyclic	+55°C; >90% Rh 6 cycles for 144 hours	IEC 68-2-30 Db Test
Vibration shock	5~20Hz,0.96m^2/s^3;20~500Hz,0.96m^2/s^3-3dB/oct, 1hour/axis; no function	2423.13-1997 Test Fdb IEC 68-2-36 Fdb Test
Heat test	85°C, 2 hours, Operational	GB/T 2423.1-2001 Ab IEC 68-2-1 Test
Cold test	-40°C, 2 hours, Operational	GB/T 2423.1-2001 Ab IEC 68-2-1 Test
Heat soak	90°C, 72 hours, Non-Operational	GB/T 2423.2-2001 Bb IEC 68-2-2 Test B
Cold soak	-45°C, 72 hours, Non-Operational	GB/T 2423.1-2001 A IEC 68-2-1 Test

6 Mechanics

This chapter describes the mechanical dimensions of the module.

6.1 Mechanical Dimensions of the Module

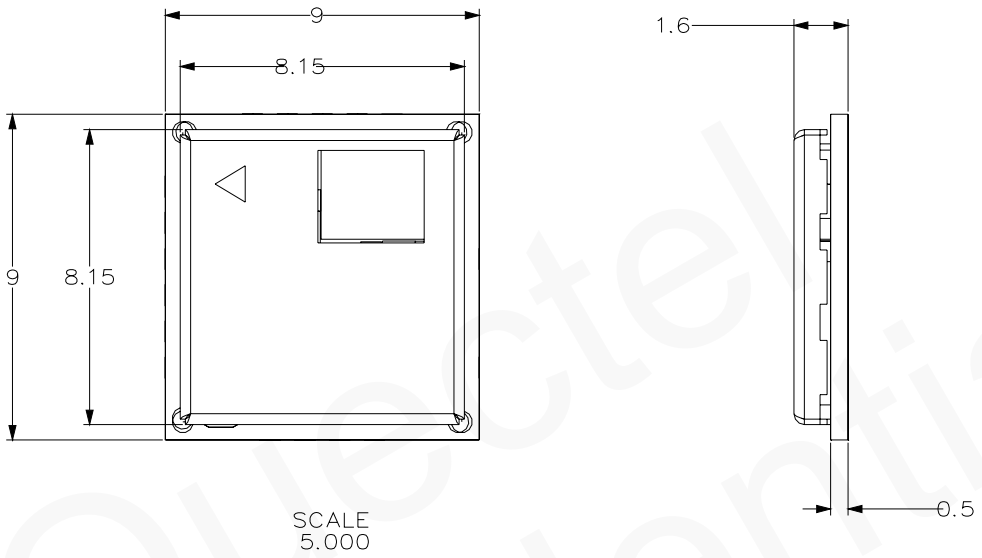


Figure 19: L30 Top view and Side view（Unit:mm）

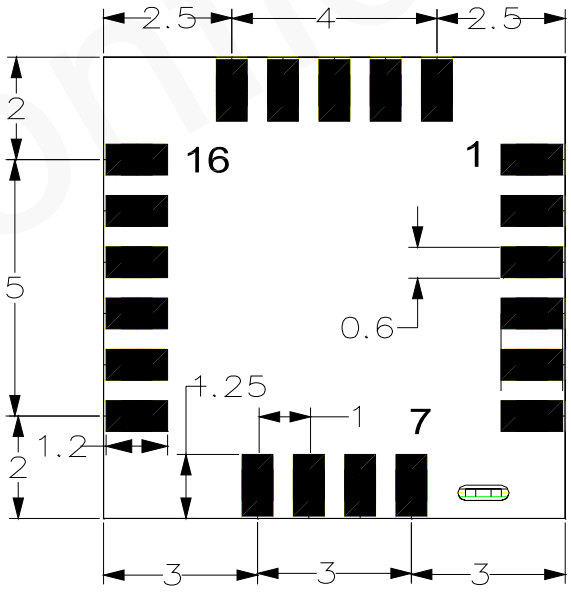


Figure 20: L30 Bottom view（Unit:mm）

6.2 Footprint of Recommendation

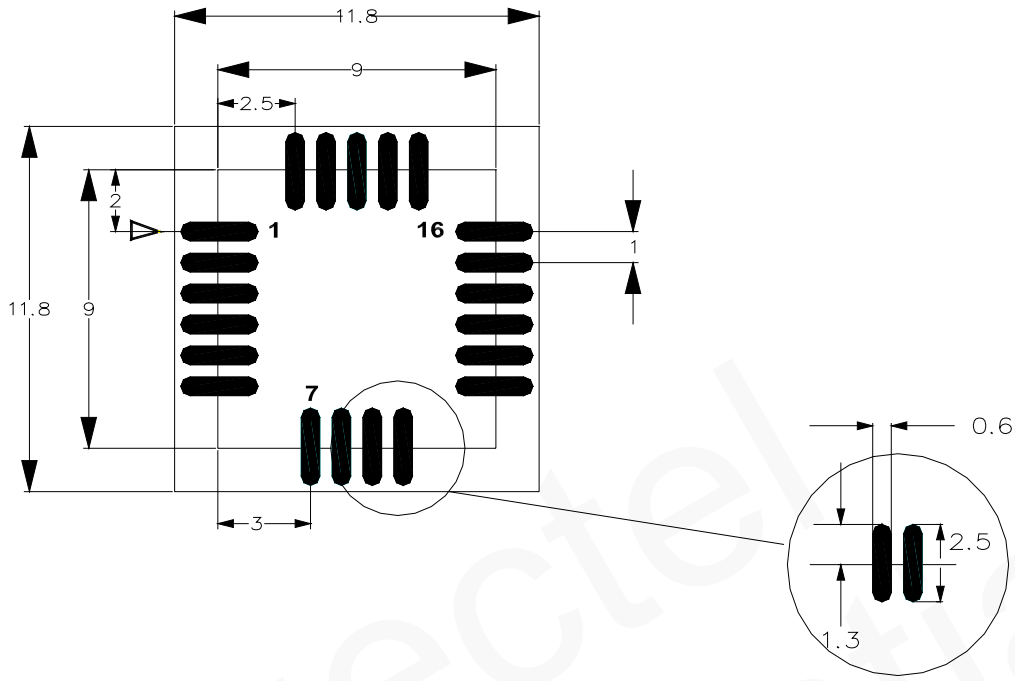


Figure 21: Footprint of recommendation（Unit:mm）

Note：Keep out on the host board below the module and the keep-out area should be covered by solder mask and top silk layer for isolation between the top layer of host board and the bottom layer of the module.

6.3 Top View of the Module

Figure 22: Top view of module

6.4 Bottom View of the Module

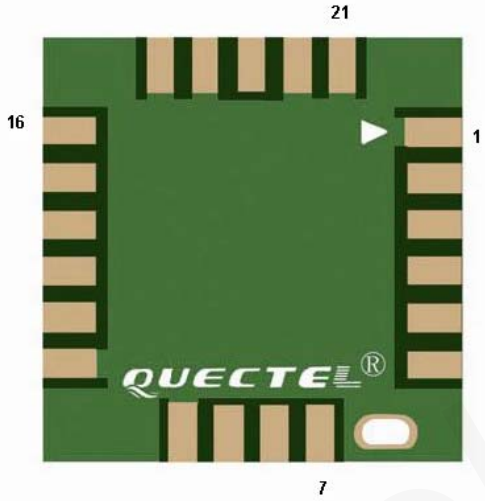


Figure 23: Bottom view of module

7 Manufacture

7.1 Assembly and Soldering

L30 is intended for SMT assembly and soldering in a Pb-free reflow process on the top side of the PCB. It is suggested that solder paste stencil height is 130um minimum to ensure sufficient solder volume. Paste mask pad openings can be increased to ensure proper soldering and solder wetting over pads. Suggest peak reflow temperature is 235…245ºC (for SnAg3.0Cu0.5 alloy). Absolute max reflow temperature is 260ºC. To avoid damage to the module when it was repeatedly heated, it is suggested that the module should be mounted after the first panel has been reflowed. The following picture is the actual diagram which we have operated.

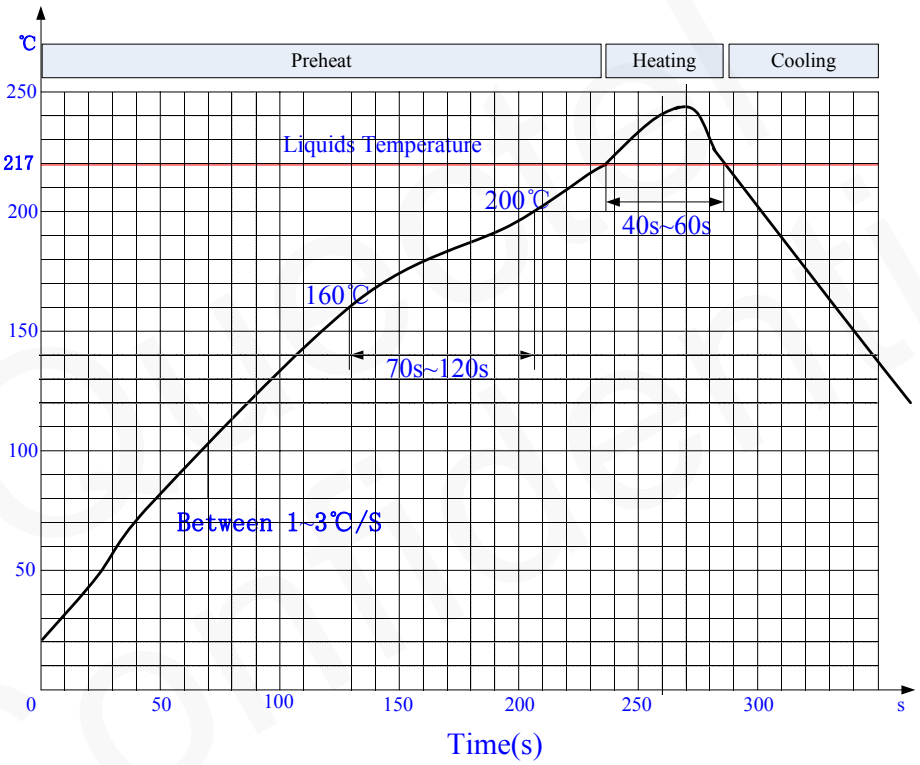


Figure 24: Ramp-soak-spike-reflow of furnace temperature

7.2 Moisture Sensitivity

L30 is sensitivity to moisture absorption. To prevent L30 from permanent damage during reflow soldering, baking before reflow is required in following cases:

- Humidity indicator card: At least one circular indicator is no longer blue
- The seal is opened and the module is exposed to excessive humidity.

L30 should be baked for 192 hours at temperature 40℃+5℃/-0℃ and <5% RH in low-temperature containers, or 24 hours at temperature 125℃±5℃ in high-temperature containers. Care should be

taken that plastic tray is not heat resistant. L30 should be taken out before preheating, otherwise, the tray maybe damaged by high-temperature heating.

7.3 ESD Safe

L30 module is an ESD sensitive device and should be careful to handle.

7.4 Tape and Reel

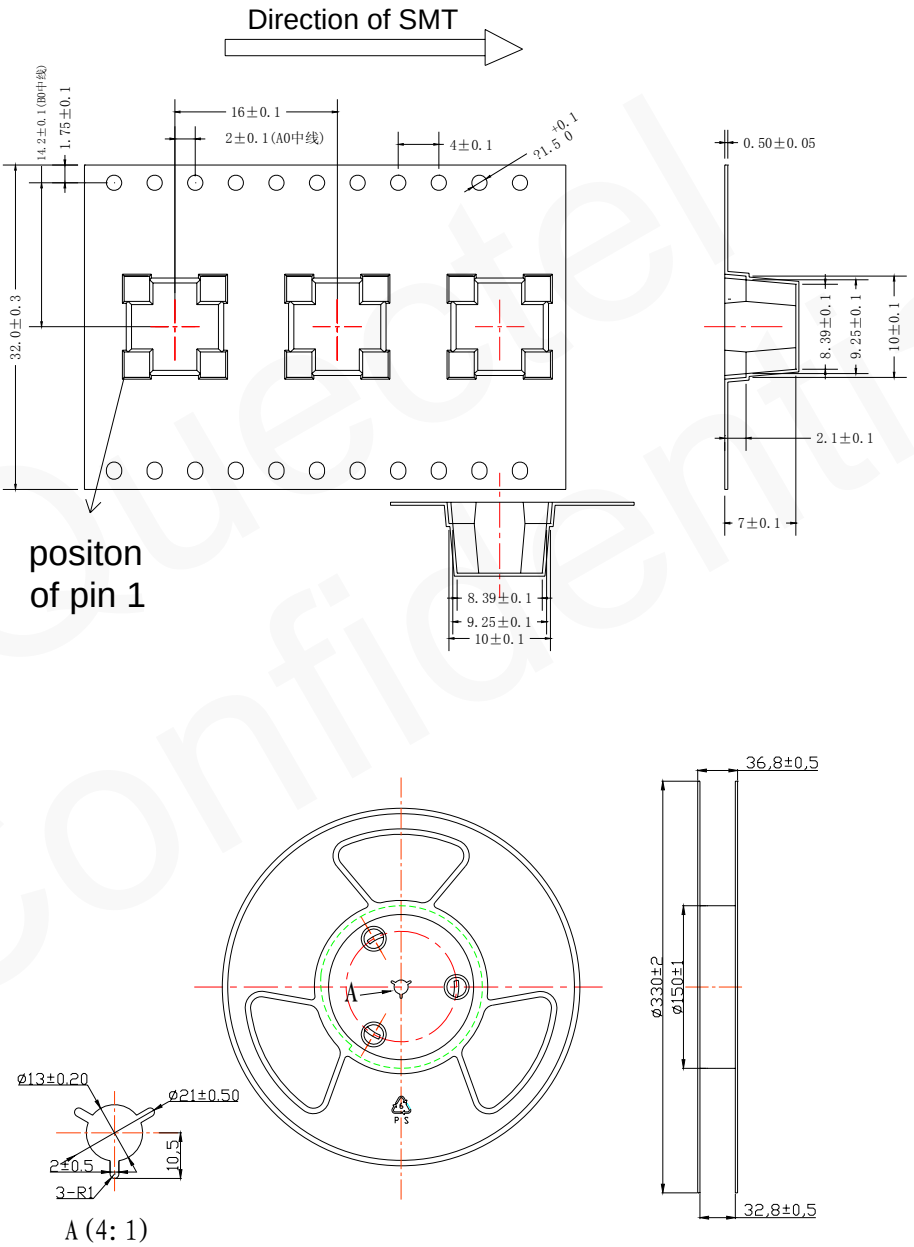


Figure 25: Tape and reel specification

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