

DATA SHEET

74HC32; 74HCT32 Quad 2-input OR gate

Product specification
Supersedes data of 2003 Aug 29

2003 Dec 12

Quad 2-input OR gate

74HC32; 74HCT32

FEATURES

- Wide supply voltage range from 2.0 to 6.0 V
- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- ESD protection:
HBM EIA/JESD22-A114-A exceeds 2000 V
MM EIA/JESD22-A115-A exceeds 200 V.

GENERAL DESCRIPTION

The 74HC/HCT32 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT32 provides the 2-input OR function.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f = 6\text{ ns}$.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$	6	9	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	16	28	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

2. For 74HC32 the condition is $V_I = \text{GND to } V_{CC}$.

For 74HCT32 the condition is $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$.

FUNCTION TABLE

See note 1.

INPUT		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

Note

1. H = HIGH voltage level;
L = LOW voltage level.

Quad 2-input OR gate

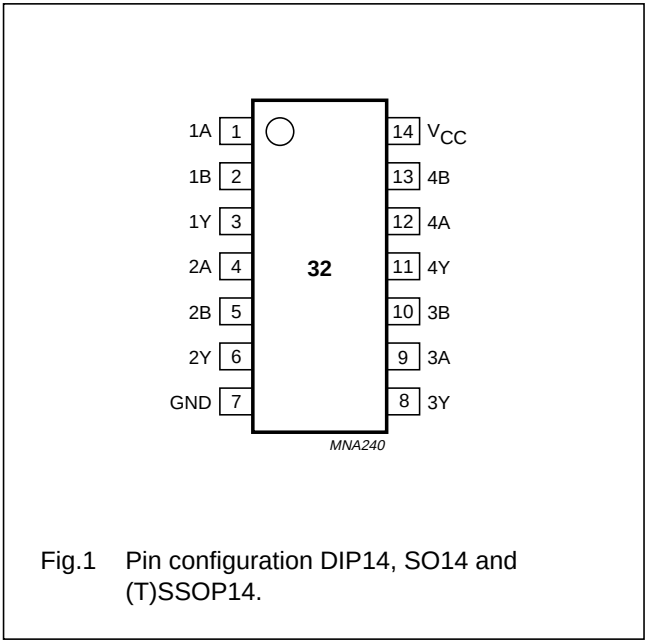
74HC32; 74HCT32

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74HC32N	−40 to +125 °C	14	DIP14	plastic	SOT27-1
74HCT32N	−40 to +125 °C	14	DIP14	plastic	SOT27-1
74HC32D	−40 to +125 °C	14	SO14	plastic	SOT108-1
74HCT32D	−40 to +125 °C	14	SO14	plastic	SOT108-1
74HC32DB	−40 to +125 °C	14	SSOP14	plastic	SOT337-1
74HCT32DB	−40 to +125 °C	14	SSOP14	plastic	SOT337-1
74HC32PW	−40 to +125 °C	14	TSSOP14	plastic	SOT402-1
74HCT32PW	−40 to +125 °C	14	TSSOP14	plastic	SOT402-1
74HC32BQ	−40 to +125 °C	14	DHVQFN14	plastic	SOT762-1
74HCT32BQ	−40 to +125 °C	14	DHVQFN14	plastic	SOT762-1

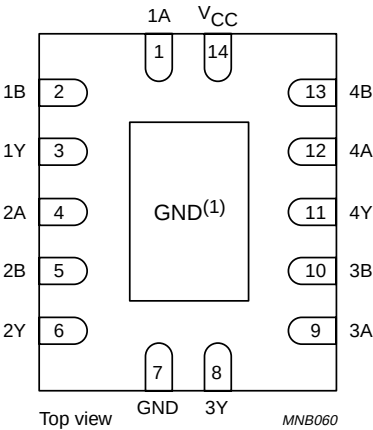
PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	1B	data input
3	1Y	data output
4	2A	data input
5	2B	data input
6	2Y	data output
7	GND	ground (0 V)
8	3Y	data output
9	3A	data input
10	3B	data input
11	4Y	data output
12	4A	data input
13	4B	data input
14	V _{CC}	supply voltage



Quad 2-input OR gate

74HC32; 74HCT32



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN14.

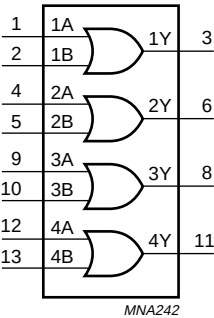


Fig.3 Logic symbol.

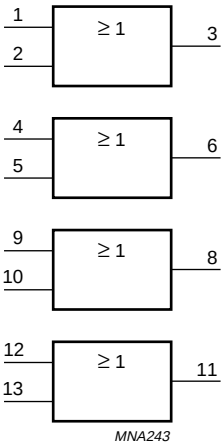


Fig.4 Logic symbol (IEEE/IEC).

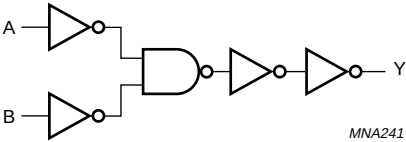


Fig.5 Logic diagram (one gate).

Quad 2-input OR gate

74HC32; 74HCT32

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC32			74HCT32			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	–	V_{CC}	0	–	V_{CC}	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	operating ambient temperature		–40	+25	+125	–40	+25	+125	°C
t_r, t_f	input rise and fall times	$V_{CC} = 2.0\text{ V}$	–	–	1000	–	–	–	ns
		$V_{CC} = 4.5\text{ V}$	–	6.0	500	–	6.0	500	ns
		$V_{CC} = 6.0\text{ V}$	–	–	400	–	–	–	ns

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
I_{IK}	input diode current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$; note 1	–	±20	mA
I_{OK}	output diode current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$; note 1	–	±20	mA
I_O	output source or sink current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$; note 1	–	±25	mA
$I_{CC}; I_{GND}$	V_{CC} or GND current	note 1	–	±50	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	$T_{amb} = -40\text{ to }+125\text{ °C}$; note 2	–	300	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For DIP14 packages: above 70 °C the value of P_{tot} derates linearly with 12 mW/K.
 For SO14 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
 For SSOP14 and TSSOP14 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
 For DHVQFN14 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

Quad 2-input OR gate

74HC32; 74HCT32

DC CHARACTERISTICS

Family 74HC

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = 25 °C; note 1							
V _{IH}	HIGH-level input voltage		2.0	1.5	1.2	–	V
			4.5	3.15	2.4	–	V
			6.0	4.2	3.2	–	V
V _{IL}	LOW-level input voltage		2.0	–	0.8	0.5	V
			4.5	–	2.1	1.35	V
			6.0	–	2.8	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = –20 μA	2.0	1.9	2.0	–	V
		I _O = –20 μA	4.5	4.4	4.5	–	V
		I _O = –20 μA	6.0	5.9	6.0	–	V
		I _O = –4.0 mA	4.5	3.98	4.32	–	V
		I _O = –5.2 mA	6.0	5.48	5.81	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = 20 μA	2.0	–	0	0.1	V
		I _O = 20 μA	4.5	–	0	0.1	V
		I _O = 20 μA	6.0	–	0	0.1	V
		I _O = 4.0 mA	4.5	–	0.15	0.26	V
		I _O = 5.2 mA	6.0	–	0.16	0.26	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	6.0	–	–	±0.1	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	6.0	–	–	2.0	μA

Quad 2-input OR gate

74HC32; 74HCT32

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = −40 to +85 °C							
V _{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			4.5	3.15	–	–	V
			6.0	4.2	–	–	V
V _{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			4.5	–	–	1.35	V
			6.0	–	–	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = −20 μA I _O = −20 μA I _O = −20 μA I _O = −4.0 mA I _O = −5.2 mA	2.0	1.9	–	–	V
			4.5	4.4	–	–	V
			6.0	5.9	–	–	V
			4.5	3.84	–	–	V
			6.0	5.34	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 20 μA I _O = 20 μA I _O = 20 μA I _O = 4.0 mA I _O = 5.2 mA	2.0	–	–	0.1	V
			4.5	–	–	0.1	V
			6.0	–	–	0.1	V
			4.5	–	–	0.33	V
			6.0	–	–	0.33	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	6.0	–	–	±1.0	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	6.0	–	–	20	μA

Quad 2-input OR gate

74HC32; 74HCT32

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = −40 to +125 °C							
V _{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			4.5	3.15	–	–	V
			6.0	4.2	–	–	V
V _{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			4.5	–	–	1.35	V
			6.0	–	–	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = −20 μA I _O = −20 μA I _O = −20 μA I _O = −4.0 mA I _O = −5.2 mA	2.0	1.9	–	–	V
			4.5	4.4	–	–	V
			6.0	5.9	–	–	V
			4.5	3.7	–	–	V
			6.0	5.2	–	–	V
			V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 20 μA I _O = 20 μA I _O = 20 μA I _O = 4.0 mA I _O = 5.2 mA	2.0	–
4.5	–	–				0.1	V
6.0	–	–				0.1	V
4.5	–	–				0.4	V
6.0	–	–				0.4	V
I _{LI}	input leakage current	V _I = V _{CC} or GND				6.0	–
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	6.0	–	–	40	μA

Note

1. All typical values are measured at T_{amb} = 25 °C.

Quad 2-input OR gate

74HC32; 74HCT32

Family 74HCT

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = 25 °C; note 1							
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	1.6	–	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	–	1.2	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = –20 μA	4.5	4.4	4.5	–	V
		I _O = –4 mA	4.5	3.98	4.32	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = 20 μA	4.5	–	0	0.1	V
		I _O = 4 mA	4.5	–	0.15	0.25	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	5.5	–	–	±0.1	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	2.0	μA
ΔI _{CC}	additional quiescent supply current per input	V _I = V _{CC} – 2.1 V; I _O = 0	4.5 to 5.5	–	–	430	μA
T _{amb} = –40 to +85 °C							
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = –20 μA	4.5	4.4	–	–	V
		I _O = –4 mA	4.5	3.84	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = 20 μA	4.5	–	–	0.1	V
		I _O = 4 mA	4.5	–	–	0.33	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	5.5	–	–	±1.0	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	20	μA
ΔI _{CC}	additional quiescent supply current per input	V _I = V _{CC} – 2.1 V; I _O = 0	4.5 to 5.5	–	–	540	μA

Quad 2-input OR gate

74HC32; 74HCT32

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = −40 to +125 °C							
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = −20 μA	4.5	4.4	–	–	V
		I _O = −4 mA	4.5	3.7	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 20 μA	4.5	–	–	0.1	V
		I _O = 4 mA	4.5	–	–	0.4	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	5.5	–	–	±1.0	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	40	μA
ΔI _{CC}	additional quiescent supply current per input	V _I = V _{CC} − 2.1 V; I _O = 0	4.5 to 5.5	–	–	590	μA

Note

1. All typical values are measured at $T_{amb} = 25$ °C.

Quad 2-input OR gate

74HC32; 74HCT32

AC CHARACTERISTICS

Family 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
T _{amb} = 25 °C; note 1							
t _{PHL} /t _{PLH}	propagation delay nA, nB to nY	see Figs 6 and 7	2.0	–	22	90	ns
			4.5	–	8	18	ns
			6.0	–	6	15	ns
t _{THL} /t _{TLH}	output transition time	see Figs 6 and 7	2.0	–	19	75	ns
			4.5	–	7	15	ns
			6.0	–	6	13	ns
T _{amb} = –40 to +85 °C							
t _{PHL} /t _{PLH}	propagation delay nA, nB to nY	see Figs 6 and 7	2.0	–	–	115	ns
			4.5	–	–	23	ns
			6.0	–	–	20	ns
t _{THL} /t _{TLH}	output transition time	see Figs 6 and 7	2.0	–	–	95	ns
			4.5	–	–	19	ns
			6.0	–	–	16	ns
T _{amb} = –40 to +125 °C							
t _{PHL} /t _{PLH}	propagation delay nA, nB to nY	see Figs 6 and 7	2.0	–	–	135	ns
			4.5	–	–	27	ns
			6.0	–	–	23	ns
t _{THL} /t _{TLH}	output transition time	see Figs 6 and 7	2.0	–	–	110	ns
			4.5	–	–	22	ns
			6.0	–	–	19	ns

Note

1. All typical values are measured at $T_{amb} = 25$ °C.

Quad 2-input OR gate

74HC32; 74HCT32

Family 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
T _{amb} = 25 °C; note 1							
t _{PHL} /t _{PLH}	propagation delay nA, nB to nY	see Figs 6 and 7	4.5	–	11	24	ns
t _{THL} /t _{TLH}	output transition time	see Figs 6 and 7	4.5	–	7	15	ns
T _{amb} = –40 to +85 °C							
t _{PHL} /t _{PLH}	propagation delay nA, nB to nY	see Figs 6 and 7	4.5	–	–	30	ns
t _{THL} /t _{TLH}	output transition time	see Figs 6 and 7	4.5	–	–	19	ns
T _{amb} = –40 to +125 °C							
t _{PHL} /t _{PLH}	propagation delay nA, nB to nY	see Figs 6 and 7	4.5	–	–	36	ns
t _{THL} /t _{TLH}	output transition time	see Figs 6 and 7	4.5	–	–	22	ns

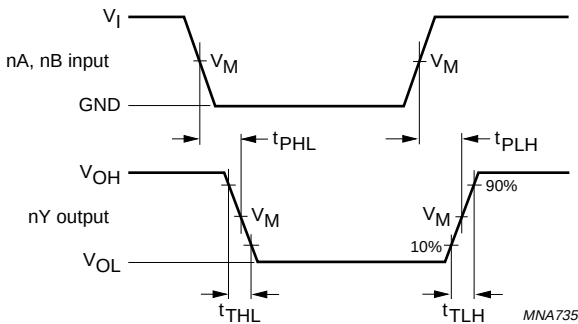
Note

1. All typical values are measured at $T_{amb} = 25$ °C.

Quad 2-input OR gate

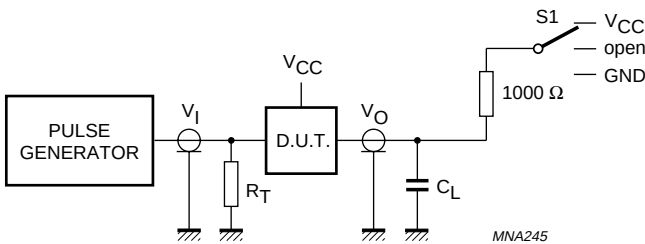
74HC32; 74HCT32

AC WAVEFORMS



74HC32 : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
74HCT32: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.6 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.



TEST	S1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

Definitions for test circuit:
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.7 Load circuitry for switching times.

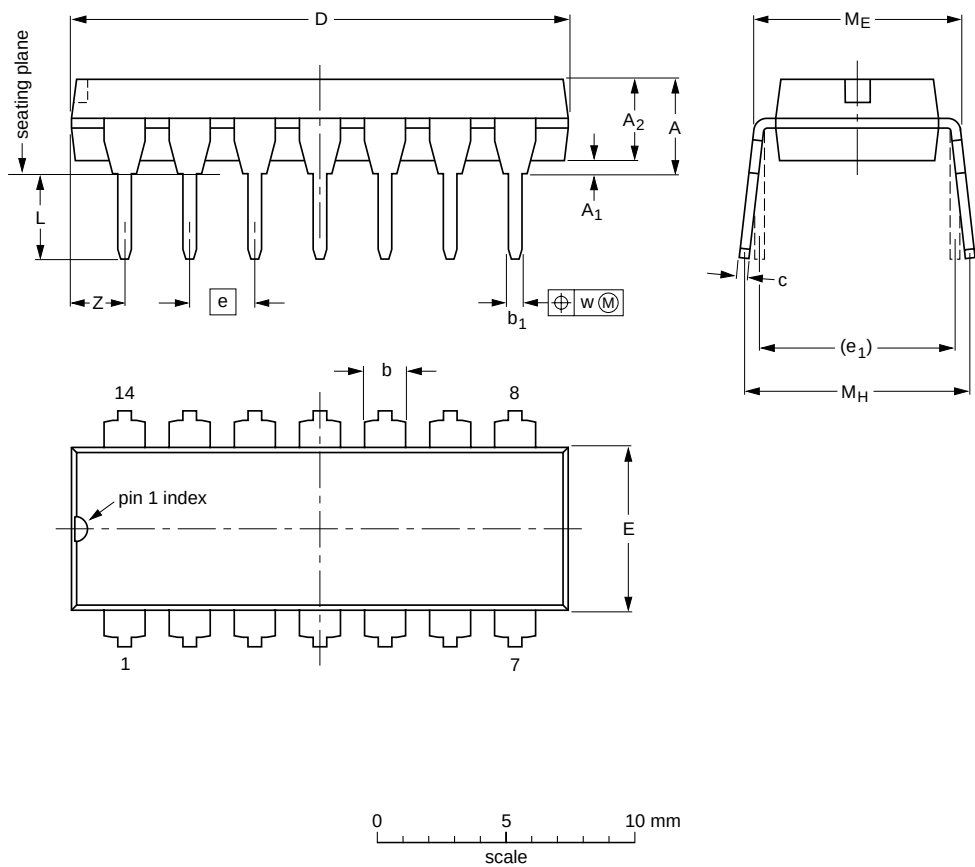
Quad 2-input OR gate

74HC32; 74HCT32

PACKAGE OUTLINES

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

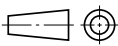


DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

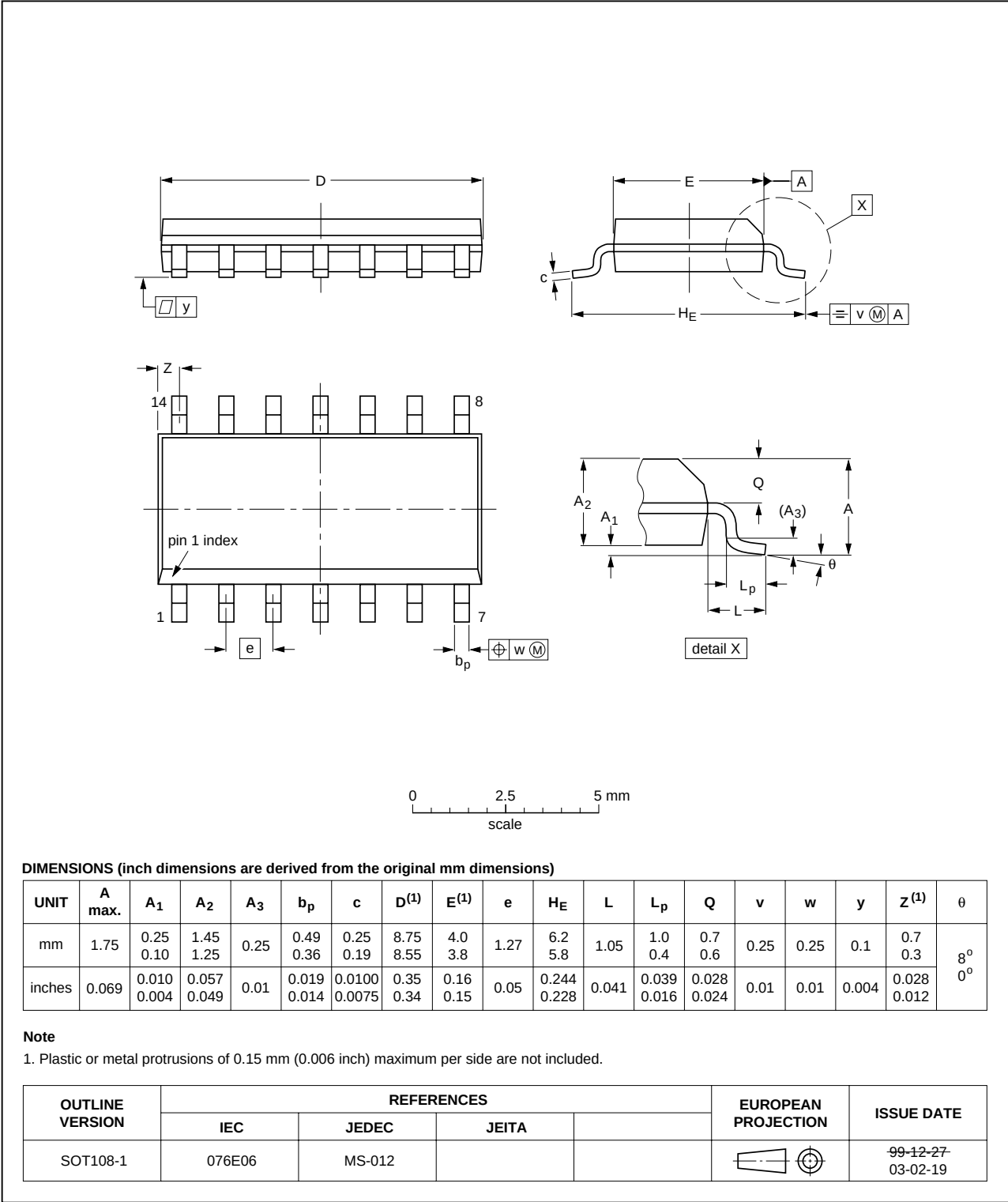
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			99-12-27 03-02-13

Quad 2-input OR gate

74HC32; 74HCT32

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

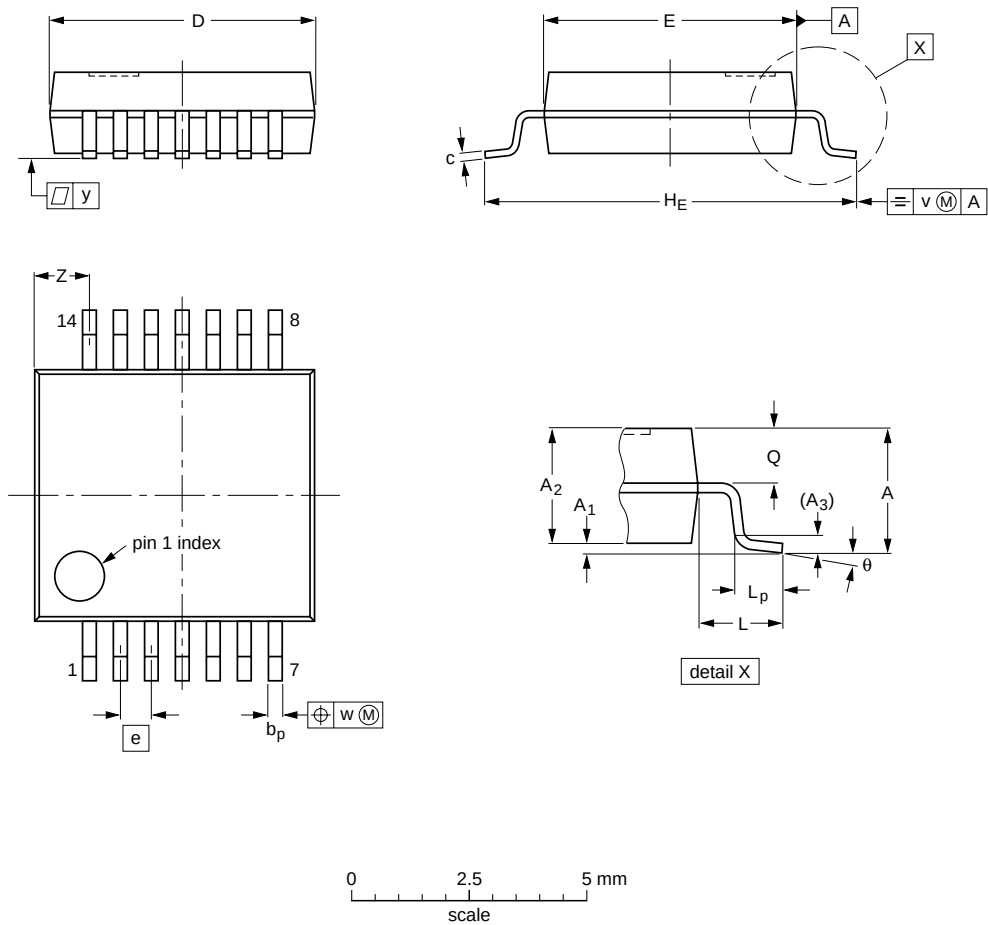


Quad 2-input OR gate

74HC32; 74HCT32

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

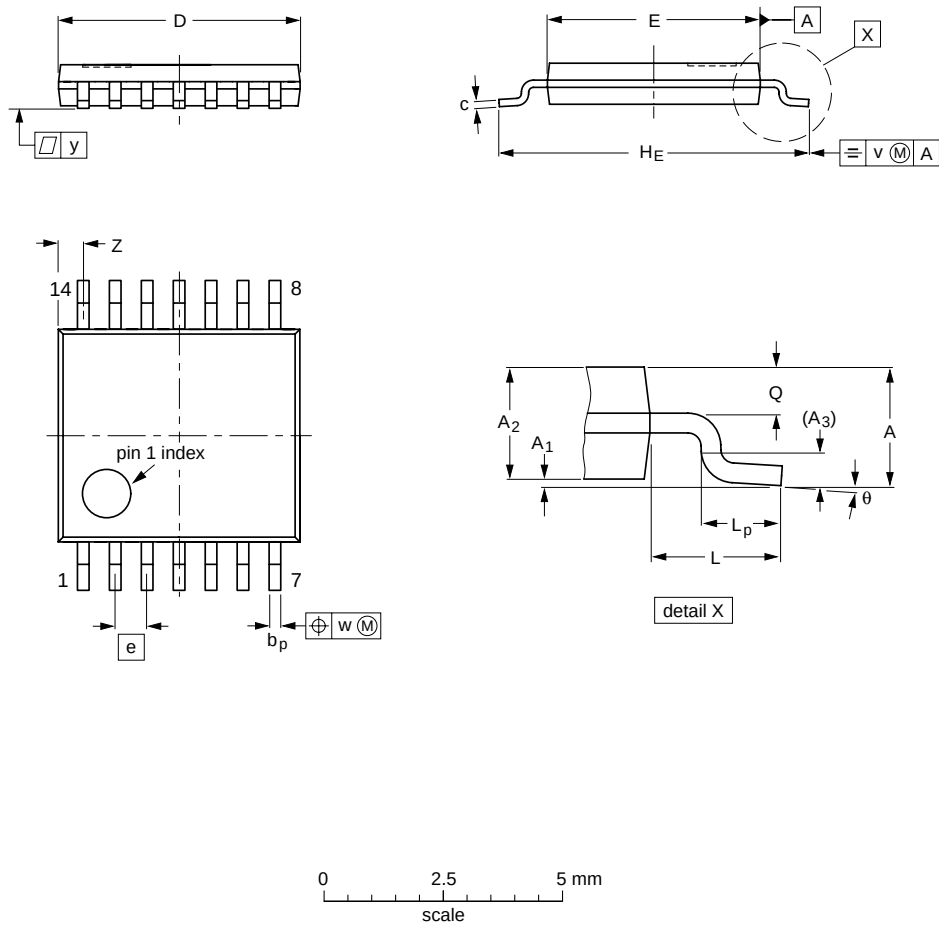
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				99-12-27 03-02-19

Quad 2-input OR gate

74HC32; 74HCT32

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

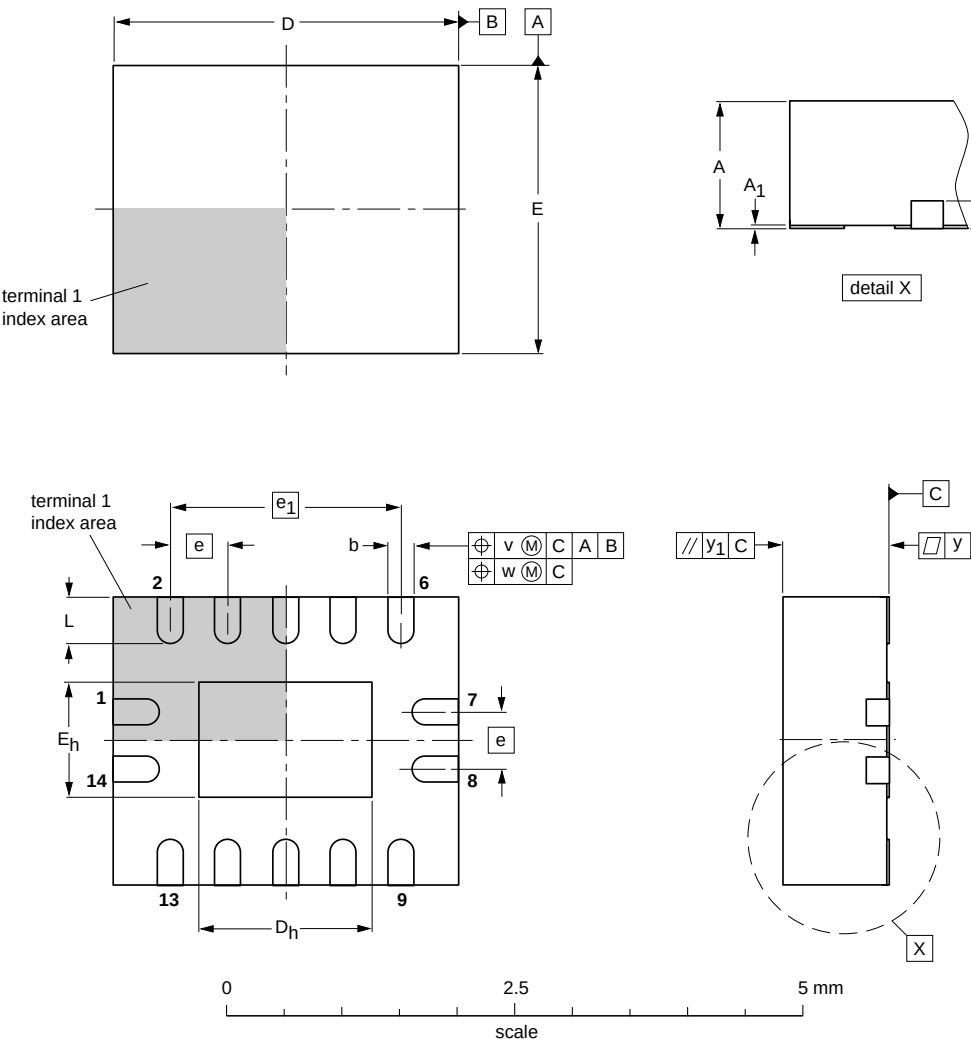
- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				99-12-27 03-02-18

Quad 2-input OR gate

74HC32; 74HCT32

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm SOT762-1



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾ max.	A ₁	b	c	D ⁽¹⁾	D _h	E ⁽¹⁾	E _h	e	e ₁	L	v	w	y	y ₁
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	---	MO-241	---			02-10-17 03-01-27

Quad 2-input OR gate

74HC32; 74HCT32

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors – a worldwide company

Contact information

For additional information please visit <http://www.semiconductors.philips.com>. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to: sales.addresses@www.semiconductors.philips.com.

© Koninklijke Philips Electronics N.V. 2003

SCA75

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

R44/04/pp20

Date of release: 2003 Dec 12

Document order number: 9397 750 12488

Let's make things better.

**Philips
Semiconductors**



PHILIPS