

AT65-0233
V5

SO-16

- Attenuation: 2.0 dB steps to 30 dB
- Low DC Power Consumption
- Integral TTL Driver
- 50 Ohm Impedance
- Temperature Stability: ± 0.18 dB from -55°C to $+85^{\circ}\text{C}$ Typ.

MECHANICAL DRAWING OF THE 74VHC00 PACKAGE. The drawing includes a top view, a side view, and a detail view of the package body.

Top View Dimensions:

- Pin 16 to Pin 1 distance: .1497-.1574 (3.80-4.00)
- Pin 16 to Pin 1 distance: .2284-.2340 (5.80-6.20)
- Pin 16 to Pin 1 distance: .0010 (0.2539)
- Pin 16 to Pin 1 distance: .3859-.3937 (9.80-10.00)
- Pin 16 to Pin 1 distance: .0532-.0688 (1.39-1.75)
- Pin 16 to Pin 1 distance: .0049 (0.10)
- Pin 16 to Pin 1 distance: .0040-.0118 (0.10-0.30)
- Pin 16 to Pin 1 distance: .013-.020 TYP. (0.33-.51)
- Pin 16 to Pin 1 distance: .050 (1.27) BSC

Side View Dimensions:

- Pin 16 to Pin 1 distance: .0096-.0196 x 45° CHAMFER (0.25-.50)
- Pin 16 to Pin 1 distance: .0075-.009 (0.19-.25)
- Pin 16 to Pin 1 distance: .016-.050 (0.40-1.27)

Orientation Mark: A circle with a dot is located near Pin 1.

Package conforms to JEDEC standard MS-012AC

MA-COM's AT65-0233 is a GaAs FET 4-bit digital attenuator with a 2.0 dB minimum step size and a 30 dB total attenuation range. This device is in a SOIC-16 plastic surface mount package. The AT65-0233 is ideally suited for use where accuracy, fast speed, very low power consumption and low costs are required. Typical applications include dynamic range setting in precision receiver circuits and other gain/leveling control circuits.

Absolute Maximum Ratings ¹

Pin No.	Function	Pin No.	Function
1	GND	9	C2
2	RF1	10	C1
3	GND	11	GND
4	N/C	12	GND
5	Vee	13	N/C
6	Vcc	14	GND
7	C4	15	RF2
8	C3	16	GND

N/C = No Connection

Parameter	Absolute Maximum
Max. Input Power 0.05 GHz 0.5 - 3.0 GHz	+27 dBm +34 dBm
+Vcc	+5.5V
-Vee	-8.5V
Control Voltage ²	-0.5 to Vcc to +0.5V
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +125°C

1. Operation of this device above any one of these parameters may cause perament damage.
2. Standard CMOS TTL interface, latch-up will occur if logic signal is applied prior to power supply.

**Digital Attenuator, 30 dB, 4-Bit, TTL Driver,
 DC - 3.0 GHz**
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Electrical Specifications: T_A = 25°C

Parameter	Test Conditions	Frequency	Units	Min.	Typ.	Max.
Insertion Loss	—	DC - 0.5 GHz DC - 2.0 GHz DC - 3.0 GHz	dB dB dB	— — —	1.7 2.3 2.6	2.0 2.7 3.1
Attenuation Accuracy	Any Bit or Combination of Bits	DC - 3.0 GHz	dB	+ (0.4 +8% of attenuation setting)		
VSWR	Full Range	DC - 2.0 GHz	Ratio	—	—	1.7:1
Trise, Tfall, Ton, Toff Transients	10% to 90% 50% Cntl to 90%/10% RF In-Band		nS nS mV	— — —	10 30 35	50 150 —
1 dB Compression	Input Power Input Power	0.05 GHz 0.5 - 3.0 GHz	dBm dBm	— —	+20 +28	— —
Input IP3	Two-tone inputs up to +5 dBm	0.05 GHz 0.5 - 3.0 GHz	dBm dBm	— —	+40 +50	— —
Input IP2	Two-tone inputs up to +5 dBm	0.05 GHz 0.5 - 3.0 GHz	dBm dBm	— —	+45 +68	— —
V _{cc} -V _{ee}	— —	— —	V V	4.5 -8.0	5.0 -5.0	5.5 -4.75
V _{ctl} V _{ctl}	Logic (0) TTL Logic (1) TTL	— —	V V	0.0 2.0	— —	0.8 5.0
Input Leakage Current (Low) Input Leakage Current (High)	0 to 0.8 V 2.0 to 5.0 V	— —	μA μA	— —	— —	20 20
I _{cc}	V _{cc} =4.5 to 5.5V	—	mA	—	—	4.0
-I _{ee}	V _{ee} = -5.0 to -8.0	—	mA	—	—	-1

Ordering Information

Part Number	Package
AT65-0233	SOIC-16 Lead Plastic
AT65-0233TR	Tape and Reel (1K Reel)
AT65-0233-TB	Unit Mounted on Test Board

Truth Table

C1	C2	C3	C4	Attenuation
0	0	0	0	Loss, Reference
1	0	0	0	2.0 dB
0	1	0	0	4.0 dB
0	0	1	0	8.0 dB
0	0	0	1	16.0 dB
1	1	1	1	30.0 dB

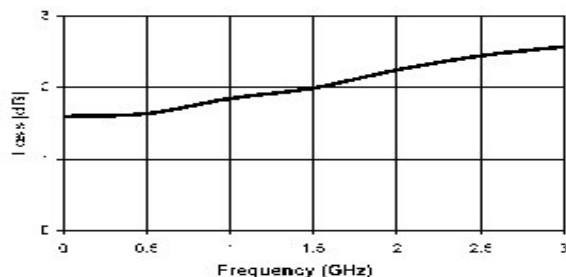
0 = TTL Low; 1 = TTL High

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DC - 3.0 GHz**

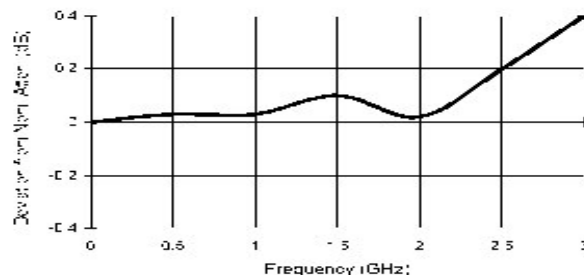
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Typical Performance Curves

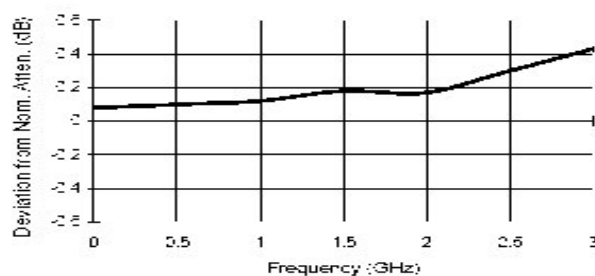
Typical Insertion Loss (dB)



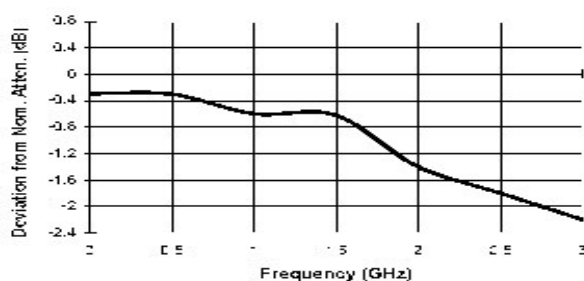
Attenuation Accuracy, 8 dB



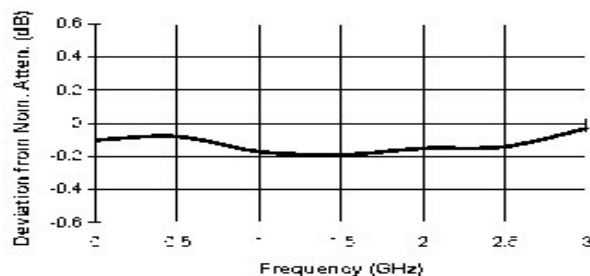
Attenuation Accuracy, 4 dB



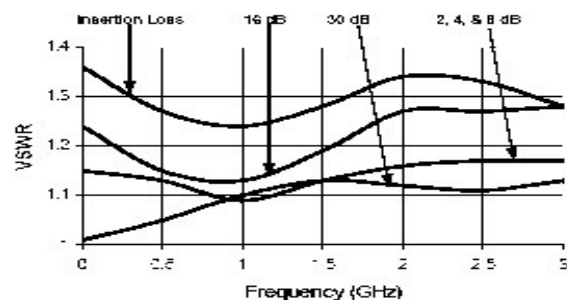
Attenuation Accuracy, 30 dB



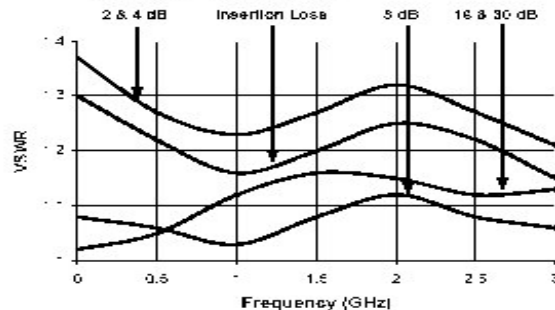
Attenuation Accuracy, 2 dB



Typical RF2 VSWR



Typical RF1 VSWR



Attenuation Accuracy, 16 dB

