

74HC138; 74HCT138

3-to-8 line decoder/demultiplexer; inverting

Rev. 03 — 23 December 2005

Product data sheet

1. General description

The 74HC138; 74HCT138 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL).

The 74HC138; 74HCT138 decoder accepts three binary weighted address inputs (A0, A1 and A2) and when enabled, provides 8 mutually exclusive active LOW outputs ($\bar{Y}0$ to $\bar{Y}7$).

The 74HC138; 74HCT138 features three enable inputs: two active LOW ($\bar{E}1$ and $\bar{E}2$) and one active HIGH (E3). Every output will be HIGH unless $\bar{E}1$ and $\bar{E}2$ are LOW and E3 is HIGH.

This multiple enable function allows easy parallel expansion of the 74HC138; 74HCT138 to a 1-of-32 (5 lines to 32 lines) decoder with just four 74HC138; 74HCT138 ICs and one inverter.

The 74HC138; 74HCT138 can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Not used enable inputs must be permanently tied to their appropriate active HIGH- or LOW-state.

The 74HC138; 74HCT138 is identical to the 74HC238; 74HCT238 but has inverting outputs.

2. Features

- Demultiplexing capability
- Multiple input enable for easy expansion
- Complies with JEDEC standard no. 7A
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- ESD protection:
 - ◆ HBM EIA/JESD22-A114-C exceeds 2000 V
 - ◆ MM EIA/JESD22-A115-A exceeds 200 V
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

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3. Quick reference data

Table 1: Quick reference data

$GND = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; $t_r = t_f = 6\text{ ns}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HC138						
t_{PHL} , t_{PLH}	propagation delay	$V_{CC} = 5\text{ V}$; $C_L = 15\text{ pF}$				
	An to \bar{Y}_n		-	12	-	ns
	E3 to \bar{Y}_n		-	14	-	ns
	\bar{E}_n to \bar{Y}_n		-	14	-	ns
C_i	input capacitance		-	3.5	-	pF
C_{PD}	power dissipation capacitance	$V_I = GND$ to V_{CC}	[1]	67	-	pF
74HCT138						
t_{PHL} , t_{PLH}	propagation delay	$V_{CC} = 5\text{ V}$; $C_L = 15\text{ pF}$				
	An to \bar{Y}_n		-	17	-	ns
	E3 to \bar{Y}_n		-	19	-	ns
	\bar{E}_n to \bar{Y}_n		-	19	-	ns
C_i	input capacitance		-	3.5	-	pF
C_{PD}	power dissipation capacitance	$V_I = GND$ to $(V_{CC} - 1.5\text{ V})$	[1]	67	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

4. Ordering information

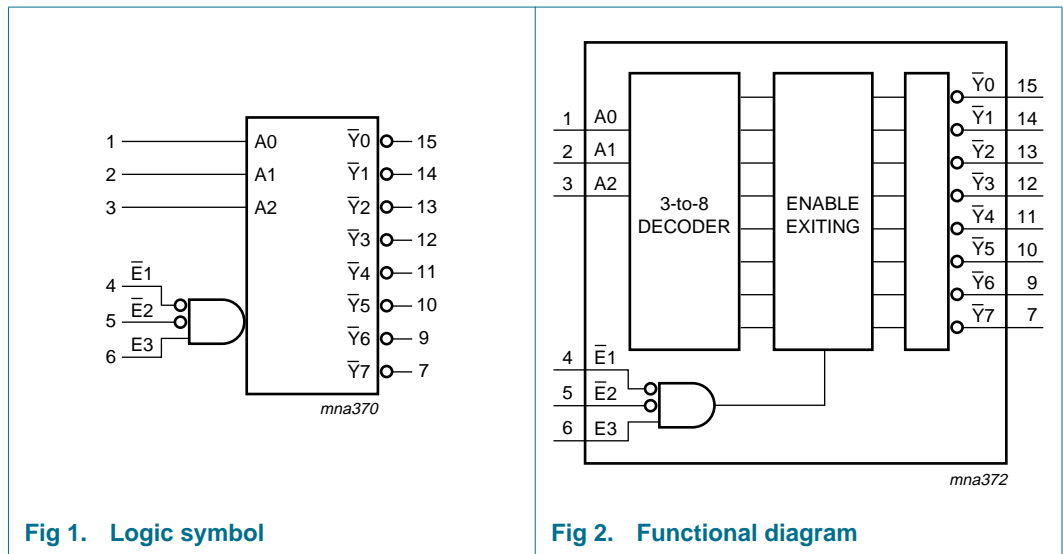
Table 2: Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC138				
74HC138N	-40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
74HC138D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC138DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC138PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC138BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

Table 2: Ordering information ...continued

Type number	Package			Version
	Temperature range	Name	Description	
74HCT138				
74HCT138N	-40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
74 HCT138D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT138DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT138PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT138BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

5. Functional diagram



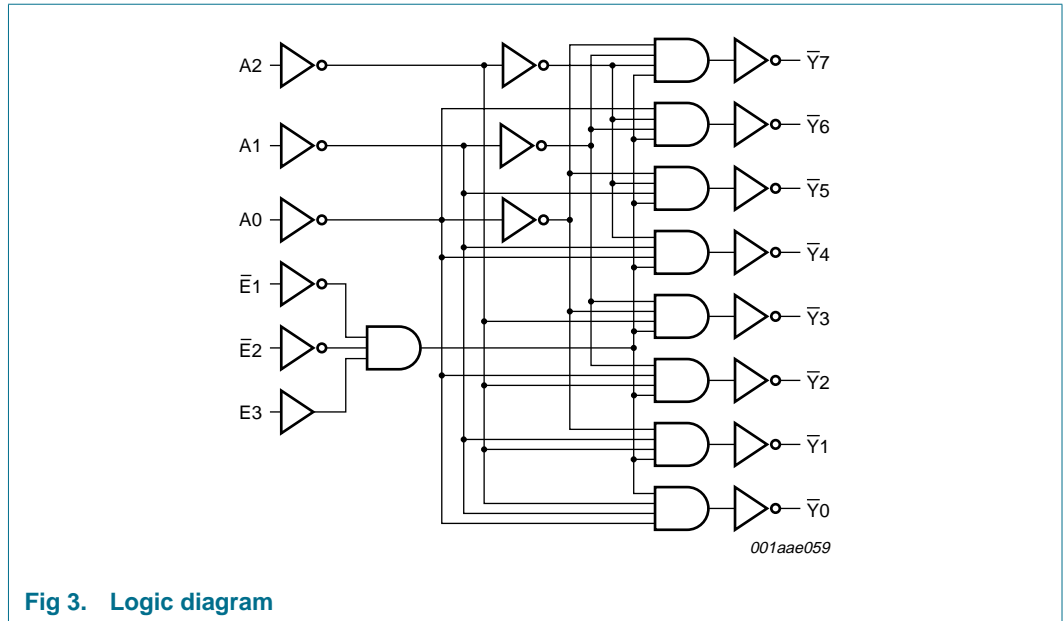


Fig 3. Logic diagram

6. Pinning information

6.1 Pinning

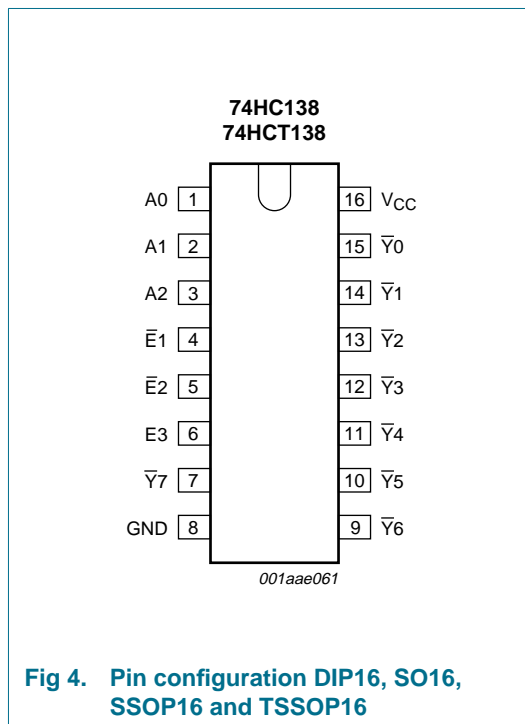


Fig 4. Pin configuration DIP16, SO16, SSOP16 and TSSOP16

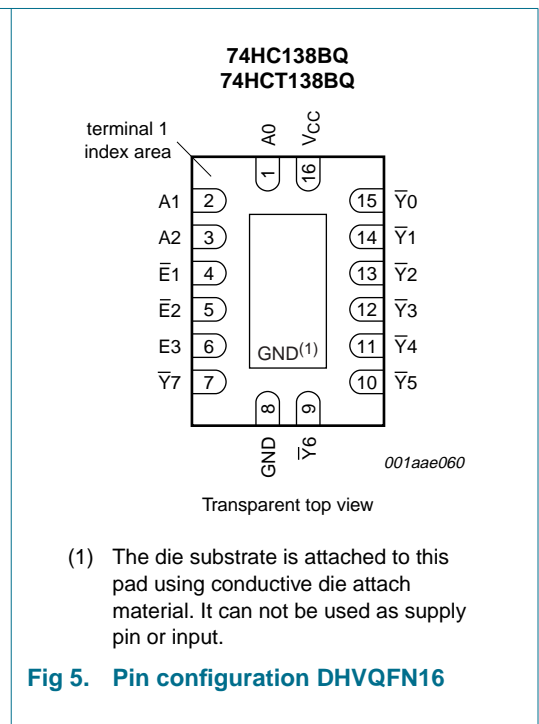


Fig 5. Pin configuration DHVQFN16

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
A0	1	address input 0
A1	2	address input 1
A2	3	address input 2
$\bar{E}1$	4	enable input 1 (active LOW)
$\bar{E}2$	5	enable input 2 (active LOW)
E3	6	enable input 3 (active HIGH)
$\bar{Y}7$	7	output 7 (active LOW)
GND	8	ground (0 V)
$\bar{Y}6$	9	output 6 (active LOW)
$\bar{Y}5$	10	output 5 (active LOW)
$\bar{Y}4$	11	output 4 (active LOW)
$\bar{Y}3$	12	output 3 (active LOW)
$\bar{Y}2$	13	output 2 (active LOW)
$\bar{Y}1$	14	output 1 (active LOW)
$\bar{Y}0$	15	output 0 (active LOW)
V _{CC}	16	positive supply voltage

7. Functional description

Table 4: Function table [1]

Control			Input			Output							
$\bar{E}1$	$\bar{E}2$	E3	A2	A1	A0	$\bar{Y}7$	$\bar{Y}6$	$\bar{Y}5$	$\bar{Y}4$	$\bar{Y}3$	$\bar{Y}2$	$\bar{Y}1$	$\bar{Y}0$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X											
X	X	L											
L	L	H	L	L	L	H	H	H	H	H	H	H	L
			L	L	H	H	H	H	H	H	H	L	H
			L	H	L	H	H	H	H	H	L	H	H
			L	H	H	H	H	H	H	L	H	H	H
			H	L	L	H	H	H	L	H	H	H	H
			H	L	H	H	H	L	H	H	H	H	H
			H	H	L	H	L	H	H	H	H	H	H
			H	H	H	L	H	H	H	H	H	H	H

[1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_O	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$	-	± 25	mA
I_{CC}	quiescent supply current		-	50	mA
I_{GND}	ground current		-	-50	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation				
	DIP16 package		[1] -	750	mW
	SO16 package		[2] -	500	mW
	SSOP16 package		[3] -	500	mW
	TSSOP16 package		[3] -	500	mW
	DHVQFN16 package		[4] -	500	mW

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[4] For DHVQFN16 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HC138						
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
t_r, t_f	input rise and fall time	$V_{CC} = 2.0\text{ V}$	-	-	1000	ns
		$V_{CC} = 4.5\text{ V}$	-	6.0	500	ns
		$V_{CC} = 6.0\text{ V}$	-	-	400	ns
74HCT138						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
t_r, t_f	input rise and fall time	$V_{CC} = 4.5\text{ V}$	-	6.0	500	ns

10. Static characteristics

Table 7: Static characteristics 74HC138

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V _{IH}	HIGH-state input voltage	V _{CC} = 2.0 V	1.5	1.2	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	V
V _{IL}	LOW-state input voltage	V _{CC} = 2.0 V	-	0.8	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	V
V _{OH}	HIGH-state output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	V
V _{OL}	LOW-state output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	V
		I _O = 5.2 mA; V _{CC} = 6 V	-	0.16	0.26	V
I _{LI}	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6 V	-	-	±0.1	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 6.0 V			±0.5	μA
I _{CC}	quiescent supply current	V _{CC} = 6.0 V; I _O = 0 A; V _I = V _{CC} or GND	-	-	8.0	μA
C _i	input capacitance		-	3.5	-	pF
T_{amb} = -40 °C to +85 °C						
V _{IH}	HIGH-state input voltage	V _{CC} = 2.0 V	1.5	-	-	V
		V _{CC} = 4.5 V	3.15	-	-	V
		V _{CC} = 6.0 V	4.2	-	-	V
V _{IL}	LOW-state input voltage	V _{CC} = 2.0 V	-	-	0.5	V
		V _{CC} = 4.5 V	-	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.8	V
V _{OH}	HIGH-state output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	-	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	-	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	-	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.84	-	-	V
		I _O = -5.2 mA; V _{CC} = 6 V	5.34	-	-	V

Table 7: Static characteristics 74HC138 ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{OL}	LOW-state output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 2.0 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	-	0.33	V
		I _O = 5.2 mA; V _{CC} = 6 V	-	-	0.33	V
I _{LI}	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6 V	-	-	±1.0	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 6.0 V			±5.0	μA
I _{CC}	quiescent supply current	V _{CC} = 6.0 V; I _O = 0 A; V _I = V _{CC} or GND	-	-	80	μA
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-state input voltage	V _{CC} = 2.0 V	1.5	-	-	V
		V _{CC} = 4.5 V	3.15	-	-	V
		V _{CC} = 6.0 V	4.2	-	-	V
V _{IL}	LOW-state input voltage	V _{CC} = 2.0 V	-	-	0.5	V
		V _{CC} = 4.5 V	-	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.8	V
V _{OH}	HIGH-state output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	-	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	-	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	-	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.7	-	-	V
		I _O = -5.2 mA; V _{CC} = 6 V	5.2	-	-	V
V _{OL}	LOW-state output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 2.0 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6 V	-	-	0.4	V
I _{LI}	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6 V	-	-	±1.0	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 6.0 V			±10.0	μA
I _{CC}	quiescent supply current	V _{CC} = 6.0 V; I _O = 0 A; V _I = V _{CC} or GND	-	-	160	μA

Table 8: Static characteristics 74HCT138

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V _{IH}	HIGH-state input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V _{IL}	LOW-state input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V
V _{OH}	HIGH-state output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 µA; V _{CC} = 4.5 V	4.4	4.5	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	V
V _{OL}	LOW-state output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 µA; V _{CC} = 4.5 V	-	0.0	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	V
I _{LI}	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	µA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _{CC} = 5.5 V; V _O = V _{CC} or GND; I _O = 0 A	-	-	±0.5	µA
I _{CC}	quiescent supply current	V _{CC} = 6.0 V; I _O = 0 A; V _I = V _{CC} or GND	-	-	8.0	µA
ΔI _{CC}	additional quiescent supply current	per input pin; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A				
		pin An	-	150	540	µA
		pin $\bar{E}n$	-	125	450	µA
		pin E3	-	100	360	µA
C _i	input capacitance		-	3.5	-	pF
T_{amb} = -40 °C to +85 °C						
V _{IH}	HIGH-state input voltage	V _{CC} = 4.5 to 5.5 V	2.0	-	-	V
V _{IL}	LOW-state input voltage	V _{CC} = 4.5 to 5.5 V	-	-	0.8	V
V _{OH}	HIGH-state output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 µA; V _{CC} = 4.5 V	4.4	-	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.84	-	-	V
V _{OL}	LOW-state output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 µA; V _{CC} = 4.5 V	-	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	-	0.33	V
I _{LI}	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±1.0	µA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _{CC} = 5.5 V; V _O = V _{CC} or GND; I _O = 0 A	-	-	±5.0	µA
I _{CC}	quiescent supply current	V _{CC} = 5.5 V; I _O = 0 A; V _I = V _{CC} or GND	-	-	80	µA
ΔI _{CC}	additional quiescent supply current	per input pin; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A				
		pin An	-	-	675	µA
		pin $\bar{E}n$	-	-	562.5	µA
		pin E3	-	-	450	µA

Table 8: Static characteristics 74HCT138 ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = -40\text{ °C to }+125\text{ °C}$						
V_{IH}	HIGH-state input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2.0	-	-	V
V_{IL}	LOW-state input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	0.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}\text{ or }V_{IL}$				
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 4.5\text{ V}$	4.4	-	-	V
		$I_O = -4.0\text{ mA}; V_{CC} = 4.5\text{ V}$	3.7	-	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}\text{ or }V_{IL}$				
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 4.5\text{ V}$	-	-	0.1	V
		$I_O = 4.0\text{ mA}; V_{CC} = 4.5\text{ V}$	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}\text{ or GND}; V_{CC} = 5.5\text{ V}$	-	-	1.0	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH}\text{ or }V_{IL}; V_{CC} = 5.5\text{ V};$ $V_O = V_{CC}\text{ or GND}; I_O = 0\text{ A}$	-	-	± 10.0	μA
I_{CC}	quiescent supply current	$V_{CC} = 5.5\text{ V}; I_O = 0\text{ A};$ $V_I = V_{CC}\text{ or GND}$	-	-	160	μA
ΔI_{CC}	additional quiescent supply current	per input pin; $V_I = V_{CC} - 2.1\text{ V};$ other inputs at $V_{CC}\text{ or GND};$ $V_{CC} = 4.5\text{ V to }5.5\text{ V}; I_O = 0\text{ A}$				
		pin An	-	-	735	μA
		pin $\bar{E}n$	-	-	612.5	μA
		pin E3	-	-	490	μA

11. Dynamic characteristics

Table 9: Dynamic characteristics 74HC138

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified.

For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25$ °C						
t_{PHL} , t_{PLH}	propagation delay					
	An to \bar{Y}_n	see Figure 6				
		$V_{CC} = 2.0$ V	-	41	150	ns
		$V_{CC} = 4.5$ V	-	15	30	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	12	-	ns
		$V_{CC} = 6.0$ V	-	12	26	ns
	E3 to \bar{Y}_n	see Figure 6				
		$V_{CC} = 2.0$ V	-	47	150	ns
		$V_{CC} = 4.5$ V	-	17	30	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	14	-	ns
		$V_{CC} = 6.0$ V	-	14	26	ns
	\bar{E}_n to \bar{Y}_n	see Figure 7				
		$V_{CC} = 2.0$ V	-	47	150	ns
		$V_{CC} = 4.5$ V	-	17	30	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	14	-	ns
		$V_{CC} = 6.0$ V	-	14	26	ns
t_{THL} , t_{TLH}	output transition time	see Figure 6 and 7				
		$V_{CC} = 2.0$ V	-	19	75	ns
		$V_{CC} = 4.5$ V	-	7	15	ns
		$V_{CC} = 6.0$ V	-	6	13	ns
C_{PD}	power dissipation capacitance	$V_I = \text{GND to } V_{CC}$	[1] -	67	-	pF
$T_{amb} = -40$ °C to $+85$ °C						
t_{PHL} , t_{PLH}	propagation delay					
	An to \bar{Y}_n	see Figure 6				
		$V_{CC} = 2.0$ V	-	-	190	ns
		$V_{CC} = 4.5$ V	-	-	38	ns
		$V_{CC} = 6.0$ V	-	-	33	ns
	E3 to \bar{Y}_n	see Figure 6				
		$V_{CC} = 2.0$ V	-	-	190	ns
		$V_{CC} = 4.5$ V	-	-	38	ns
		$V_{CC} = 6.0$ V	-	-	33	ns
	\bar{E}_n to \bar{Y}_n	see Figure 7				
		$V_{CC} = 2.0$ V	-	-	190	ns
		$V_{CC} = 4.5$ V	-	-	38	ns
		$V_{CC} = 6.0$ V	-	-	33	ns

Table 9: Dynamic characteristics 74HC138 ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified.

For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{THL} , t_{TLH}	output transition time	see Figure 6 and 7				
		$V_{CC} = 2.0$ V	-	-	95	ns
		$V_{CC} = 4.5$ V	-	-	19	ns
		$V_{CC} = 6.0$ V	-	-	16	ns
$T_{amb} = -40$ °C to $+125$ °C						
t_{PHL} , t_{PLH}	propagation delay					
	A_n to \bar{Y}_n	see Figure 6				
		$V_{CC} = 2.0$ V	-	-	225	ns
		$V_{CC} = 4.5$ V	-	-	45	ns
		$V_{CC} = 6.0$ V	-	-	38	ns
	E_3 to \bar{Y}_n	see Figure 6				
		$V_{CC} = 2.0$ V	-	-	225	ns
		$V_{CC} = 4.5$ V	-	-	45	ns
		$V_{CC} = 6.0$ V	-	-	38	ns
	\bar{E}_n to \bar{Y}_n	see Figure 7				
		$V_{CC} = 2.0$ V	-	-	225	ns
		$V_{CC} = 4.5$ V	-	-	45	ns
		$V_{CC} = 6.0$ V	-	-	38	ns
t_{THL} , t_{TLH}	output transition time	see Figure 6 and 7				
		$V_{CC} = 2.0$ V	-	-	110	ns
		$V_{CC} = 4.5$ V	-	-	22	ns
		$V_{CC} = 6.0$ V	-	-	19	ns

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

Table 10: Dynamic characteristics 74HCT138

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified.
For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25$ °C						
t_{PHL} , t_{PLH}	propagation delay					
	An to \bar{Y}_n	see Figure 6				
		$V_{CC} = 4.5$ V	-	20	35	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	17	-	ns
	E3 to \bar{Y}_n	see Figure 6				
		$V_{CC} = 4.5$ V	-	18	40	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	19	-	ns
	\bar{E}_n to \bar{Y}_n	see Figure 7				
		$V_{CC} = 4.5$ V	-	19	40	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	19	-	ns
t_{THL} , t_{TLH}	output transition time	see Figure 6 and 7				
		$V_{CC} = 4.5$ V	-	7	15	ns
C_{PD}	power dissipation capacitance	$V_I = \text{GND to } (V_{CC} - 1.5 \text{ V})$ [1]	-	67	-	pF
$T_{amb} = -40$ °C to $+85$ °C						
t_{PHL} , t_{PLH}	propagation delay					
	An to \bar{Y}_n	see Figure 6				
		$V_{CC} = 4.5$ V	-	-	44	ns
	E3 to \bar{Y}_n	see Figure 6				
		$V_{CC} = 4.5$ V	-	-	50	ns
	\bar{E}_n to \bar{Y}_n	see Figure 7				
		$V_{CC} = 4.5$ V	-	-	50	ns
t_{THL} , t_{TLH}	output transition time	see Figure 6 and 7				
		$V_{CC} = 4.5$ V	-	-	19	ns
$T_{amb} = -40$ °C to $+125$ °C						
t_{PHL} , t_{PLH}	propagation delay					
	An to \bar{Y}_n	see Figure 6				
		$V_{CC} = 4.5$ V	-	-	53	ns
	E3 to \bar{Y}_n	see Figure 6				
		$V_{CC} = 4.5$ V	-	-	60	ns
	\bar{E}_n to \bar{Y}_n	see Figure 7				
		$V_{CC} = 4.5$ V	-	-	60	ns
t_{THL} , t_{TLH}	output transition time	see Figure 6 and 7				
		$V_{CC} = 4.5$ V	-	-	22	ns

- [1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

12. Waveforms

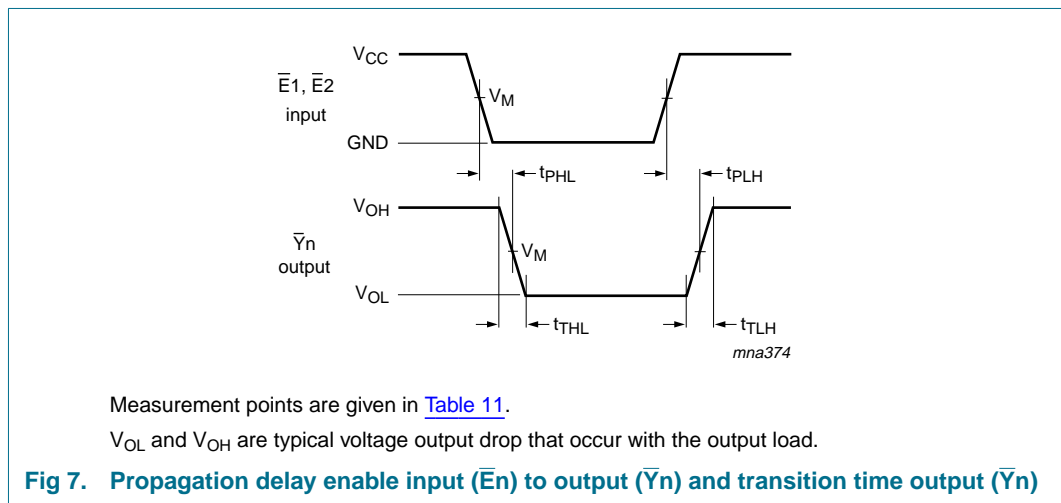
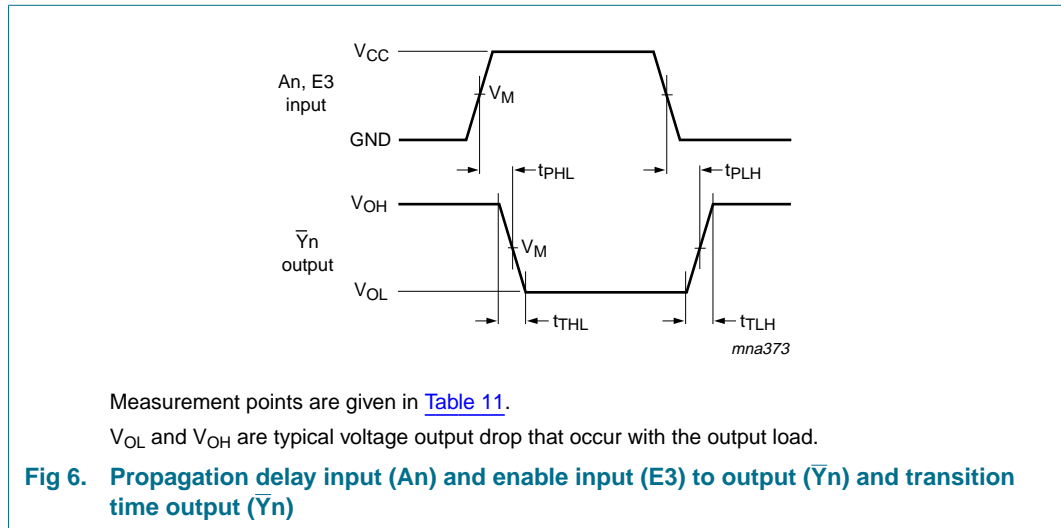


Table 11: Measurement points

Type	Input	Output
	V_M	V_M
74HC138	$0.5V_{CC}$	$0.5V_{CC}$
74HCT138	1.3 V	1.3 V

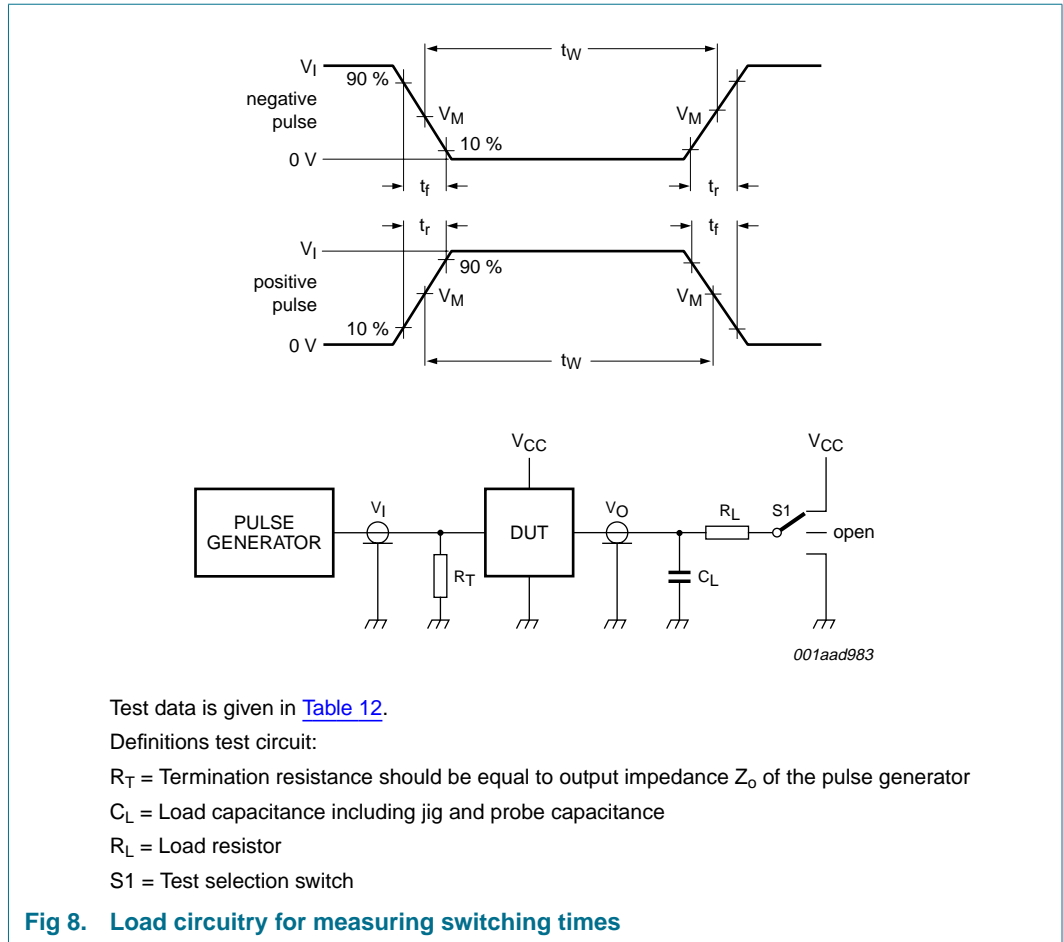


Table 12: Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC138	V_{CC}	6 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}
74HCT138	3 V	6 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil); long body

SOT38-1

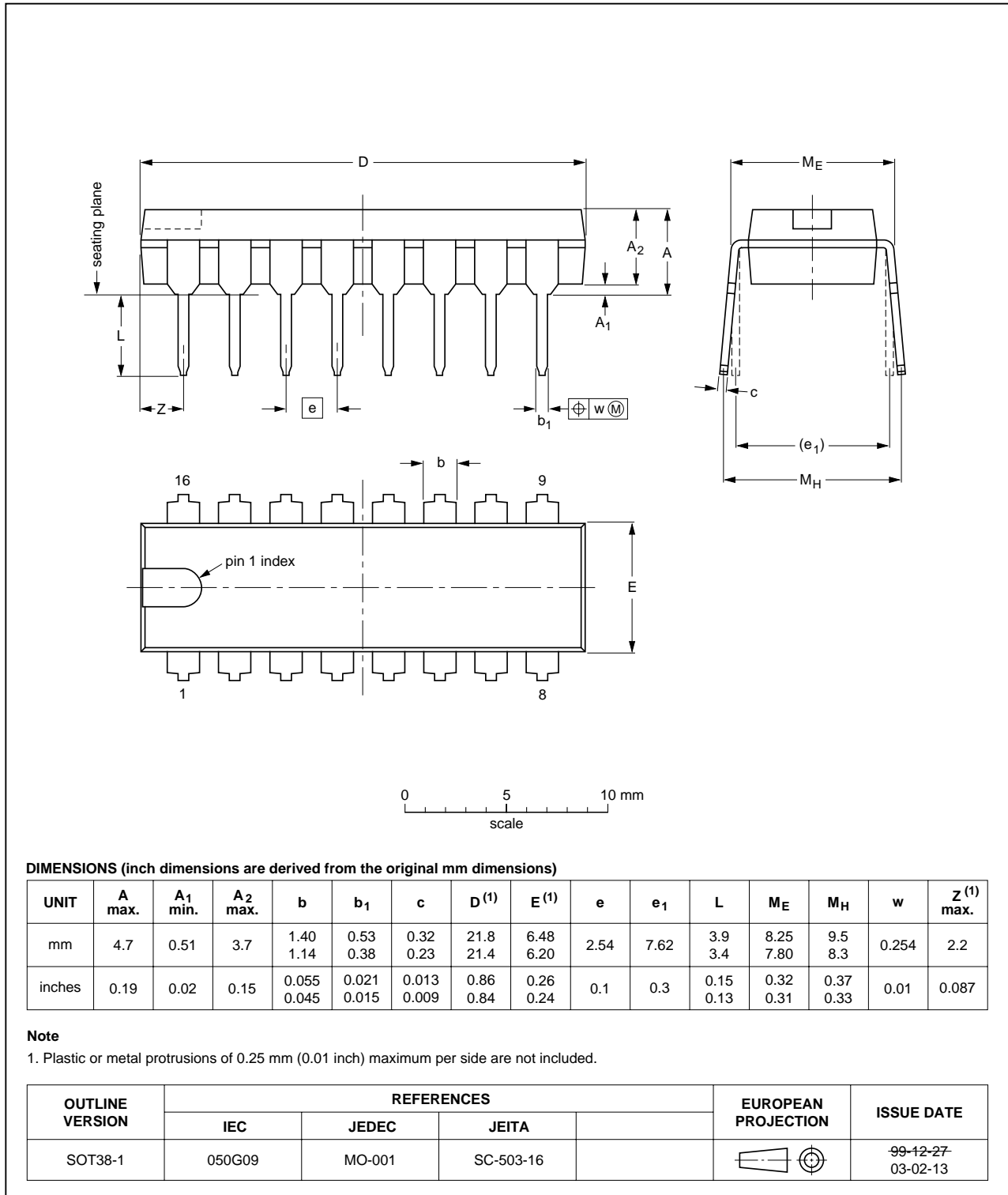


Fig 9. Package outline SOT38-1 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

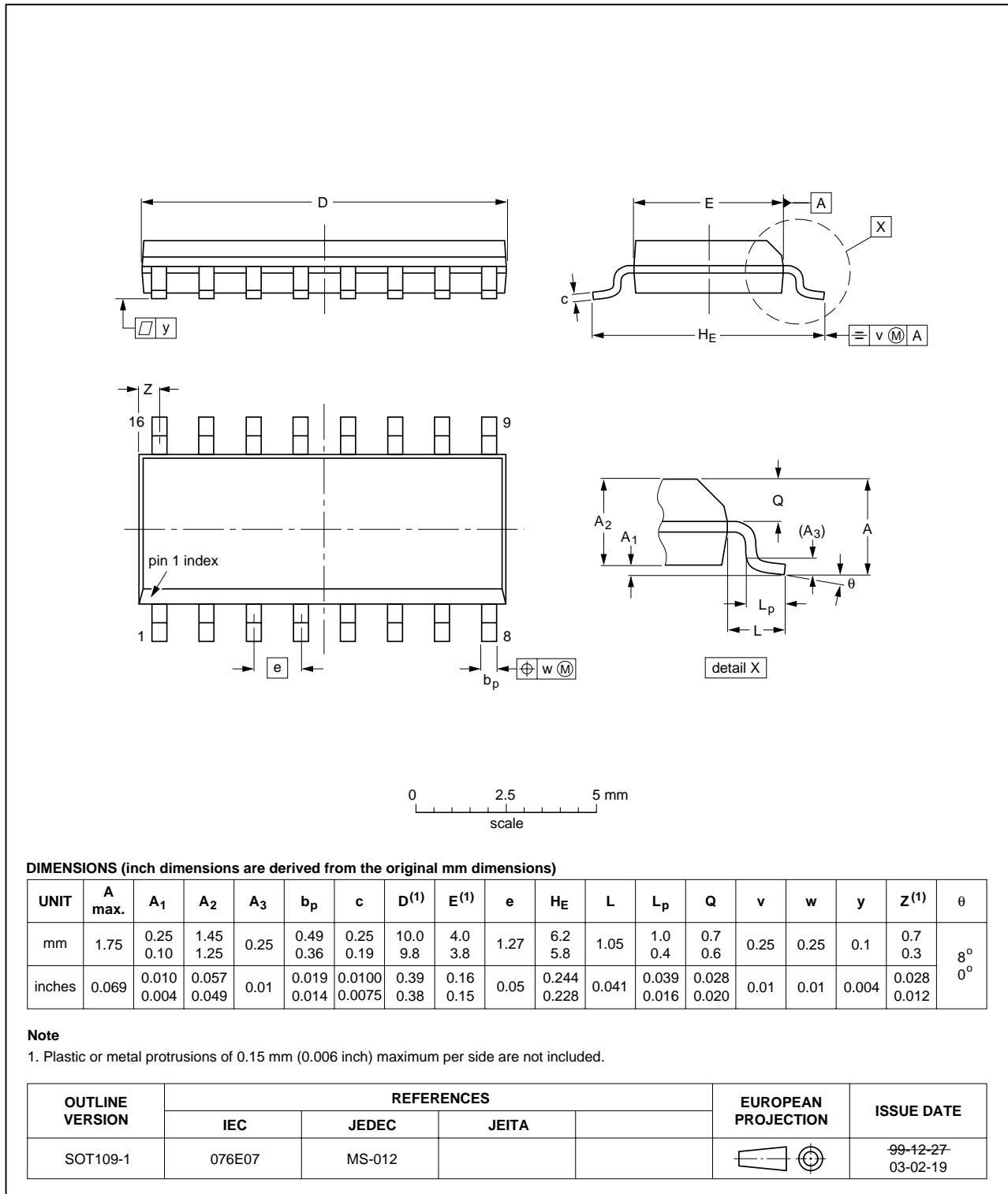


Fig 10. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

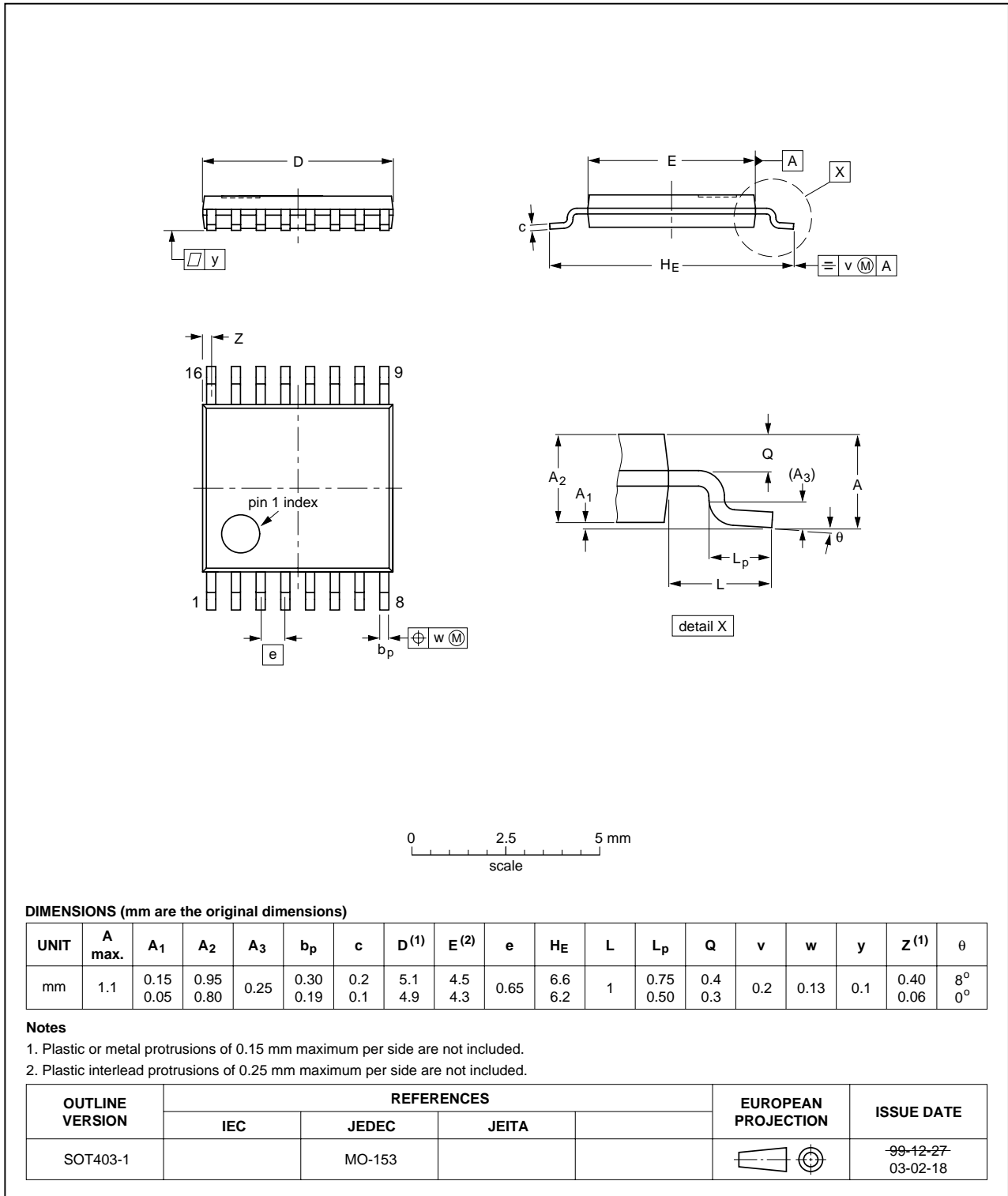


Fig 11. Package outline SOT403-1 (TSSOP16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

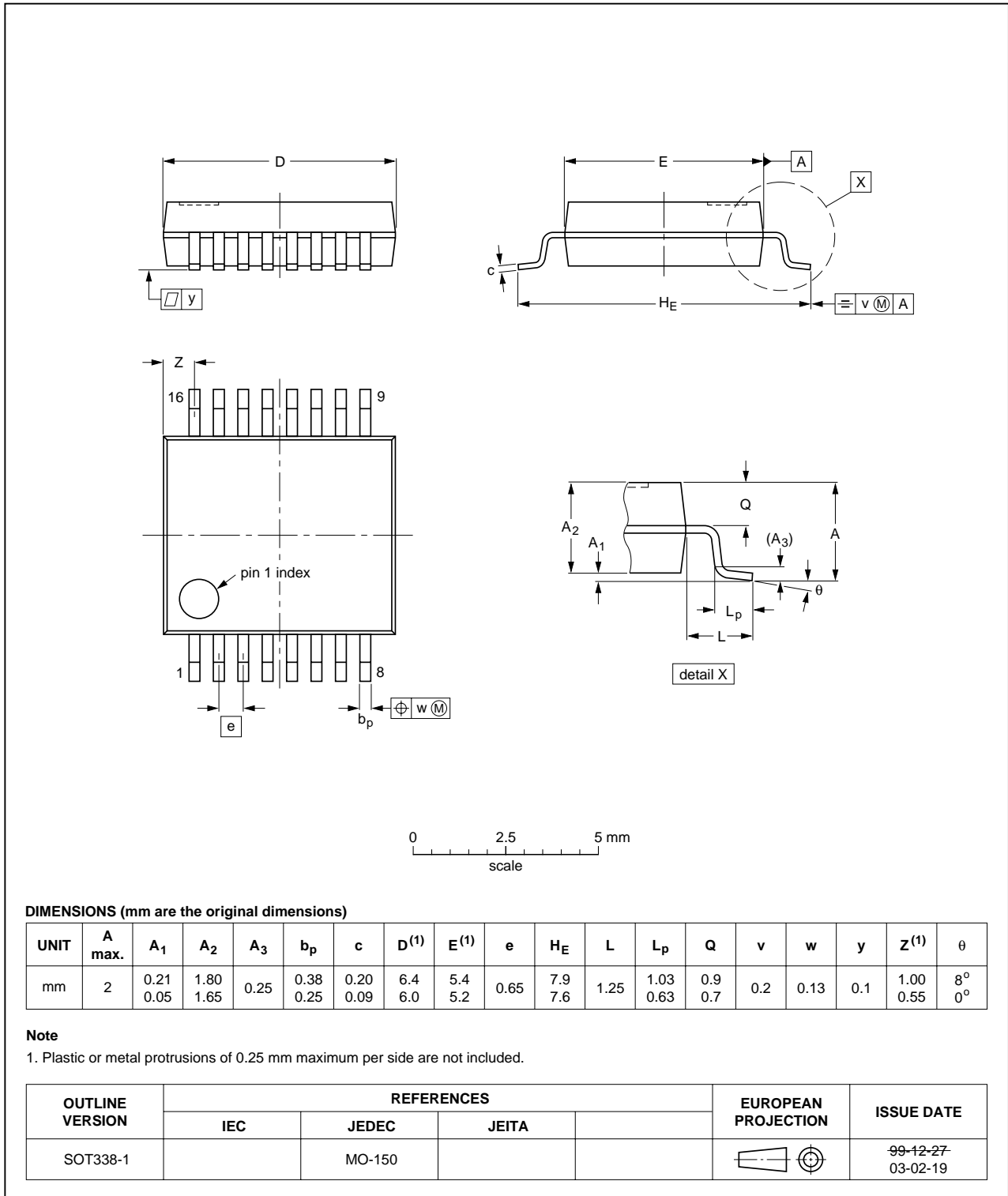


Fig 12. Package outline SOT338-1 (SSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

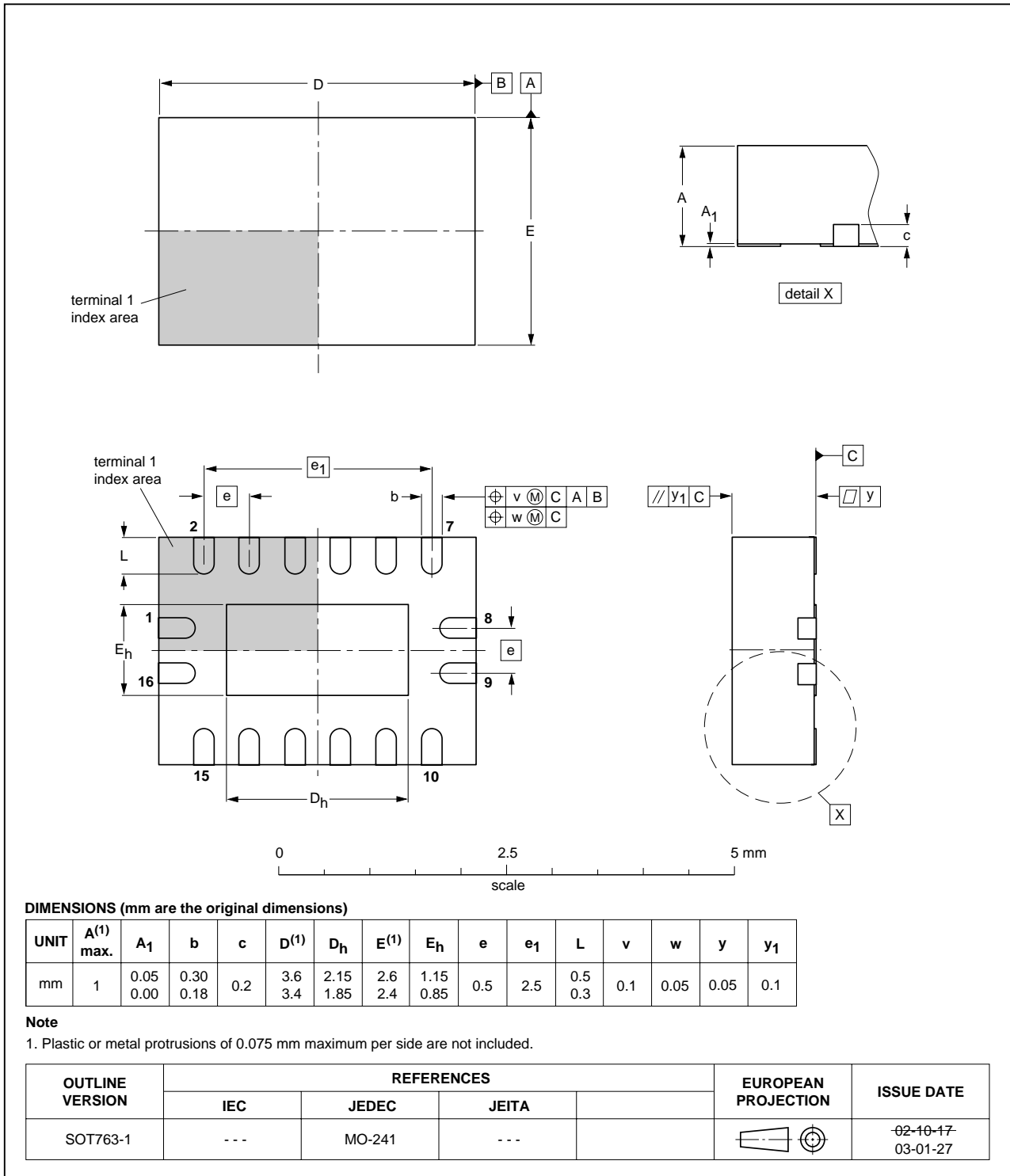


Fig 13. Package outline SOT763-1 (DHVQFN16)

14. Abbreviations

Table 13: Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model

15. Revision history

Table 14: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74HC_HCT138_3	20051223	Product data sheet	-	-	74HC_HCT138_CNV_2
Modifications:					
					<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. Section 4 "Ordering information", Section 6 "Pinning information" and Section 13 "Package outline": Added DHVQFN package information Section 10 "Static characteristics": Added from the family specification
74HC_HCT138_CNV_2	19970827	Product specification	-	-	-

16. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Date of release: 23 December 2005
Document number: 74HC_HCT138_3

Published in The Netherlands